

Modelling of Digital HVDC Control Systems Using a Graphical Electromagnetic Simulation Program

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Abstract - This paper describes the modelling of Siemens programmable high speed control system (SIMADYN D) for HVdc / SVC systems using a graphical digital electromagnetic transients program (PSCAD/EMTDC). The control system model is created graphically very similar to the graphical programming of the actual control system at a function block level. The model directly executes the same arithmetic and logic functions as used by the actual control system, including the processing time step, giving very high correlation of function behavior. This results in very fast and flexible programming of any control system associated with a HVdc system. This greatly enhances confidence in the model and gives faster study results even for complex systems. The availability of detailed HVdc control and protection models allows a much broader application of digital simulation including design of new project dependent control features, optimization of control performance, protection co-ordination, support during system commissioning among others.

I. INTRODUCTION

With the development of commercially available graphically programmed digital simulation tools such as PSCAD/EMTDC [1] and with the availability of powerful workstations it is practical to develop much more sophisticated control system representations. Considerable progress has been made in the modelling of analog control systems used in earlier schemes [2,3]. However the modelling of digital controls is relatively new [4].

Whereas several earlier formulations of HVdc control models have included linear representation of the basic control loops (with limits as required), the approach used here involves no simplification of the control loops. One important feature of the modelling philosophy used here is the accurate representation of the different time-steps used in the actual digital controls. These controls use various different time-steps, which impact on the stability and dynamic performance limits of the controller.

While the simplified models satisfied most of the requirements of the system oriented planning studies, such models could not easily be applied to more control performance related studies. Such tests have been the domain of the real time TNA/DC Simulator using actual control system hardware and software.

The direct digital control modelling technique described here expands the possible applications of electromagnetic transients simulations to studies that require a very precise control model. This can reduce the dependance of the HVdc supplier or user on the conventional HVdc simulator/TNA for many detailed control studies.

II. DESCRIPTION OF SIMADYN D CONTROL SYSTEM

The SIMADYN D control system [5] is a multi-processor system for fast closed-loop control and arithmetic operations, open-loop control and monitoring and for signaling and logging. The programmable SIMADYN D control system is used by Siemens for all HVdc and SVC applications [6] where it is utilized both for control and protection functions.

A. Hardware

The multi-processor control system is made up of various plug-in boards optimally configured in a rack for HVdc/SVC type applications with the typical components as follows. Several different *processor boards* can be used depending the application and peripheral interface requirements with up to eight processor boards in one sub-rack. Each processor board has its own program and data memory and processes its allocated tasks independent of other processors. The *program memory sub-module* inserted in each processor board contains the system and application software. The parallel processors communicate via a local bus through a *communication buffer board*. *Input/output boards* interface the processors to external systems and signals with normalized input and output levels. *Interface sub-modules* which can be inserted in the processor board provide standardized serial interface (20mA, V.24 or EIA 485) for data exchange with other equipment and systems. Separate *Communication boards* are also used for serial data exchange if required.

B. Software

The programming of control or protection functions, including all control parameter settings, is done graphically using STRUC G configuring software

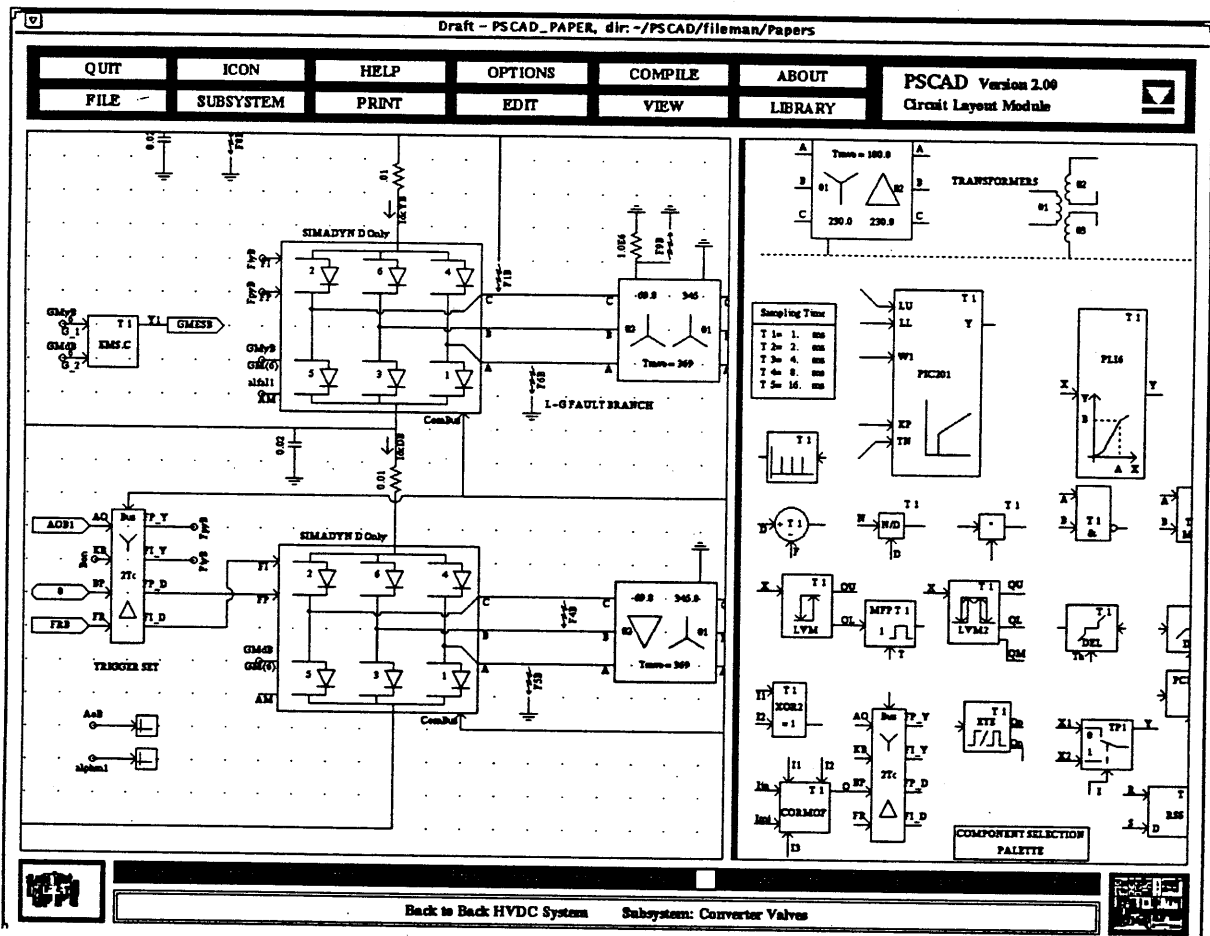


Fig. 1. Draft module for circuit construction

with function blocks available from an extensive library of control functions. The library consists of control blocks, converter specific blocks, arithmetic blocks, logic and switch blocks, and input/output blocks. Execution time step of these function blocks from 100 μ s and up are assigned according to the response time requirements of the particular control loop or protection application. Up to five different sampling times can be assigned to each processor. The valve firing system ("trigger set") and extinction angle measurement are specially created function blocks for HVdc applications with corresponding specific high-speed processors that ensure firing pulse and extinction angle accuracy of $\pm 0.1^\circ$. The software also includes the communication functions to handle data transfer within the SIMADYN D system and with external systems. Diagnostic software identifies errors/faults in the SIMADYN D system and provides external signals to allow the appropriate contingency actions such as switch-over to a redundant control channel. The control function software is self documenting.

III. GRAPHICAL SIMULATION INTERFACE

The SIMADYN D Library was developed in the PSCAD/EMTDC environment discussed briefly below. The PSCAD/EMTDC module called *Draft* contains the

drawing palette shown in Fig. 1. The displayed area shows a part of the negative pole circuit of a bipolar 600 MW HVdc system. The components needed to build the circuit are picked up from the component library on the right hand side and placed on the drawing canvas as seen in Fig. 1. In the figure, in addition to the power circuit, some control system blocks such as the firing pulse generator or the "trigger set" are also visible although conventionally the control circuit is usually drawn on a separate page from the power circuit. The parameters for the components are selected using a pop-up menu as seen in Fig. 2, which shows the parameters being selected for a proportional-integral gain block.

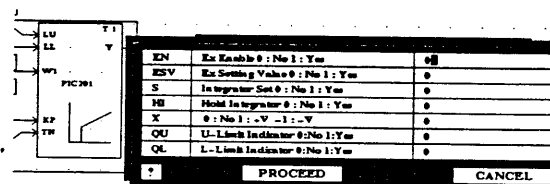


Fig. 2. Data Entry via Pop-Up Menu

The components are connected using the stretchable wire components. Control circuit wires can also be referenced by using the wire label component. Any points connected by the same signal label are automatically con-

nected. For example in Fig. 1, the measured extinction angle signal (GMyB) from the upper 6-pulse group is passed onto the minimum γ selection block on the left using these technique. If the circuit has several identical sub-circuits (e.g., each pole of an HVdc station is more or less similar) it is only necessary to draw the first subcircuit and merely copy and paste it several times. Minor changes can then be introduced into the pasted sections.

After the circuit is completed, the run is initiated on another module called *Runtime*. The *Runtime* palette allows the user to customize the appearance of the console to show as many of the curves required. Any number of graphical plot windows may be opened. Also run control devices such as sliders and switches can be opened for interactive control of the program. The *Runtime* palette in Fig. 3 shows a typical screen appearance for a controller performance study of a 600 MW HVdc system illustrating recovery from a dc line fault. Controller gains, reference settings or any other value may be changed interactively during the course of the run. The program may also be paused, single-stepped through or re-started using the tape-recorder type buttons on the menu bar immediately above the graphs. Also, cross-hairs and zoom in/out features are available for closer inspection of the traces. In addition to the graphs, the output can also be displayed on a meter as an analogue or digital display. The results (i.e., the data corresponding to the plots) can also be stored in

output files for further processing (such as Fourier Analysis, etc.). Other control artifacts such as dials, push-buttons (to initiate faults or start an event) are also available on the *Runtime* palette. Thus if all the necessary blocks are available, the circuit can be constructed with great ease and rapidity. The interactive feature makes the *Runtime* module an extremely convenient medium to conduct the control studies. However for presentation quality reports, a separate plotting/analysis module is used.

IV. DEVELOPMENT OF CONTROL MODELS

The power circuit components required for the simulation of HVdc System dynamics can usually be found within the selection available with standard electromagnetic transients programs. However for detailed studies in which specific parameters of a control system are to be selected or while investigating the controller interactions in an actual or proposed control scheme, the controls must be modelled very precisely. In order to avoid excessive simulation duration, it is customary to use simulation time-steps in the order of 25-50 μ s. Based on this, the control models may be divided into three different categories:

A. Analog Circuits

These include anti-aliasing filters, transducers, measurement delays and so on. The integration step used

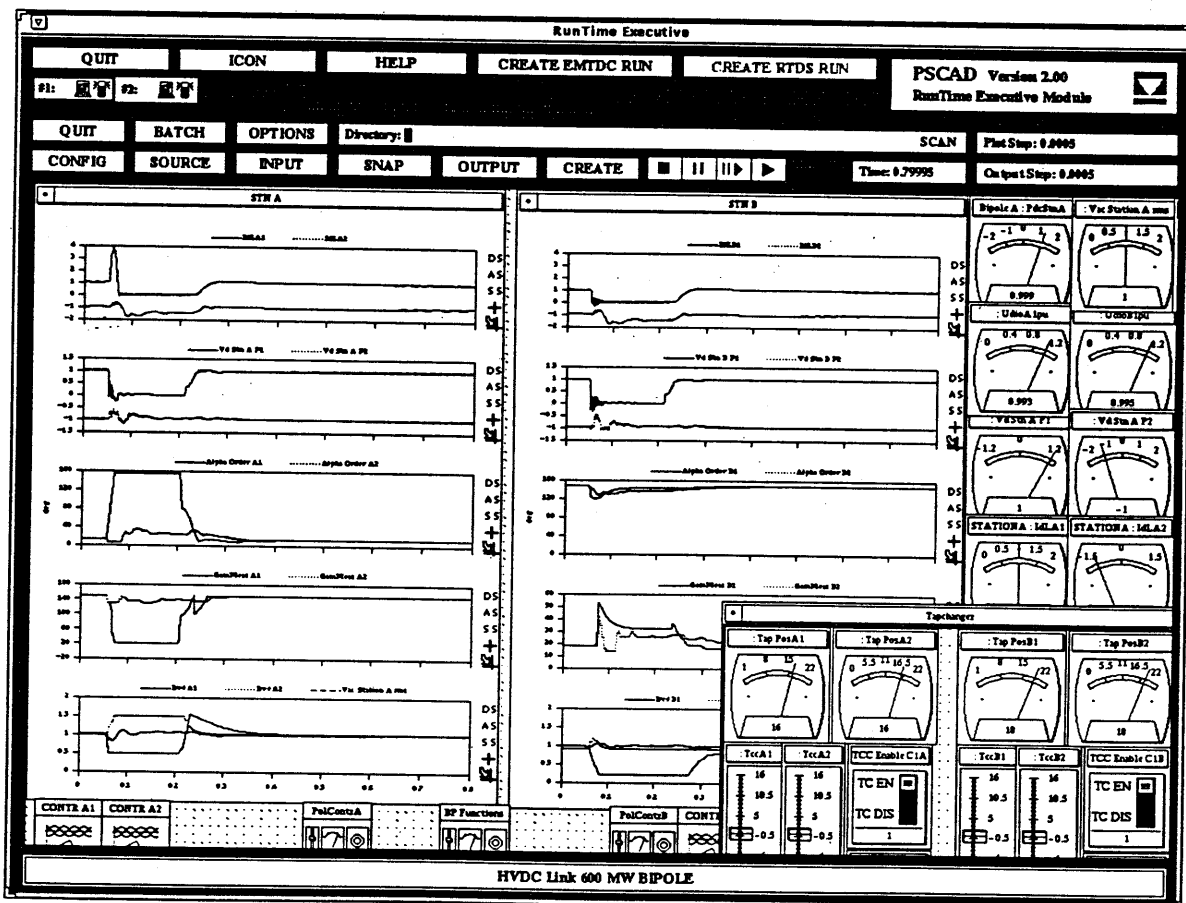


Fig. 3. RUNTIME Palette

in these models is equal to the simulation program's time step as the actual systems exhibit continuous-time behavior. For more accurate simulation interpolation between time-steps is required. For example a 50 μ s time-step represents about one 1° on a fundamental frequency waveform whereas firing control systems often require a resolution of about 0.1° . Other modelling considerations are discussed in earlier literature and will not be discussed further.

B. Very Fast Digital Controls

Some specialized control blocks particularly those in the firing control system (trigger set) or extinction angle measurement are often digital processor systems operating at time steps of less than 1 μ s. For modelling purposes, these are treated in the same manner as the analog blocks described above.

C. Other Control Blocks

These form the bulk of the control system and are the ones that are normally considered in the design of specific controllers for an HVdc system. These are the blocks available in the SIMADYN D Library discussed earlier. In the actual system, these blocks are implemented in the software program that runs on the control hardware. Thus in one sense they should be straightforward to model as the actual software could be emulated in the transients simulation program. On the other hand they are different from analog control models because each block operates on its assigned time-step which is a multiple of the minimum time-step in the microprocessor based control system. In addition, some blocks are capable of being 'hardware interrupted' by an external signal if some urgent function is required of them before their normal sample time.

We now discuss the modelling philosophy with the specific example of a Proportional-Integral Controller (SIMADYN D Block PIC201) shown in Fig. 2. In this

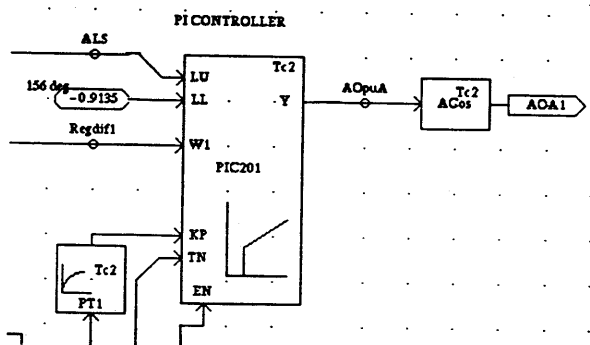


Fig. 4. Control Block PIC201

figure W1 is the input to the block, KP and TN the pro-

portional gain and integral time constant, LL and LU the upper and lower limits. The output Y is derived from W1 according to the equation below:

$$Y_n = Y_{n-1} + KP \left[\left(1 + \frac{TA}{TN} \right) W1_n - W1_{n-1} \right]$$

In the figure, the output signal is further transmitted to downstream control blocks. The gains and limits are not fixed and can themselves be the outputs of other blocks. Additional inputs and outputs to the block can be enabled and the connection wires become visible on the palette upon selection. In the PSCAD/EMTDC model, the same features is modelled, as can be seen from Fig. 2 which shows the corresponding PSCAD menu for the component. The following steps were carried out in the design of the PSCAD component:

1) Construction of the Graphical Icon

This is a straightforward function that is carried out using the Graphical Design Language of the PSCAD program, which includes function calls for drawing lines, arcs, text, menus, etc., and allows specification of the FORTRAN code that the block is required to execute. Once the a rough design for the block has been developed, its description can be modified or the FORTRAN code directly edited from PSCAD's *Draft* palette in the manner shown in Fig. 5.

2) Construction of the Fortran Subroutine

The appropriate FORTRAN code is now typed in usually in the form of a subroutine. Fig. 5 shows a fragment of the code for this block. The time-step is modeled by keeping an internal count of the number of times the subroutine was entered (once every PSCAD/EMTDC time-step) and only executing the contents of the subroutine when the count reaches the contents of the subroutine when the count reaches the desired multiple value. The time-step to be used is entered via the pop-up menu and appears on the top right corner of every component (see for example, Fig. 4).

3) The Timing Selection Block

One function block assigns the various time-steps that are required by each control block. This block has no visible outputs, but an internal FORTRAN array makes these values available throughout the PSCAD/EMTDC environment. The pop-up menu for this component is shown in Fig. 6. In this example the menu shows that time-steps ranging from 0.5 ms to 16 ms can be selected by assigning sample times T1 through T5 to any control block as required.

D. Validation of the Control Models

To validate the results, each designed block was subjected to tests to confirmed its adherence to the wave-

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Title: UNIVERSAL PI CONTROLLER ( PIC201 2/14 )
Written by X. Jiang
April 6, 1993

SUBROUTINE PICUS6(W,X,LU,LL,Kp,Tn,S,HI,EN,SV,NO,
TTa,Ta,IC,Y,QU,QL)

INPUT OUTPUT
W Setpoint (Input Signal)
X Actual Value (Input Signal)
LU Upper Limit
LL Lower Limit
Kp Proportional Gain
Tn Reset Time
S Integrator Set
HI Hold Integrator
EN External Enable
SV External Setting Value
NO Order of FB
TTa Sampling Indicator
Ta Sample Time ( Ta/Delta )
IC I-Controller Enable

Y Output Signal
QU Upper Limit Indics
QL Lower Limit Indics

Include and Common Block Declarations
INCLUDE 'out.d'
INCLUDE 'out.e'
COMMON /S1/TIME,DELT,ICH,PRINT,FINTIM
COMMON /S2/STOR(N010),NEXC
  
```

Fig. 5. Fragment of FORTRAN code for PIC201

T	Name of Sample Time	T ₁
T1	1st Sampling Time	0.5
T2	2nd Sampling Time	1
T3	3rd Sampling Time	2
T4	4th Sampling Time	8
T5	5th Sampling Time	16
?		

PROCEED

Fig. 6. Selection of Sampling Time

forms shown in the SIMADYN D Manual [5]. The block was required to exhibit the same response as that in the manual for all possible operating states. Fig. 7 shows a typical comparison of simulated and catalogued waveforms that was used to validate the PIC201 component.

Special attention was given to the blocks related to the measurement of converter quantities and to the trigger set (see subsections A and B of section IV). In the case of the trigger set extensive comparisons were carried out with the actual hardware.

V. VALIDATION OF SYSTEM MODEL

In addition to the control block verification, substantial comparisons between the digital model and the conventional HVdc Simulator/TNA have been conducted for complete HVdc systems. Fig. 8 shows a comparison of results obtained from a digital simulation and an analog simulator at FGH Mannheim. The controls used in the digital simulation are comprised completely of SIMADYN D building blocks identical to the actual control system used in the analog simulation. The test shown in the

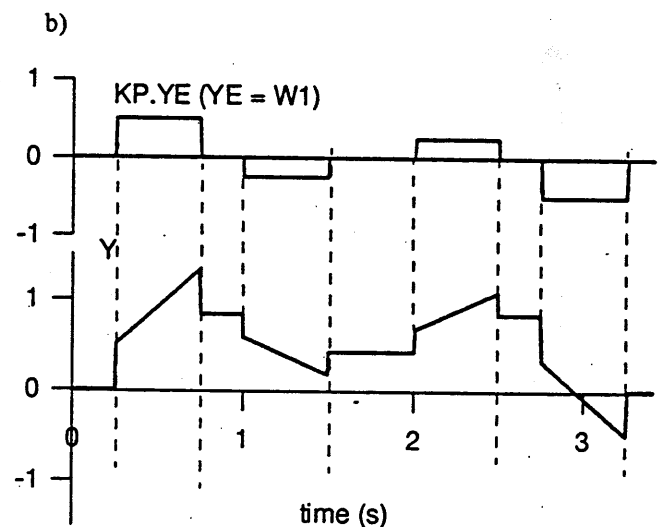
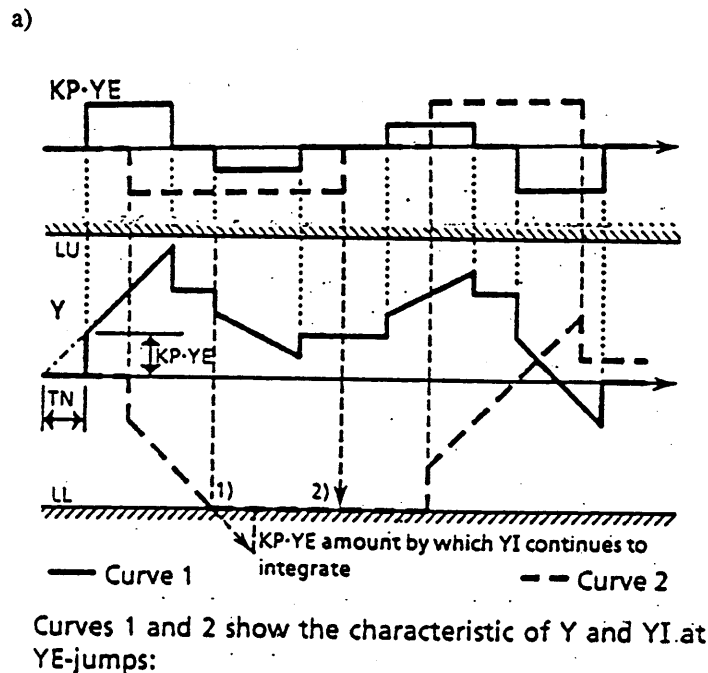
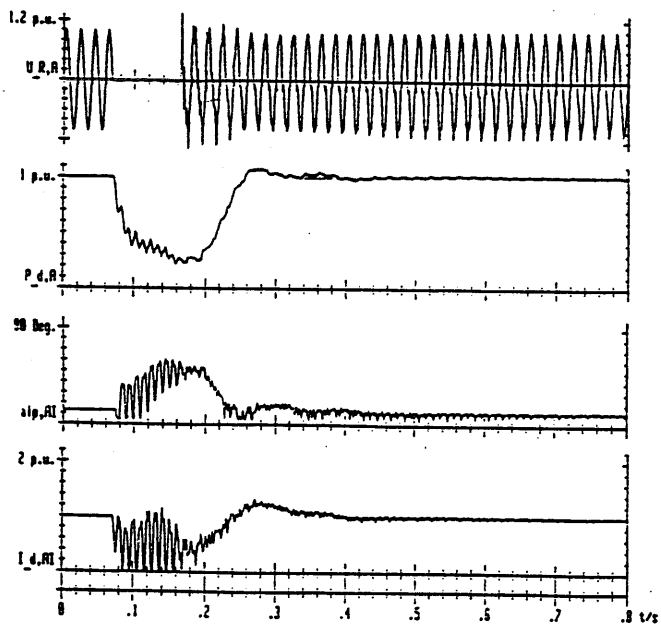


Fig. 7. Waveforms for P-I block a) Catalogued b) Simulated figure is for a rectifier side solid single phase to ground fault. The traces for ac voltage on the faulted phase, the dc power, the firing angle and the dc current at the rectifier are shown. As can be seen, the agreement is excellent.

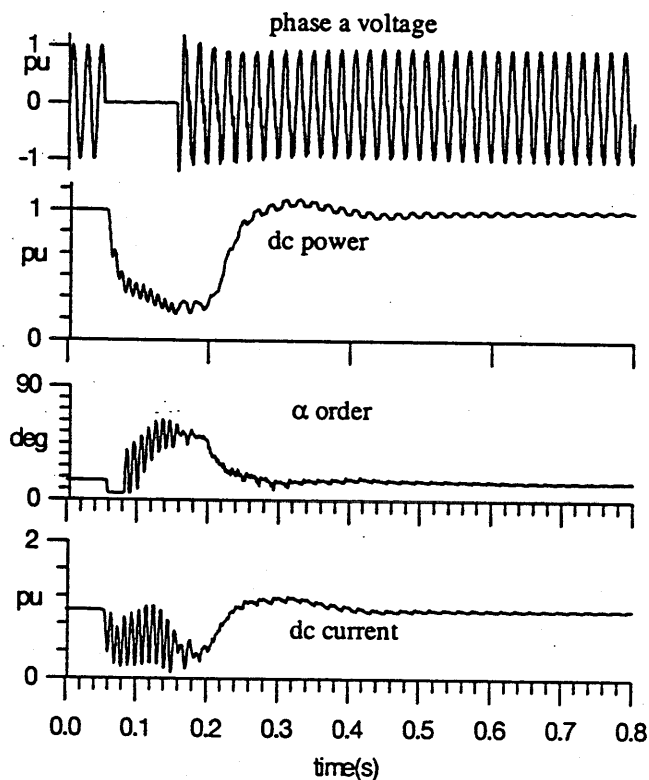
These comparisons allow us to increase our reliance on the developed digital models and the simulation environment for performance studies

VI. CONCLUSIONS

Extremely accurate models for the SIMADYN D control library have been developed for use in an electromagnetic transients simulation program. The accuracy of the models has been extensively checked against the standard catalogue and laboratory tests. The graphical format



a) TNA Results



b) Simulated Results

Fig. 8. Comparisons of digital and TNA Results for l-g fault on 1800 MW HVdc System

that has been used make the simulation particularly straightforward to set up. Conventional Copy/Paste commands can now be used to extend the size of the network.

Connection errors are easy to find as the information is contained in pictorial form. In addition, the run-time interface gives the look and feel of a control desk or a Analog Simulator/TNA control panel. Dials, switches and sliders are controllable during the progression of the run. This saves the need for detailed post-processing.

While digital simulation was formerly used primarily for the planner working at the system level the development reported here expands its applications. The detailed digital control model can be used as a preliminary design tool with immediate verification of function very similar to dc simulator/TNA work. This may significantly reduce costly development work on the simulator/TNA. In the same way this digital model has the potential to reduce the need for resolution of unexpected during site commissioning when a dc simulator may not be readily available. The type of model developed here is also very useful for development and testing of protection functions for any dc station equipment including converter equipment, ac and dc filters, etc. Due to the direct correlation between the digital model and the SIMADYN D controls, the model translates more directly into the actual control design with significant time saving.

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