Investigation of the False Operation of a Digital Directional Comparison Relay During 500-kV Series Capacitor Reinsertion

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Abstract - **False operation of a new set of digital directional comparison relays occurred on the Winnipeg-Twin Cities 500-kV line during reinsertion of a set of series capacitors. Capacitor reinsertion under load produces subharmonic transients that look like a forward fault to the relay. An EMTP study determined that lowering the relay sensitivity is not secure. An alternative algorithm is proposed which adds negative sequence and zone 2 supervision to the directional relay's trip signal.**

Keywords: protection, EMTP, series capacitor, directional comparison, real time playback, field testing.

I. INTRODUCTION

A 500-kV line, interconnecting Manitoba Hydro with Minnesota Power and Northern States Power, was completed in May 1980 [1]. A single line diagram showing the major 500-kV facilities between Winnipeg (Dorsey bus) and the Twin Cities (Chisago bus) is given in Fig. 1.

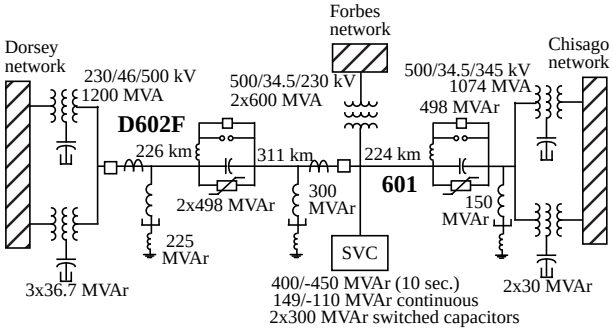

Fig. 1. Winnipeg-Twin Cities 500-kV single line diagram.

Two independent protection systems with separate communications were provided for the 537 km north section (D602F) and 224 km south (601) section. The installed protection relays on the north line are memory polarized impedance (ZM) type while the south line uses one ZM relay and one phase comparison (PC) system.

In May 1993, the north section of the 500-kV line was upgraded to include 50% series compensation near the midpoint of the line [2]. The south line was upgraded to include 56% series compensation at the southern end. With the addition of series capacitors, modifications in the relay settings were required in order to avoid such things as overreaching on remote faults due to the reduced transmission line impedance. Tests were conducted in October 1991, using the Real Time Digital Simulator (RTDS) developed by the Manitoba HVdc Research Centre [6]. Approximately 40 balanced and unbalanced fault tests were applied to each set of relays at Dorsey and Forbes on line D602F and each relay at Forbes and Chisago on line 601. In total, 236 RTDS tests were conducted. The new settings proposed following the testing have functioned properly since the series capacitors were placed in-service. More reliance on communication is required as a single set of protection settings are required to function regardless of the status of the series capacitors.

A static var compensator was installed between the north and south 500 kV lines at the Forbes substation in May 1994 [3]. Protection settings did not require modification.

Northern States Power advised the Manitoba/Minnesota protection working group in 1997 that the existing 500-kV line relays were in need of replacing due to continuing problems with troubleshooting and repair. The relay package chosen to be installed in November 1998, was a digital superimposed directional (SD) comparison protection relay. Hydro Québec also uses superimposed directional (SD) and current differential (CD) relays on their 765-kV series-compensated network with memory polarized impedance (ZM) relays used as backups [4].

On February 4, 1999, two outages of the north line were caused by false operation of the new relay during reinsertion of the series capacitors under load. The original voltage trip setting was 2.0 V. The actual change in voltage experienced during the two events was 5.5 V (800 MW on D602F) and 3.75 V (420 MW on D602F). A temporary operating restriction is in place that requires the new relay to be disabled during series capacitor insertion. Aggarwal *et al.* mentions that problems can arise during series capacitor reinsertion and one solution to the problem can be found by lowering the relay sensitivity at the expense of reducing its limits of applicability [5].

This paper documents an EMTP investigation of the problem. A detailed EMTP model of the 500-kV line, series capacitors and surrounding network is created. The statistical switching feature of EMTP is used to determine the maximum change in superimposed voltage caused by a series capacitor insertion and the minimum change in superimposed voltage caused by an internal fault. A simple EMTP model of the new relay is created and simulations indicate a raised protection setting is possible. COMTRADE files of the worst cases were created and played back into a spare relay. It was found that a new secure setting could not be found. The paper proposes an alternative protection algorithm, which is extensively tested by off-line relay tests.

II. RELAY TEST SETUP

A number of different technologies and techniques are available to test a relay [6]-[7]. The technique chosen in this investigation is to simulate the network given in Fig. 1 in great detail using EMTP. The simulation data is then converted into COMTRADE format, read by a Real Time Playback (RTP) recorder [7], amplified and fed directly into a spare set of test relays. Each end of line D602F is tested by playing back separately their own bus end recordings. End-to-end testing using the RTP's GPS functionality was deemed not necessary.

III. EMTP MODEL OF RELAY

The algorithm used by the directional comparison relay is very different from conventional impedance relays [5]. As shown in Fig. 2, the relay calculates a superimposed voltage and current signal. A definite relation exists between the superimposed voltage and current:

- for a forward fault in phase *a* or *b*, ΔV_{ab} $\angle$-θ and ΔI_{ab} are of opposite polarity.
- for a reverse fault in phase *a* or *b*, ΔV_{ab} $\angle$-θ and ΔI_{ab} are of the same polarity.

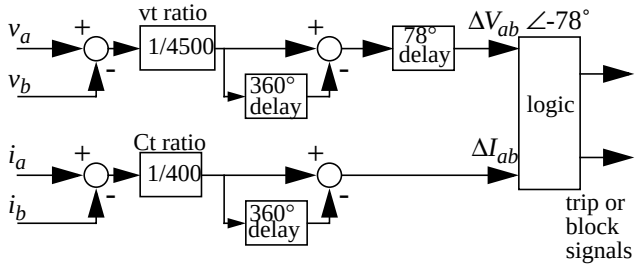

Fig. 2. Derivation of superimposed voltage and current signals.

The protection operates as a permissive overreach scheme. All faults causing a current change greater than 20% of nominal and a voltage change greater than a voltage setting (2 V) are detected within 6-8 ms. If the remote end also detects a forward fault, the line will trip once a permissive trip signal is received (20 ms communication time).

The EMTP model assumes no filtering of the input and output signals. An ideal voltage transformer (vt) and current transformer (Ct) is assumed in Fig. 2. The effect of more detailed instrument transformer models is discussed later in the paper.

IV. SENSITIVITY TO CT AND CCVT MODELS

Detailed models of the 500-kV current transformer (Ct) and coupling capacitor voltage transformer (ccvt) were developed. The purpose was to determine if the SD relay is immune to Ct saturation effects and ccvt subsidence transients.

Data for the 500-kV ccvt is published in [8]. However, the series reactor and main capacitor values do not appear to be correct because there is a phase shift between the input and output voltages. The data from [10] is used instead. A 42 H series inductor (L_c) is typical of ccvts used in 115 kV to 345 kV circuits [9]. The main capacitors (C_1 and C_2) are calculated by solving the following two equations:

$$C_1 + C_2 = \frac{1}{\omega^2 L_c} \tag{1}$$

$$C_1 = (C_1 + C_2)\frac{V_2}{V_1} \tag{2}$$

The tap ratio of the intermediate transformer is adjusted until the desired 4500:1 ratio is achieved. A 200 VA burden is modelled using data from CSA standard CAN3-C13.1-M79. Fig. 3 shows the layout of the ccvt.

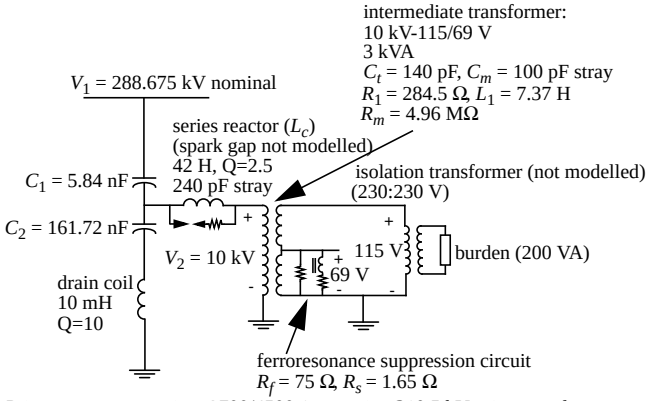

Fig. 3. 500-kV ccvt model.

Current transformer data is taken from [8]. The 8 ohm (B-8) burden determines the voltage across the saturable reactor. In order to match the transients that result during zero voltage faults [8], an additional point was added to the saturation data corresponding to an air-core reactance of one times the leakage reactance. Fig. 4 shows a single line diagram of the Ct model.

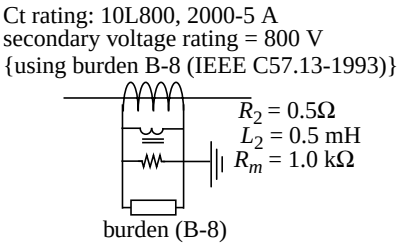

Fig. 4. 500-kV Ct model.

The performance of the Ct and ccvt models were compared against zero voltage and peak voltage faults, series capacitor reinsertion and ccvt secondary faults. The worst case Ct and ccvt transients result from zero voltage faults.

Fig. 5 compares the transients following a zero voltage fault as recorded by an ideal Ct and ccvt and by the actual device models. The large dc offset in current following a zero voltage fault results in Ct saturation, which is not modelled by an ideal Ct. The first half-cycle of current (ΔI_{ab}) seen by the SD relay, however, is nearly identical in the two cases. Subsidence transients in the ccvt are also the worst following a zero voltage fault. The superimposed

voltage seen by the SD relay is nearly identical in the two cases.

During the first 1/2 cycle following a zero voltage fault, an ideal device model is sufficiently accurate. Less than a 1 ms delay in operating time resulted when Fig. 5b was played back into the relay. Other disturbances do not cause a noticeable deviation in measured voltages and currents.

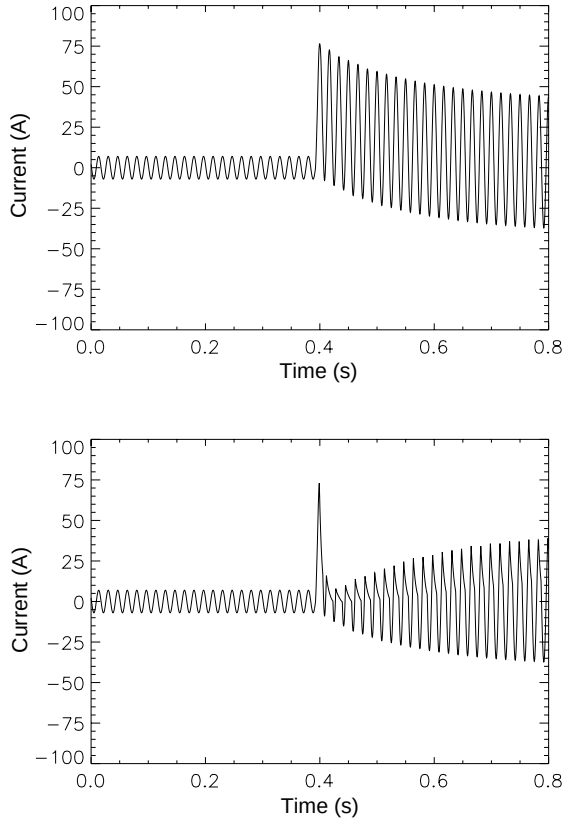

Fig. 5. Comparison of Dorsey zero-voltage line-side fault, (a) ideal Ct, (b) saturable Ct model.

V. D602F PROTECTION STUDY

The purpose of the EMTP study is to determine the maximum change in system voltage caused by series capacitor reinsertion and the minimum voltage caused by an internal D602F fault as seen by the new SD relay at Dorsey. If it can be shown that there is enough separation in voltage between the two events, it may be possible to recommend a new protection setting for the SD relay. Otherwise, new protection algorithms may be required.

Series Capacitor Energization Tests

One bank of series capacitors on D602F is test energized at eight different powerflow conditions. The minimum and maximum superimposed voltages determined from statistical energization of the series capacitors are summarized in Fig. 6. The magnitude of superimposed voltage transient following insertion of a series capacitor is directly proportional to the current flow on D602F. Also shown in Fig. 6 are the two false trip events mentioned earlier (i.e. labelled #1 and #2). A good correlation exists between the model and field observations.

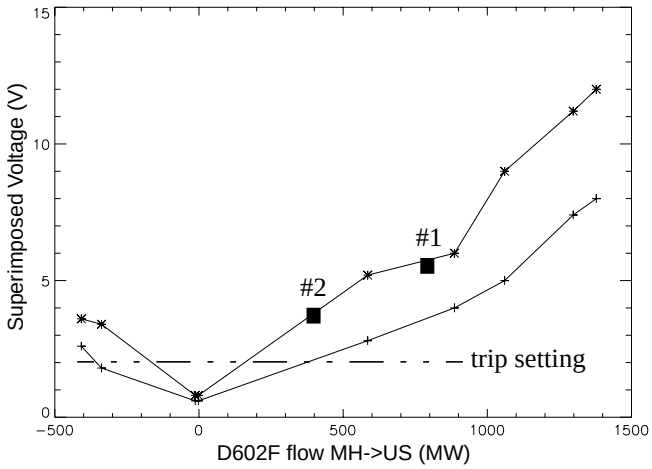

Fig. 6. Series capacitor energization tests. No SVC.

For all cases shown in Fig. 6, the Forbes SVC was disabled.

The worst case change in superimposed voltage occurs at maximum permissible current flow with a prior outage of one of the two series capacitors on D602F. Based on operating studies, the maximum permissible D602F flow is 1400 MW. Inserting the second series capacitor during this prior condition results in a 12 V change in superimposed voltage with no SVC or 15 V with a step change of 55 MVAr in SVC output. Fig. 7 compares the expected transients.

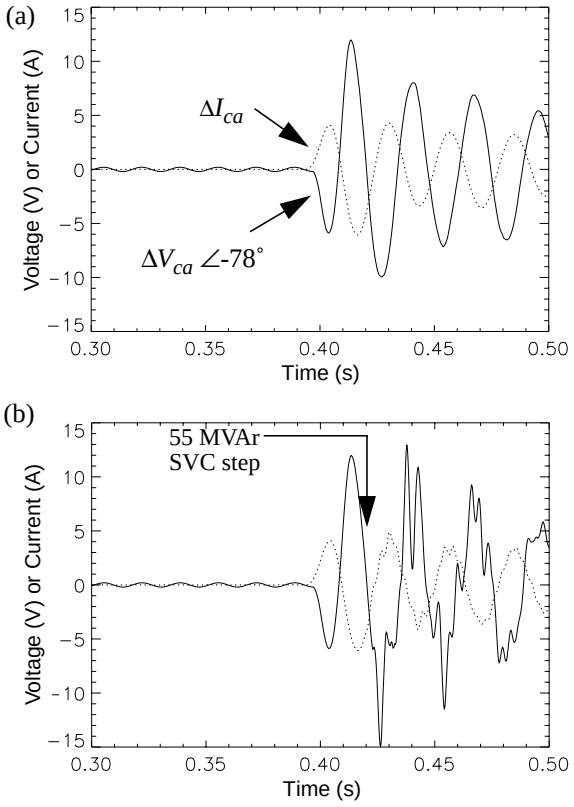

Fig. 7. Series capacitor energization tests at 1400 MW flow on D602F, (a) without SVC, (b) with SVC.

A 150 Hz transient voltage following the insertion of a 55 MVAr thyristor switched capacitor (TSC) may occur. The probability of the TSC switching depends on the voltage reference setting at the time the series capacitors are inserted. A slow susceptance control modifies the SVC's voltage reference setting in order to maintain zero MVAr output.

The SD relay does filter the input signals; however, the filter specifications are unknown. It is assumed that low pass filtering is used such that transient frequencies greater than 780 Hz can be ignored. Series capacitor bypassing will generate 13th harmonics, for example. However, filtering may not remove the 150 Hz TSC switching transient.

Fault tests

The maximum and minimum superimposed voltages were recorded for several fault locations and for three fault types; single phase normal impedance (0.01 Ω), single phase high impedance (50 Ω) and three phase normal impedance (0.01 Ω). The superimposed voltage is a function of the fault location, fault type and point-on-wave of fault initiation. The power flow on D602F did not significantly affect the recorded minimum and maximum voltages. Fig. 8 shows the expected range of superimposed voltage recorded at Dorsey for a single-phase high-impedance fault as a function of fault location.

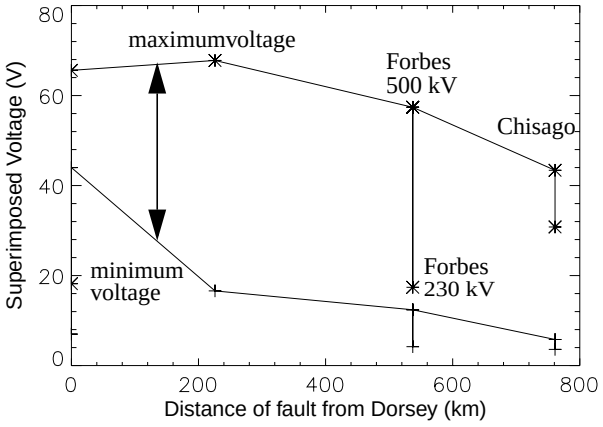

Fig. 8. Expected range of voltages for a 1 phase 50 Ω fault.

The minimum superimposed voltage that the SD relay should be able to detect is a high impedance single line-to-ground fault at the Forbes 500-kV bus. Fig. 9 shows the superimposed voltages and currents expected for this remote high impedance fault.

In order to detect all internal faults on line D602F, the SD protection setting needs to be set to 14 V according to the EMTP model. If the Forbes SVC does not operate, the 14 V setting will be high enough to avoid detecting series capacitor insertions. Switching of a 55 MVAr TSC step following insertion of the series capacitor at high D602F flow conditions may still cause a false trip of the SD relay.

Off-line relay tests investigated the sensitivity of the relay to these two cases. A minimum 8 V setting is required to detect the remote-end high impedance fault, while a minimum 13 V setting is required to avoid false tripping during capacitor reinsertion.

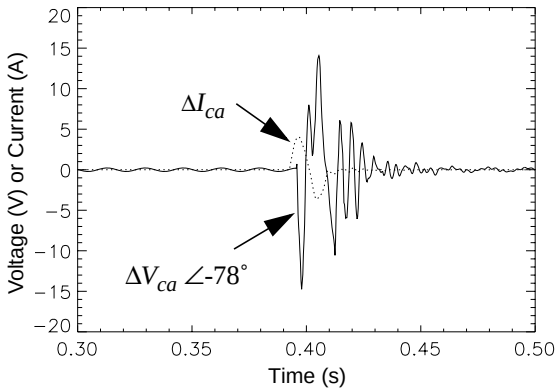

Fig. 9. Single phase remote 50 ohm fault.

Since a setting that works in both cases could not be found, an alternative protection algorithm is required.

VI. PROTECTION MODIFICATIONS

The proposed SD protection setting of 14 V is not secure for all disturbances as mentioned in the previous section. By raising the setting, the speed of the relay is reduced. An alternative technique would be to use a conventional impedance based relay to discriminate between series capacitor reinsertion and faults.

Fig. 10 shows the expected behaviour of the positive sequence impedance for the following five disturbances: series capacitor insertion, single-phase normal and high impedance faults and three-phase normal and high impedance faults.

The positive sequence impedance is calculated by first extracting the fundamental frequency voltage and current using a sliding window discrete Fourier transform. The fundamental frequency components of each phase are converted to sequence components using Fortescue's transformation.

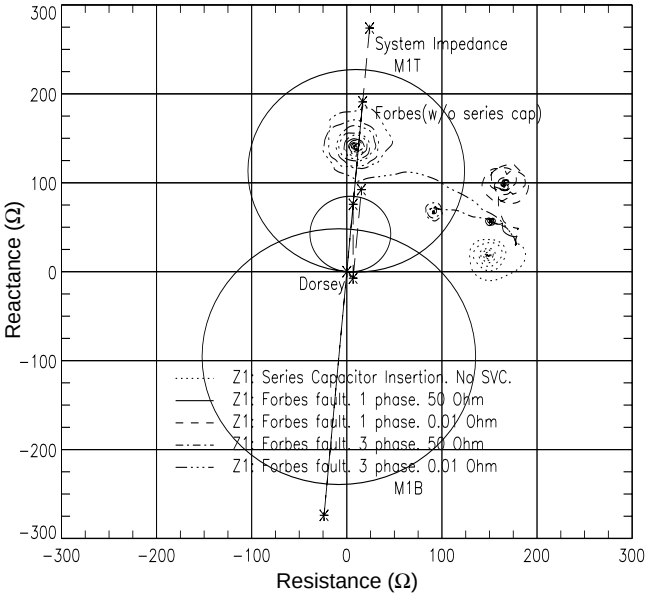

Fig. 10. Comparison of positive sequence impedance trajectories for various disturbances.

By examining Fig. 10, it is clear that the zone 2 Mho circle (M1T) can be used to differentiate three-phase faults from insertion of the series capacitor. However, single-phase faults are more difficult to distinguish.

A standard technique used in impedance based relays for determining the presence of unbalanced faults is to monitor the percentage of negative sequence current. The ratio of negative to positive sequence current is calculated for several typical disturbances and summarized in Table 1.

Single phase faults can be differentiated from series capacitor insertion by monitoring the percentage or absolute value of negative sequence current.

Table 1: Tabulation of Maximum Sequence Current

	series cap. insertion	series cap. insertion (breaker fail)	SLGF .01 Ω	SLGF 50 Ω	Three Phase fault .01 Ω	Three Phase fault 50 Ω
i_2(A)	181.5	200.6	896.7	532.7	478.4	205.1
i_1(A)	2277	2399	1972	2473	2480	2389
i_2/i_1 (%)	8	8.4	46	21.5	19.3	8.5

The relay system can be modified by including logic to determine if the fault is in zone 2 or the percent negative sequence current is greater than 15%. If such conditions have occurred, the SD relay is enabled to trip the line. The original 2 V trip setting may then be retained.

Fig. 11 indicates how the relay logic is modified. A spare set of memory polarized impedance relays (ZM relay) is used to provide the negative sequence and zone 2 supervisory inputs to the SD relay. A negative sequence current level detector was chosen because it was available in the ZM relay.

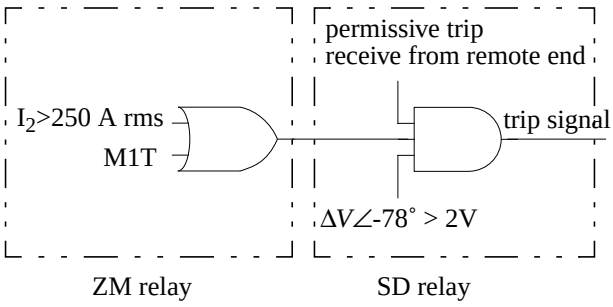

Fig. 11. Relay logic modifications.

Off-line tests showed no additional delays in fault detection times occurred as a result of the modifications.

On November 28, 2000, the proposed modifications were made to the digital directional comparison relay. Successful insertion of the series capacitors under 800 MW load was confirmed by field test.

VII. CONCLUSIONS

This paper summarized an EMTP investigation into the false operation of a digital superimposed directional comparison relay. A raised protection setting did not provided adequate security. Therefore, a modified protection algorithm is developed that supervises the SD relay trip signal with negative sequence current and positive sequence impedance location. Both off-line tests using a Real time Playback recorder and field tests have confirmed secure operation of the modified protection algorithm.

Detailed models of the Ct and ccvt were found, in general, not necessary to represent the expected transients at the input to the SD relay.

VIII. REFERENCES

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