Interpolation and reinitialization for the simulation of power electronic circuits

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Abstract **– This paper presents a new interpolation-reinitialization method for transient simulations in both forced commutation and natural commutation conditions occurring in power electronic circuits. Recently published methods in this field are also discussed.**

Keywords – transients, power electronics, EMTP, interpolation, reinitialization

I. INTRODUCTION

Recent developments in power systems, particularly in the application of power electronics, require the power system simulation tools be adapted to the specific behavior of these devices. The most common approach for detailed simulation of transients in power systems uses a fixed integration time-step with the trapezoidal integration method. This provides acceptable precision when the integration time-step is correctly selected according to system time constants. Problems arise with the introduction of natural and forced commutated devices. Although implementing Backward Euler integration in trapezoidal integration [1][2] or applying interpolation at discontinuity points, removes numerical oscillations and simplifies switching device modeling by eliminating the conventional numerical snubbers, the fixed integration time-step remains an important drawback. If the simulation method cannot account for the possibility of firing and extinction between two discrete simulation points, errors occur, non-characteristic harmonics are generated and abnormal operating modes appear. One corrective measure is to decrease the integration time-step at the expense of much longer computation time. This can increase the precision in most cases, but does not resolve the issue of simultaneous switching. The difficulty is that a variable time-step problem is being solved with a fixed time-step and ideal or linear switching device models. The fixed time-step remains a requirement to avoid unaffordable long computer execution times in addition to significantly increased complexity in device model programming. Moreover, at the power system analysis level, it is not necessary to model the switching devices with great detail since it has no significant impact on power system behavior.

Recent promising work [3]-[6] in this field is based on using interpolation and/or reinitialization techniques. The distinctive points of such techniques are reinitialization, interpolation for numerical oscillations and ability to solve both forced commutation and natural commutation conditions.

In addition to discussing previously available methods, this paper presents a new method, capable to interpolate and reinitialize to account for both forced and natural commutation conditions.

II. SOLUTION METHODS

Power semiconductor switches, typically diodes, thyristors, GTOs and IGBTs can be simulated using a number of techniques, in increasing order of complexity and increasing simulation time: ideal switches, non-ideal switches and physical models. The non-ideal switches are created by adding basic elements (resistors, capacitors, inductors and sources) in parallel and in series with ideal switches. The physical models are micromodels of the appropriate semiconductor technology, but they are not practical at the converter circuit and system levels. Power system simulators can provide acceptable results using the ideal and non-ideal switch models. Ideal means infinite resistance when open and zero resistance when closed. It is not recommended to apply very large and very small resistances, since this introduces conditioning problems in the solved system matrix and levels the integration time-step.

A. The problem of numerical oscillations

The change of status of an ideal switch can create voltage and/or current discontinuities. An important drawback of the trapezoidal integration method is its oscillating behavior following a discontinuity. It can be easily illustrated for the case of a transformer inductance being switched off in a converter circuit. At a given time-point the inductance current is given by:

$$i_{L_t} = \frac{\Delta t}{2L} v_{L_t} + \frac{\Delta t}{2L} v_{L_{t-\Delta t}} + i_{L_{t-\Delta t}} \quad (1)$$

If switch opening is detected at time-point t:

$$v_{L_{t+\Delta t}} = -v_{L_t} - \frac{2L}{\Delta t} i_{L_t} \quad (2)$$

Since $i_{L_{t+\Delta t}} = 0$ the next time-point solution gives:

$$v_{L_{t+2\Delta t}} = -v_{L_{t+\Delta t}} \quad (3)$$

and the oscillating condition is established. Numerical oscillations can be eliminated [1][2] using two halved time-step Backward-Euler integrations when a discontinuity is detected at time t so that:

$$v_{L_{t+\Delta t/2}} = -\frac{2L}{\Delta t} i_{L_t} \qquad (4)$$

and since $i_{L_{t+\Delta t/2}} = 0$, $v_{L_{t+\Delta t}} = 0$.

Another possibility is to apply interpolation [3] for voltages between time-points $t+\Delta t$ and $t+2\Delta t$. According to equation (3) this will result into $v_{L_{t+3\Delta t/2}} = 0$.

In both of the above approaches there is a problem on the significance of the intermediate solution. This can be illustrated using the circuit of Fig. 1. If the switch is forced to become open, then an impulse voltage will result on the inductance and the diode will turn on. If the Backward Euler method is used and if the intermediate solution in (4) is neglected, it will simply eliminate the impulse and the diode will not turn on. This problem has been demonstrated in [7] and recognized in [1]. A possible compensation for this problem is to account for the intermediate computation step [1]. But it is not simple to derive a rule for distinguishing between true and false impulse conditions. Indeed for the natural commutation case, the resulting impulse is only numeric (since the switch opens at current crossing zero) and should be discarded. There is also the possible simultaneous (within the same time-step) occurrence of true and false impulses in separate circuit sections, which may require using complicated topological recognition.

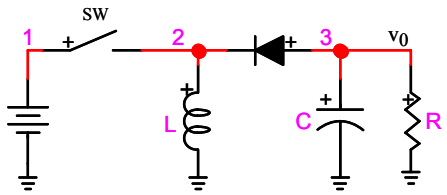

Fig. 1 Converter circuit used to demonstrate switching problems

The circuit of Fig. 1 also needs a simultaneous solution: the diode must operate simultaneously with the switch. If, for example, the diode opening is delayed after the switch closing, then the dc voltage will be forced onto the capacitor and the solution will become totally wrong. Using manual switch dependence is useless since the same circuit may enter a discontinuous mode. A simple solution to the simultaneous switching problem is to restart the circuit solution without advancing in time until all switches have settled. This will not cover for switching occurring within a time-step.

More precision can be achieved by accounting through interpolation for the actual switching time within a time-step.

B. Interpolation techniques

The distinctive features of applied techniques are reinitialization, elimination of numerical oscillations and the ability to solve both forced commutation and natural commutation conditions. The scope of this paper is on non-real time simulators.

The following presentations are based on method descriptions found in scientific publications. In some cases a method may appear straightforward, but there could be several unrevealed details in the actual implementation and some assumptions must be made in independent prototyping and testing.

The proposed approach for visualizing an interpolation technique is to present the switching device current (i_{SW}) trajectory in conjunction with the various solution time-points. The algorithm should be able to solve equally well the forced and natural commutation conditions. A diagram for the forced turn-off (GTO, for example) case is shown in Fig. 2. A solution is normally taken from the time-point t to $t+\Delta t$. A discontinuity due to turn-off is encountered when moving to $t+2\Delta t$. The difference with a thyristor is that the current between points 0 and 1 cannot be assumed to be linear (shown by the dashed line). If the solved system at each time-point is expressed through generic nodal analysis ($\mathbf{YV} = \mathbf{I}$) then an interpolated solution can be found at t_{d-}. The following steps are related to the employed algorithm. The dotted vertical lines are used here to denote the original time-mesh. The blue vertical lines are for distinguishing the time-mesh related to t_d and the red vertical lines are extra time-mesh lines required in a given algorithm.

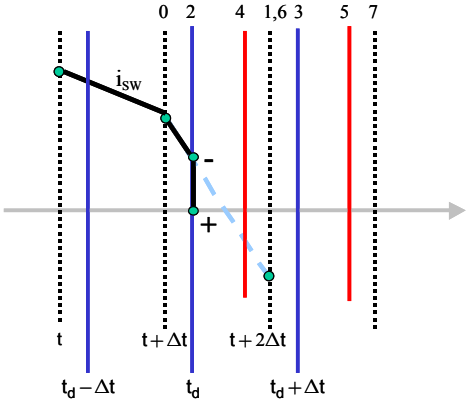

Fig. 2 Current trajectory and interpolation for forced turn-off

The method proposed in [4] corrects the limitations of its previous version [3] (limited to natural commutation problems) by performing two solutions at t_d, one at t_{d-} with the switch closed ($\mathbf{Y}^-$) and one at t_{d+} with the switch open ($\mathbf{Y}^+$). The solution then moves to time-point 3. An extra interpolation is performed at 4 for eliminating numerical oscillations. The action and drawback of this interpolation have been explained in the previous subsection on numerical oscillations. The following solution is found Δt apart at the time-point 5. An optional extra interpolation can be taken at the time-point 1 to move back onto the original time-mesh.

For the solution at t_{d+} it is assumed that $\mathbf{I}^+$ is equal to the interpolated $\mathbf{I}^-$. Although it may be acceptable in some practical cases within integration time-step limits, this assumption is questionable, since a discontinuity has occurred and the history leading to the solution at t_{d+} should be different from the history leading to the solution

at t_{d-}. There is no state variable continuity criterion.

The method proposed in [5] is a variant of [4] and limited to natural commutation problems. Contrary to [4] it has no treatment for numerical oscillations and numerical snubber (RC branch in parallel with the switching device) circuits become mandatory.

The algorithm presented in [6] is based on restarting trapezoidal integration with Backward Euler integration. The solution at t_{d-} is found again from interpolation. An extra halved time-step Backward Euler solution is taken from time-point 2 to an intermediate exploratory time-point $t_d + \Delta t/2$ using $\mathbf{Y}^+$:

$$i_{L_{t_d+\Delta t/2}} = \frac{\Delta t}{2L} v_{L_{t_d+\Delta t/2}} + i_{L_{t_{d-}}} \qquad (5)$$

It is known from theoretical considerations that the inductor currents and capacitor voltages cannot jump between t_{d-} and t_{d+}. Since the inductor current varies linearly, this algorithm takes back to t_{d+} the inductor voltage found at $t_d + \Delta t/2$: $v_{L_{t_{d+}}} = v_{L_{t_d+\Delta t/2}}$. For capacitors it is needed to take back current. The solution can then proceed to the next time-point using:

$$i_{L_{t_d+\Delta t}} = \frac{\Delta t}{2L} v_{L_{t_d+\Delta t}} + \frac{\Delta t}{2L} v_{L_{t_{d+}}} + i_{L_{t_{d+}}} \qquad (6)$$

where $i_{L_{t_{d+}}}$ is found from interpolation and $i_{L_{t_{d+}}} = i_{L_{t_{d-}}}$ which ensures state variable continuity. A similar equation can be written for the capacitor. An extra interpolation can be taken to resynchronize with the original time-mesh, but it is less important for non-real-time simulators. Numerical oscillations are automatically eliminated during the reinitialization procedure and due to Backward Euler usage.

The problem with the trapezoidal method shown in equation (1) for the inductance is that it carries a voltage term unrelated to the state variable. The extra term becomes problematic when a discontinuity is encountered. This is not the case with Backward Euler and that is why the reinitialization method of [6] can be supported mathematically. It also accounts for state variable continuity. Using Backward Euler for the entire simulation is not retainable since it truncates earlier in the Taylor series and is less precise.

C. *Proposed new method*

The method proposed in this paper follows the roots of the one in [6]. The method is illustrated in Fig. 3, which is showing in addition to the switch current a sample inductance current trajectory. A similar presentation can be made for capacitor voltage. The overall algorithm steps (corresponding to the shown vertical time lines) are:

1. Find the normal time-mesh solution at $t + 2\Delta t$ and detect that a discontinuity has occurred.
2. Find the interpolated solution for state variables at t_d and the new system matrix $\mathbf{Y}^+$.
3. Find the exploratory solution at $t_d + \Delta t/2$ using equation (5).
4. Extrapolate the solution for state variables at $t_d - \Delta t/2$. The extrapolated solution for i_L is:

$$i_{L_{t_d-\Delta t/2}} = 2 i_{L_{t_{d-}}} - i_{L_{t_d+\Delta t/2}} \qquad (7)$$

5. Move from the time-point of step 4 back to the time-point 2 using Backward Euler:

$$\hat{i}_{L_{t_d}} = \frac{\Delta t}{2L} v_{L_{t_{d+}}} + i_{L_{t_d-\Delta t/2}} \qquad (8)$$

6. Move from time-point 2 (t_d) to $t_d + \Delta t$ using the trapezoidal integration equation (6).

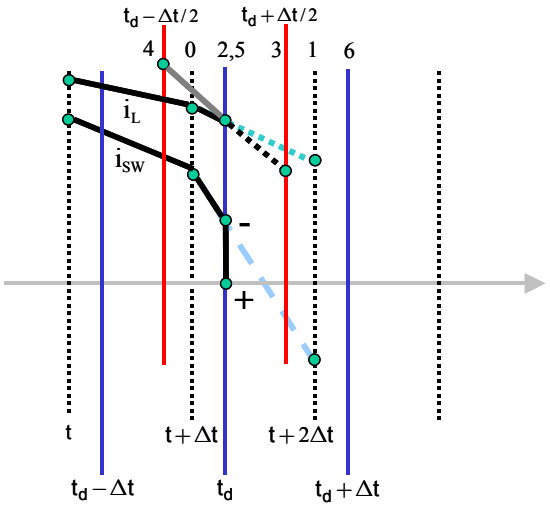

Fig. 3 New interpolation-extrapolation method

The inductance current is fixed by using $i_{L_{t_{d+}}} = i_{L_{t_{d-}}}$. The current found from (8) is discarded since this equation is only used for reinitilizing voltage. It is however expected that $\hat{i}_{L_{t_d}}$ is very close to the interpolated $i_{L_{t_{d-}}}$ when Δt is sufficiently small.

The main difference with [6] is that instead of assuming a zero slope voltage between t_d and $t_d + \Delta t/2$, a more realistic linear variation is taken into account by extrapolation. There is also an explicit method for finding the solution for all quantities at t_{d+}. The extrapolation is supported by the fact that linear variation must be assumed throughout the entire simulation within the main trapezoidal integration Δt in continuous conditions. Numerical oscillations are again automatically treated.

In the actual complete implementation of this method it is needed to account for multiple switching conditions occuring in the same time-step. The simultaneous switching case is accounted for by repeatedly testing switch status at t_d until all switch type devices are settled. As for non-simultaneous conditions it is a matter of applying multiple reinitializations within the same time-step.

III. TEST CASES

The new method is now demonstrated and compared with other methods by trying to match as closely as possible the related algorithms as explained in previous publications. All computed time-points are shown. Generally speaking, most methods will provide the correct same answer if the integration time-step is sufficiently small. In fact an almost theoretical solution can be achieved by applying extremely small time-steps. Some methods will accumulate numerical errors when the integration time-step is increased to decrease computer timings. The most difficult cases are encountered for very high switching frequency converters. Simultaneous switching is also a distinguishing competence.

A. First test case

The first test case is a simple load energization transient. The source side contains harmonics. The switch closing time is occurring at $t_d = 0.014444s$ (within a time-step). Fig. 4 presents energization results for a $\Delta t = 25\mu s$. Four methods are compared against the theoretical waveform for their reinitialization ability. Method 1 is the standard trapezoidal integration method switched into two halved time-step Backward Euler steps when a discontinuity is encountered. It does not have interpolation. Method 2 is based on the algorithm of [6]. Method 3 assumes that $\mathbf{I}^+ = \mathbf{I}^-$ and uses interpolation to eliminate numerical oscillations [4]. It is apparent from this figure that Methods 2 and 3 are able to reinitialize and come close to the initial voltage peak at switch closing time within the given time-step constraints. It is however only the New method that finds the best reinitialization for the state variables and is able to follow the theoretical solution correctly.

Fig. 5 shows the load inductance current waveforms at switch opening instant on current crossing zero. The New method is in almost perfect superposition with the theoretical solution. The interpolated opening time is not the same for all methods even with a decreased time-step of $10\mu s$. It is apparent here that interpolating to eliminate numerical oscillations is similar to Method 1 and creates an artificial insignificant or significant voltage peak. In this case it is insignificant.

B. Second test case

The second test case is simulating the converter of Fig. 1. It is a high frequency switching case where both current and voltage discontinuities are encountered. Circuit data is identical to the data used in [7] for both continuous and discontinuous operating modes.

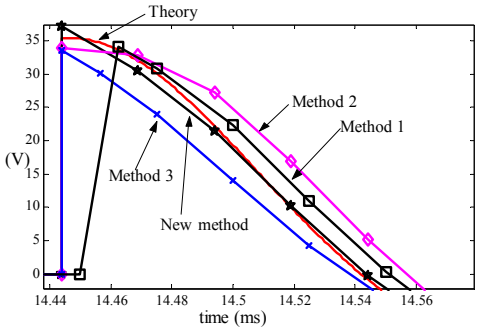

Fig. 4 Inductance voltage v_{24} ($\Delta t = 25\mu s$)

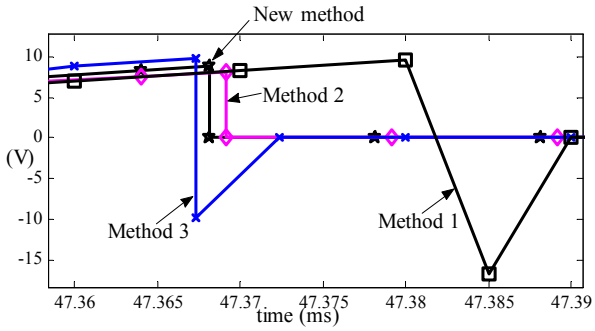

Fig. 5 Inductance voltage at switch opening

Fig. 6 ($\Delta t = 0.1\mu s$) shows the continuous operating mode output voltage v_0. The forced commutated switch is modeled as an ideal switch and the diode has a 0.7V turn-on voltage and becomes an open circuit when turned-off. The expected theoretical (from symbolic computations [7]) mean value voltage output is -24V. The simulation starts by initializing the capacitor voltage to its expected mean value voltage in order to achieve a faster steady-state. Method 1 is not shown here since it is unable to provide a simultaneous switching solution and will fail completely. It appears that due to the repetitive reinitialization and related errors, Methods 2 and 3 find a different steady-state. The actual mean value voltage found by the New method is -23.9875 (an error of 0.05%). Methods 2 and 3 find -24.315 and -23.365 respectively. The New method is also able to closely follow the theoretical envelope and the superposition makes both waveforms almost indistinguishable. If the time-step is increased to $1\mu s$ then the New method's error is only 4%. The apparent modulation effect of some methods is due to the initial transients and errors in reinitialization which cause errors in switching instants. It is impossible to achieve absolutely perfect steady-state, especially at such high frequencies, but the New method is the one that shows the best performance and enters steady-state much faster. Fig. 7 ($\Delta t = 0.1\mu s$) shows the inductance current. The theoretical minimum value is 9A. The New method finds 8.9958A. It is noticed here that Method 3 does not support current continuity.

The discontinuous mode of operation is more complex due to the increased number of reinitializations. Fig. 8 ($\Delta t = 0.1\mu s$) compares currents at switching point. The New method is very close to the theoretical solution.

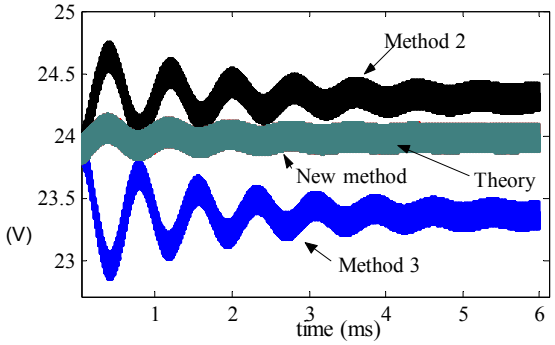

Fig. 6 Converter output voltage $-v_0$, continuous mode

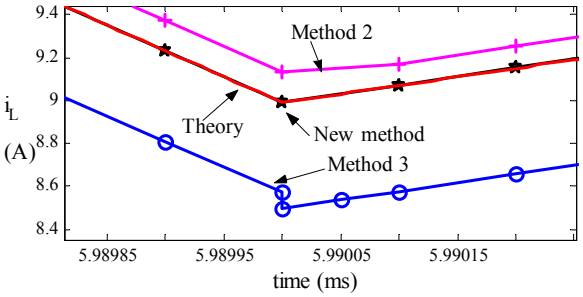

Fig. 7 Converter inductance current, continuous mode

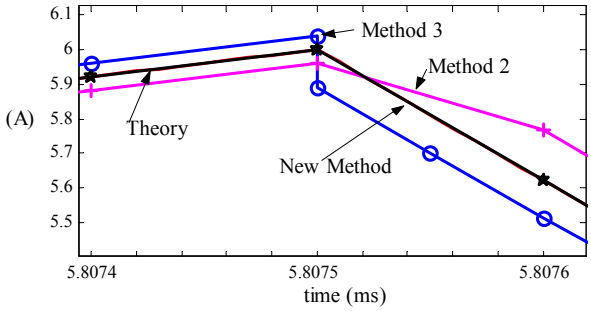

Fig. 8 Converter inductance current, discontinuous mode

C. *Third test case*

A simple diode bridge rectifier (Fig. 9) is used here to test for natural commutation. Diodes are modeled as ideal switches (0.7V turn-on). It is shown in Fig. 10 that Method 3 is less precise and noisy at the discontinuity time-point. Method 2 cannot provide a continuous transition due to the fact that both closely linked inductance voltage and capacitance current must be reinitialized at the same time-point. The New method offers the best performance. In the case of Method 1, its apparent precision is related to an averaging effect in the computation of the capacitor voltage and its other quantities remain noisy at the discontinuity treatment time-point.

D. *Fourth test case*

This test case is created to demonstrate the multiple simultaneous switching capabilities of the new method using the test circuit of Fig. 11. Fig. 12 demonstrates that the current is instantaneously switched over from IGBT1 (i_{G1}) to diode 3 (i_{D3}). When the current is reversed it is instantaneously switched from diode 3 to IGBT3 (i_{G3}). The IGBT currents i_{G1} and i_{G4}, and the diode currents i_{D2} and i_{D3} are perfectly superposed. The IGBTs and the diodes are modeled as ideal switches. The diodes conduct when the forward voltage drop exceeds 0.7V.

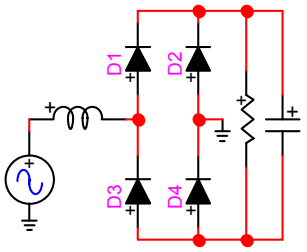

Fig. 9 Diode bridge rectifier

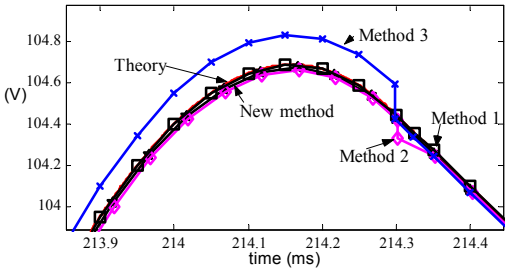

Fig. 10 Capacitor voltage (diode bridge rectifier)

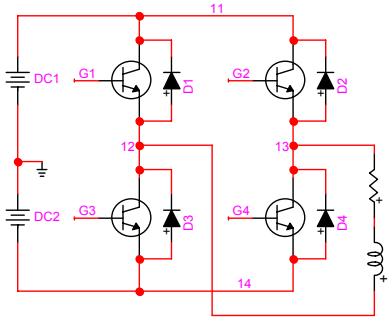

Fig. 11 PWM inverter

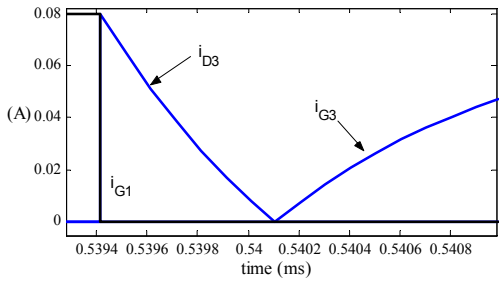

Fig. 12 IGBT and diode waveforms (New method)

Fig. 13 shows the results from the New method for unipolar voltage switching using $\Delta t = 10\mu s$. The almost perfect steady-state pattern demonstrates high precision. A very close match is also found using $20\mu s$ and $30\mu s$ time-steps.

It has been observed that one possible cure to Method 1

for detailed PWM simulation is its programming with simultaneous switching: the solution at a given time-point is restarted (not advanced to the next time-point) until no new switch status changes are found. Furthermore, the initial solution can be saved in waveform data to show an instantaneous transition. It is found that this approach (Method 1+) can provide acceptable results when sufficiently small time-steps are used.

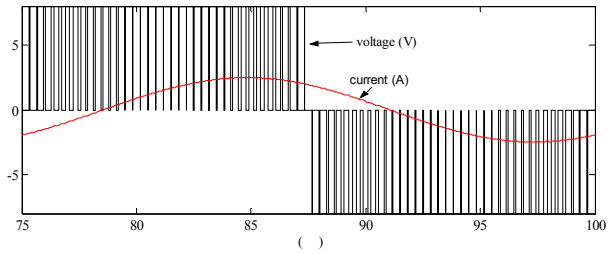

Fig. 13 PWM with unipolar voltage switching

E. Fifth test case

This test case is for simulating a simple 6-pulse dc converter (for a 250kV dc voltage) with equidistant firing scheme. The almost perfectly periodic dc waveform found by the New method using a $\Delta t = 50\mu s$, is shown in Fig. 14. Fig. 15 shows the same simulation using $\Delta t = 10\mu s$ in Method 1. In addition to being less precise, this method shows switching spikes related to current discontinuity. Better precision is achieved using the previously proposed Method 1+. It is remarkable that the New method, due to its interpolation scheme, is able to calculate more precisely using a larger time-step.

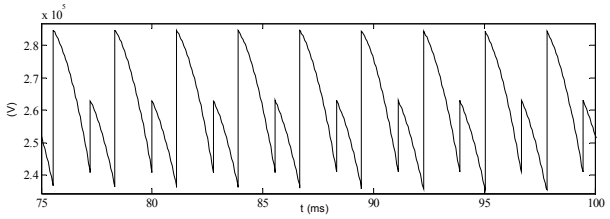

Fig. 14 6-pulse dc converter voltage (New method)

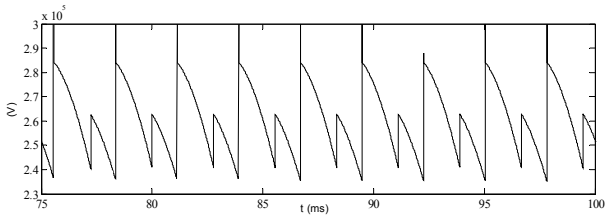

Fig. 15 6-pulse dc converter voltage (Method 1)

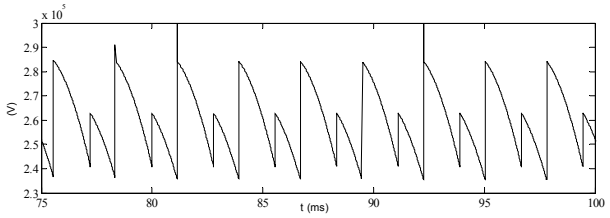

Fig. 16 6-pulse dc converter voltage (Method 1+)

IV. CONCLUSIONS

A new method for simulating discontinuous power electronic circuits has been proposed. The new method is based on reinitialization through interpolation and extrapolation. It is based on and theoretically supported by the assumption of linear variation of quantities within the main trapezoidal integration time-step during continuous conditions. The new method has been shown to provide superior results for the demonstrated cases: it is more precise and less sensitive to integration time-step increase.

With sufficiently small time-steps, most methods can achieve acceptable precision even without interpolation. The simultaneous switching condition and numerical oscillations can however remain problematic in some circuits. These considerations directed to an extra method (Method 1+) proposed in this paper. It is based on adding the simultaneous switching function to an existing technique for eliminating numerical oscillations. Although less precise, it can become a viable alternative and requires a significantly reduced programming effort.

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