Modelling of the back-to-back converter between Uruguay and Brazil in A.T.P.

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Abstract – The analysis of certain transients in power systems that include thyristor bridge converters, requires the inclusion of detailed models of the converter and its associated controls in the network under study.

In the case of the Rivera's Frequency Converter an ATP (Alternative Transients Program) back -to- back converter and associated controllers model has been developed. The same model was already used in the design and putting into service stages.

At the design stage, the model was validated by directly comparing their results with the results of an RTDS-type study (Real Time Digital Simulator) carried out by the Converter supplier.

Keywords – converter, ATP, modeling, valves.

I. INTRODUCTION

In February 2001 the first interconnection between , the Uruguayan and the Brazilian power systems was brought into service. The back to back converter station interconnects the Uruguayan network (150 kV, 50 Hz) and the Brazilian network (230 kV, 60 Hz) , with a maximum transferred power of 70 MW.

During the studies performed to design and to put the converter into operation, it was observed that it was not necessary to model in detail the converter and its associated controllers for certain types of electromagnetic transient studies (AC surge arresters selection, switching of filters and transformers , circuit breaker transient recovery voltages, etc.).

On the other hand, for other type of studies , (AC surge arresters selection, valve short circuit studies, etc.) to have a quite detailed model of the converter power circuit and the main components of the valves firing system was essential.

Finally, for a third type of transient study (behavior of the system when submitted to faults in the adjacent AC systems, with and without re-closing), the elaboration of a detail model of the converter's control system became necessary. Nevertheless working with simplified power circuit models was possible in such cases. In order to accomplish system studies like the above mentioned ones, the development of an ATP model for the converter station (Including both: the main components of the power circuit as well as their associated main control loops) was found to be necessary not only during the design and the putting into service stages but also during the system operation.

The main features of the model developed in ATP are described in this report along with a study carried out to validate the model at the design stage.

II. DESCRIPTION OF THE CONVERTER

Figure 1 shows a one line diagram of the back-to-back converter.

The transformers are of the 4 winding type, with rated voltages 150/15/9.8/9.8 kV, rated powers 75/70/46/46 MVA, connection group YNyny0d11 in the 50 Hz side and with rated voltages 230/15/9.8/9.8 kV ,rated powers 75/70/46/46 MVA, connection group YNyny0d11 in the 60 Hz side.

The 15 kV winding is used to connect the filters and the reactors (the latest are used for controlling the voltage rise at the 150 kV and 230 kV buses when switching in the filters).

An additional 15.5 MVAr filter is connected to the 150 kV, 50 Hz side. The filter in the 150 kV bus is a hi-pass one, with a cut-off frequency that correspond to the 11th harmonic for 50 Hz.

One of the filters (15.5 MVAr) in the 15 kV bus is of the C-type for the 3rd harmonic . The other two filters (15.5MVAr) in the 15 kV bus are of the same type, tuned to eliminate the 11th harmonic. There is also a capacitor of 10 MVAr in the 15 kV bus.

In the Brazilian side there are three identical filters (20.7 MVAR), each one having one branch tuned for the 11th harmonic (for 60 Hz), one C-type for the 3rd harmonic and a double-tuned one for the 13th and the 25th harmonic.

The DC rated voltage is 22.0 kV for maximal transferred power.

Each valve of the bridge is composed by seven thyristors in series connection.

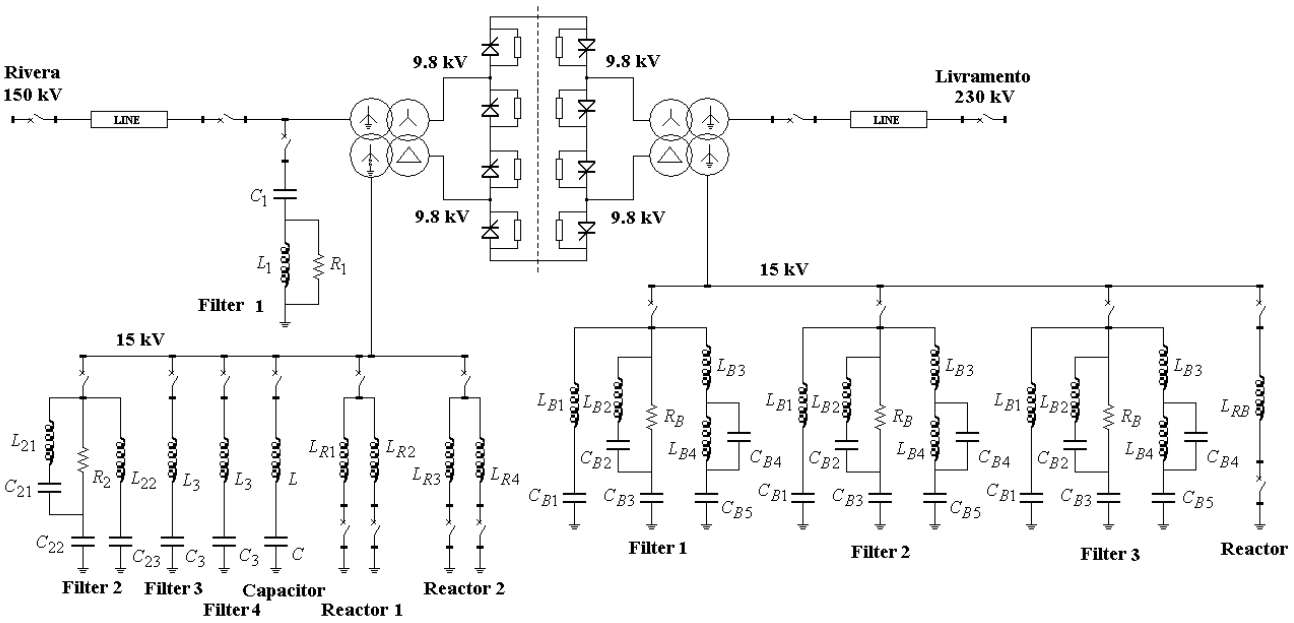

Fig. 1 One line diagram for the converter station

III. ATP MODELLING

The ATP (Alternative Transients Program), (a program developed for electromagnetic and electromechanic transients studies) , was used to develop the system and converter models.

The power systems were represented in detail in the converter's neighborhood and with a Thevenin equivalent at more distant busbars. These equivalents take into account the network frequency response through ladder-type passive circuits

A. Power Circuit

The converter power circuit was modeled by means of an equivalent thyristor for each one of the valves including the snubber circuits connected between its terminals (figure 2 shows the thyristor circuit).

Each thyristor was represented by a type 11 switch, controlled by TACS . The snubber circuits were represented by lumped parameters. In order to simplify the model an equivalent snubber circuit was represented for each valve and the nonlinear reactors were considered with constant inductance value.

The following values were assigned to the main parameters of the type 11 switch: VIG =420 V, IHOLD=1A and TDEION=0.3 ms .It has been found that these values have a relevant influence in the right performance of the converter model.

B. Thyristor firing scheme

Each side of the converter is a 12 pulses thyristor controlled bridge as can be seen in Figure 1.

To assure a correct operation, the thyristor firing system uses a "refresh system" which operates the following way:

a) Each thyristor of the bridge is on during 120° of the 360° cycle. Each 60° even an odd thyristors of each 6-pulse bridge are fired alternately one at a time**.**
Although each thyristor needs only a single shot pulse in the 360°cycle, a confirmation shot is applied to the thyristor that should continue conducting ,simultaneously with the "real" shot to the thyristor that enters now in the conducting stage.

a) Taking now into account the two six pulses bridges as a whole, the shots are generated each 30°, and another confirmation is made by generating a pulse for those thyristors that should remain conducting.

b) Each thyristor receives ,this way, 4 pulses in each 360° cycle: one for firing and three for confirmation. So that it is possible to have two thyristors in the upper bridge and two thyristors in the lower bridge with simultaneous shot orders.

C. Pulses Generation and ATP modelling

The pulses generation system is of the equidistant type, i.e a direct measure of the wanted firing angle is not taken.

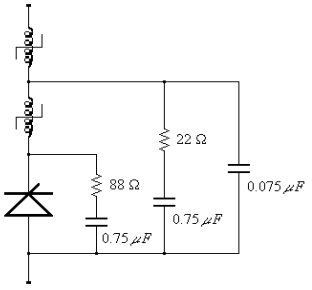

Fig.2 Thyristor electrical circuit

Figure 3 shows the block diagram of the electric circuit that generates the thyristors gate train pulses. This circuit has two input signals: BIAS and Error, the first is a constant value and the second is built from comparing the controlled variable value in the converter and the reference value. The different kinds of error signals utilized in all the control loops corresponding to different controlled variables are going to be presented below in item D.

If the error is zero the integrative block integrates the value BIAS, returning to zero when the tension –Vref is reached. Vref and BIAS are determined in such a way that T (time interval between two successive firings) corresponds to 30° in steady state conditions without error as shown in Figure 4.

If the error is not zero (for example the current of the DC-link is lower than the reference value) the integrator integrates the BIAS plus the error (see figure 4), arriving earlier to -Vref . So the pulses are then generated faster, the angle α diminishes , increasing the DC-link current and correcting the error.

The most important aspects of the ATP modelling of the train pulse generator are the following ones:

The controlled variable of the converter is passed to TACS as a source in order to build the error signal and it is added to the BIAS through Fortran expressions. After that it is integrated through a controlled integrator (device code = 58). The control signal is defined as OUT+VREF being OUT the output of the integrator.

When the output of the controlled integrator equals -VREF (integrator is set to zero), the corresponding instant of time is stored in a variable named T1REC as shown in Figure 5. In steady state conditions this variable is a staircase function for which each step is equal to T.

Each pulse is defined in TACS as a logical variable PULSE as follows:

IF (TIMEX.LE.(T1REC+ TEDE)) THEN
PULSE=1
ELSE
PULSE=0
ENDIF

where TEDE is the pulse width (25°), as shown in Figure 5.

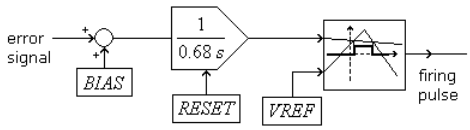

Fig.3 Block diagram

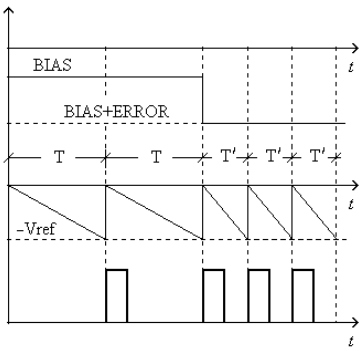

Fig.4 Firing pulses generation

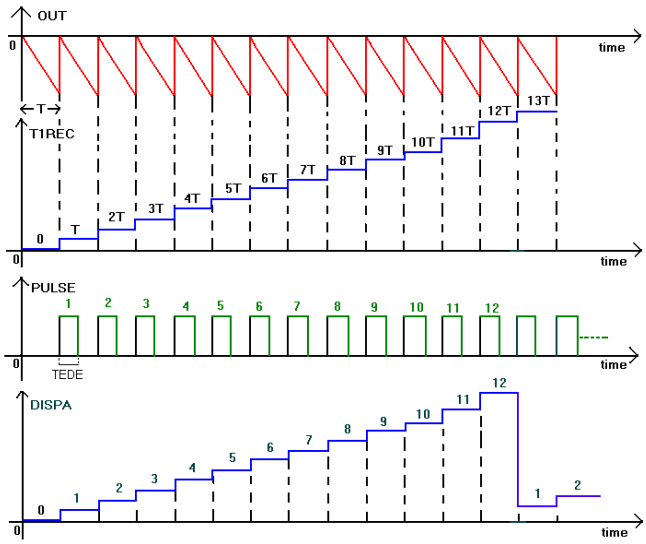

Fig.5 T1REC, PULSE and DISPA variables

Each pulse of the train generated this way , is assigned to a different thyristor through a variable named DISPA as shown in Figure 5.Once DISPA has reached the value 12 corresponding to the last thyristor to be fired it is again reset to its initial value again.

D. Control Loops

Figure 6 shows the eight control loops corresponding to each side of the converter.

The main loops are: loop 1 (DC-link current) for the rectifier and loop 2 (DC-link voltage) for the inverter. When the bridge works as a rectifier loop 2 is disabled, loop 3 (gamma minimum) prevents commutation failures in case the rectifier enters the inverter firing angle zone during a transient condition, and loop 7 limits the maximum DC-link voltage.

When the bridge works as an inverter loop 1 is used to force the system to follow the VDCOL-characteristic (see item E) , loop 6 (gamma of the other side bridge) is disabled and loop 7 fulfills the task of limiting the minimum DC-link voltage. Loops 4 (AC voltage), 5 (maximum alpha) and 8 (minimum alpha) are always active either in

rectifier or in inverter mode.

It should be pointed out that the loops have two different functions. Loops on the top of the diagram generate the firing train pulses while the loops at the bottom of the diagram enable the loops on the top to fire if they fulfil all the requirements. For instance: if the DC current in the link is below its reference setting point, loop 1 tries to generate train pulses faster, but this happens only if the firing angle is greater than alpha minimum (loop 8), so it is necessary to wait until this loop output reaches the logic 1.

The controlled integrators are set to zero all together with the output of the last AND logical gate.

The corresponding control loops and the logical gates which combine their outputs were carried out in TACS from the block diagrams shown in fig.6.

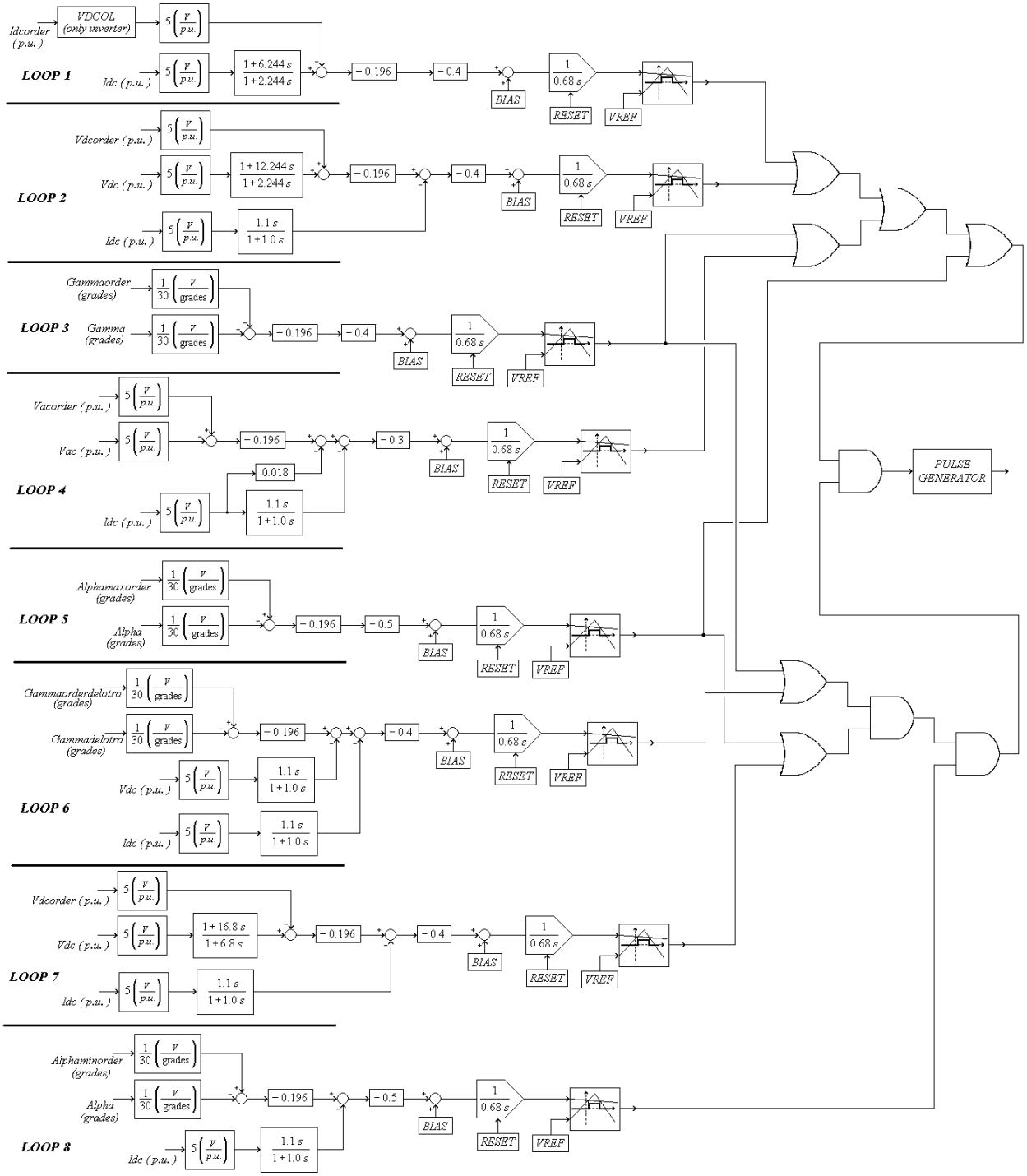

Fig.6 The eight control loops of the converter

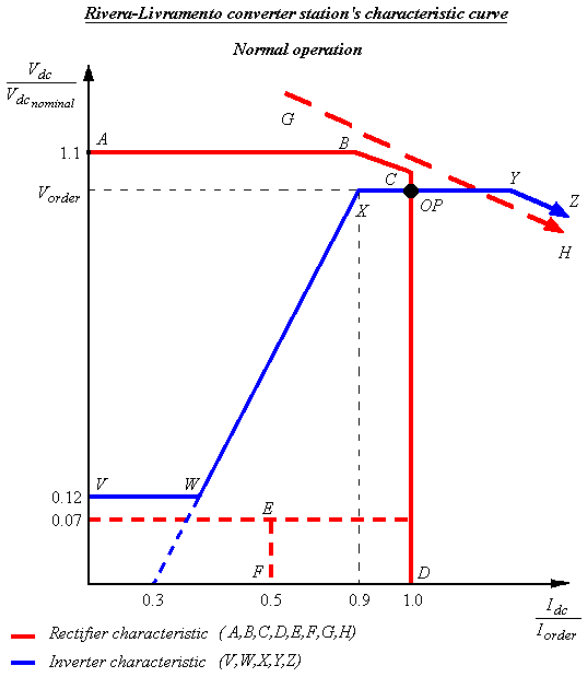

Fig.7 Static characteristic for the converter station.

E. The Static Characteristic

The control system operation is reflected in the so-called "static curve" (See figure 7). The interrelation between the rectifier and the inverter curve in this characteristic allows to observe the dynamic operation of the converter in a quasi-static way.

The different branches of the rectifier and inverter characteristic curves are directly related with the different control loops that are observed in the block diagram (figure 6). In this way, it is observed that the line AB corresponds to loop 7 of the rectifier (maximum DC voltage), the line BC corresponds to loop 8 of the rectifier (minimum alpha), the line CD corresponds to loop 1 (current reference) of the rectifier, the line GH corresponds to loop 6 (minimum-gamma of the other side bridge), the line VW corresponds to loop 7 (minimum DC voltage) of the inverter, the line WX corresponds to loop 1 (VDCOL characteristic) of the inverter, the line XY corresponds to loop 2 (DC voltage reference) of the inverter and the line YZ corresponds to loop 3 (minimum gamma) of the inverter.

In normal operation conditions, on the rectifier side the dominant block is the Idc one (loop 1), while on the inverter side the dominant block is the Vdc one (loop 2).

The remark must be made that the VDCOL characteristic in the inverter side allows to keep approximately the same reactive consumption during different transients.

IV. Study of Fault Application in the Rectifier Side. RTDS vs ATP Comparison

In order to evaluate the model behavior, the ATP simulation results using the described model were compared to those obtained by the converter supplier during the simulation of a disturbance in the net carried out by means of a RTDS (Real Digital Time Simulator). RTDS is a study tool that combines computational models of the adjacent AC networks and prototypes of the control equipment designed for the converter station .

It was considered a case in which Uruguay works as rectifier with a reference current (DC) of 2932.5 A and a reference voltage (DC) of 23.584 kV. In this case, with the converter transferring an active power of 69.16 MW, the following events sequence is simulated:

1) At 350 ms a three-phase fault involving earth is applied in the line Rivera - Tacuarembó at the Tacuarembó side.
2) At 450 ms the line opens (both sides).
3) At 700 ms the fault vanishes.
4) At 850 ms the line re-closes (both sides).

The Uruguayan system was modeled in detail from Rivera to Terra, including the generators in Terra, and an equivalent of the remaining AC network was added in the Terra 150 kV bus (figure 8 shows a one line diagram of the modeled Uruguayan system). In the Brazilian side a similar model was made up to Alegrete and Candiota busbars (figure 9 shows a one line diagram of the modeled Brazilian system).

An additional difficulty was found because there was no information about the exact instant of application of the fault with respect to the voltage wave form in the RTDS study.

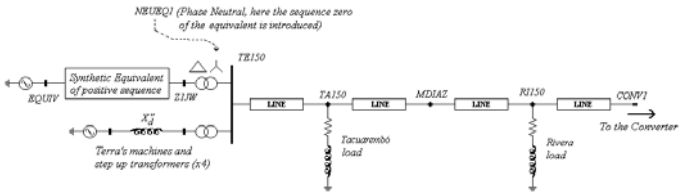

Fig. 8 One line diagram of the modeled Uruguayan system

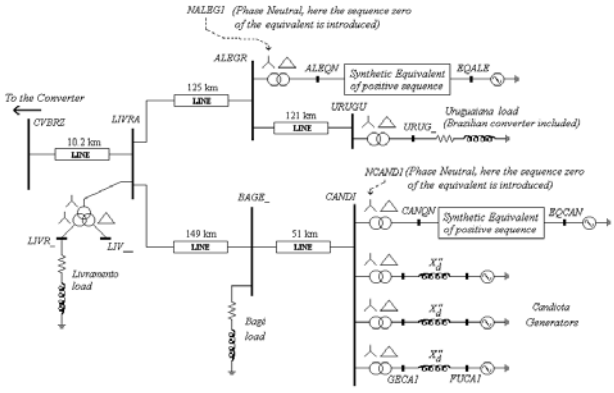

Fig. 9 One line diagram of the modeled Brazilian system

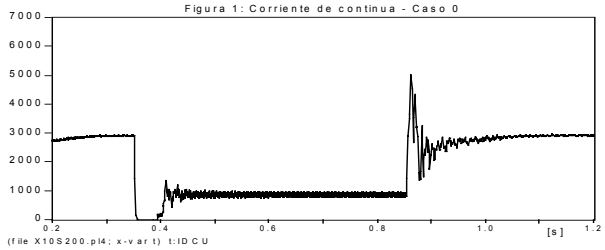

Fig. 10 DC current obtained from ATP model

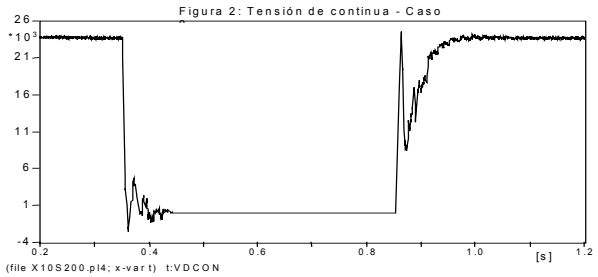

Fig. 11 DC voltage obtained from ATP model

Figures 10 and 11 show the ATP results of the DC and DC voltage.

Figure 12 shows the RTDS study results carried out by the Converter supplier.

The wave forms are very similar to those presented in figures 10 and 11.

In both set of results it can be observed that during the time there is not voltage in the rectifier side a natural by-pass pair happens, the current takes the approximate value of 880 A and the DC voltage takes a zero value. These results are compatible with the static characteristic of the converter (figure 7) , it is not possible, as it can be seen, to maintain the operation restriction of the VW line and the operation point is forced to lay in the current axis with Idc = 0.3 Iorder=0.3*2932.5 = 879.75 A

V. CONCLUSIONS

In the present work the main characteristics of the back-to-back converter station and its control system are described.

The models implemented in ATP were presented: adjacent AC power system, power circuit of the converter and its associated controls.

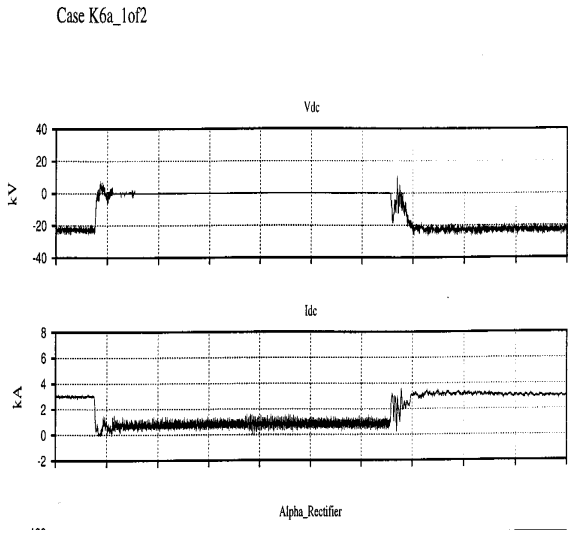

Fig. 12 Results obtained by the Converter supplier

The results obtained with the ATP model for a particular disturbance in the AC power systems and those obtained with RTDS by the converter supplier were shown.

Comparing both results it can be concluded that the model had very accurate results so becoming (from this and other studies) completely validated.

REFERENCES

[1] H.W. Dommel, “EMTP Theory Book”, Microtran Power System Analysis Corporation, Vancouver, Canada, 1992.

[2] E.W. Kimbark, “Direct Current Trasmission Vol. 1, John Wiley & Sons, 1971

[3] “Alternative Transients Program (ATP)- Rule Book”, Canadian/American EMTP User Group, 1987-92.

[4] J.D. Ainsworth , “The Phase-Locked Oscillator- A New Control System for Controlled Static Conver tors”, IEEE Vol. PAS-87, No 3, March 1968.

[5] J.D. Wheeler, C.C. Davidson, J.D.G. Williams and A.K. Roy, “Design Aspects of the Chandrapur 2x500 MW Back-to back HVDC Scheme”, CIGRE Session 1996.

[6] R.S. Whitehouse, “Protecting a HVDC Link against accidental isolation from its receiving AC System”, IEEE 92 SM 468-9 PWRD.