

Real-time simulation of induction motor IGBT drive on a PC-cluster

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Abstract – This paper presents a real-time motor drive simulator capable to accurately simulate a double IGBT bridge inverter connected to an induction motor through an interphase transformer. The simulator also includes a DC-link model with regeneration capability and two choppers. The paper will detail the implementation of the model and simulation results and timing. The whole system, with external I/O IGBT fiber optic gate signals, executes in real-time at 80 μ s time step under the RT-Lab real-time distributed simulation software on a PC-cluster composed of 3 Pentium processors running at 1 GHz. The same model, but this time with only one bridge and no interphase transformer, runs in real-time at 65 μ s time step.

Keywords – real-time simulation, hardware in the loop, time stamping, I/O, drives.

I. INTRODUCTION

Testing, integration and validation of complex controlled systems have been traditionally made in a systematic way consisting of analyzing the behavior of individual components, mostly by simulation, before complete integration on analog simulators or real apparatus. In several cases, the integration is directly made with prototypes of the real equipments. At this stage, real cautions were to be taken because of the power levels: a simple controller malfunction could damage the prototype or the real system and create project delays and cost increases. A more graduate testing/integration approach was needed to diminish the probability of damage and personal injuries and also to decrease total development costs and time to market.

With the increasing complexity and costs of projects, as well as the advances in computer science, it has become advantageous to make a more complete and gradual approach during the course of system integration. An excellent way to achieve that goal is to use Hardware-in-the-Loop (HIL) digital simulation. In HIL simulation, a device under test is run fully connected to a real-time simulated dynamic equivalent of an apparatus. Thus, if the apparatus equivalent is correctly modeled, the device under test will behave as if it was connected to the real apparatus. The devices under test, often a controller, can therefore be tested for a wide range of parameters without any risk to the main system.

Software package for the simulation of electrical circuits usually rely on intermediary routines that compute discrete time iteration equations of the circuit. This is done based on a nodal voltage approach like EMTP [5] or on the state-space formalism of the SimPowerSystem blockset (PSB) [4] for Simulink and ARTEMIS [2][3]. Those

approaches have the advantage of implicitly solving any causality problems that may lie in the network equations. Otherwise, if the network is simple enough and suffers from no causality problems, modeling can be done using individual integrators for each element of the networks.

In the case of a voltage source inverter driving an motor, the presence of a huge capacity in front of the bridge itself permits the decoupling of the inverter devices from any circuit *en amont* of the capacity, provided the capacitor voltage will not change much during a single time step. The DC-link-inverter-motor set-up then becomes simple enough to be computed directly from its individual differential equations, *without the use of EMTP or ARTEMIS type algorithms*.

An important consideration for the choice of HIL simulation is the minimum sampling time that can be achieved under realistic conditions. Even with GHz-speed processor technology, practical time step achievable by high-end HIL simulators like RT-LAB [1], RTDS [9] and HYPERSIM [10] rarely goes under 25 μ s for a variety of reasons, like the I/O access time and inter-processor communication latency. This performance limitation found in most high-end commercial real-time simulator available today may be acceptable for power network simulation that can be simulated with time step of about 50 μ s. However, a minimum time step as low as 25 μ s is not acceptable for some stringent simulation needs, like motor-IGBT-drive simulation. In this case, IGBT turn-on and turn-off time must be sampled precisely to ensure proper integration of the motor fluxes. For example, the train traction simulation application described in [6] required a 1 μ s switch timing resolution. The solution to this problem is found by sampling the I/O gate signals with high frequency counter cards and by inserting this timing information in the simulation process. The paper will describe an implementation of this solution to simulate a complex IGBT motor drive system used in large mining off-highway trucks.

II. PARALLEL IGBT BRIDGE MOTOR DRIVE MODEL

The simulator is aimed at the real-time simulation of one wheel motor drive of an off-highway vehicle used in mining facilities. The simulated model comprises two IGBT bridges connected to an interphase transformer that feeds the induction motor.

The IGBT bridges are fed by a DC-link composed of a capacitance and two choppers. A key parameter in the model is the value of the DC-link capacity that is large enough to assume that its voltage changes negligibly

during one step of simulation. The DC-link is modeled to be able to simulate over-voltage that can occur in regeneration mode, i.e. braking. When in the regeneration mode, the capacitor voltage of the DC-link is computed from the integration of bridges and choppers currents. Otherwise, the diode in the model sets the DC-link voltage to a user defined value. The complete model is detailed in Figure 1.

Bridge control is made from external fiber optic IGBT gate signals which are time stamped with NI6602 timer cards running at 20MHz. Measurements have shown that the card provides a ± 150 ns *effective* gate pulse timing resolution. This resolution allows for precise IGBT leg dead-time computation as well as accurate modeling of switching delays and voltage unbalances between bridges.

The model provides analog outputs of user selected model signals like machine currents and DC-link voltage as well as incremental speed sensor signals. The model is design in the Simulink software from The Mathworks inc. The integration algorithms are selected to be compatible with the Real-Time Workshop code generator and RT-LAB software since that the objective is to interconnect the real-time simulated plant model with actual IGBT control systems.

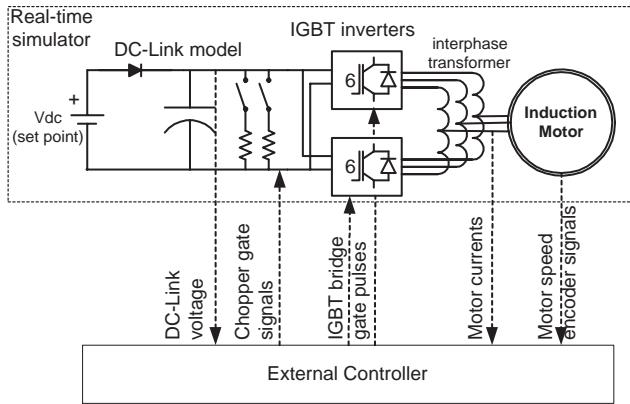


Figure 1 Real-time simulator model

A. Interphase transformer model

The interphase transformer (IPT) limits current spikes in the IGBTs in cases where there would be a mismatch between correspondent IGBTs rise-fall times or a controller-generated firing delay between them.

The current going through the IPT, and therefore though the corresponding IGBTs, is computed by integrating the voltage difference at the IPT terminals. Normally, if cousin IGBTs of both bridges turn on and off at the same time, the voltage at the IPT is null and only the motor current goes through the IPT, equally divided between both bridges. If a voltage is present at the IPT terminals then a current grows from one bridge terminal to the other. This current is superimposed on the motor current to compute each bridge current.

B. Motor model with IGBT gate time stamping

The induction motor is modeled in the Park domain with stationary reference frame:

$$\dot{\psi} = [R / L, \omega_r] \psi + V_s \quad (1)$$

The motor equations are discretized with the Euler-Cauchy method, a explicit second order method. As the motor fluxes do not change abruptly (states variables of a physical system are linked to the energy of the system and thus cannot be discontinuous), precise integration of the motor flux equation is highly dependent on the integration of the stator voltage V_s which toggles quasi-instantly between zero and the DC-link voltage depending on the IGBT conduction states.

The motor phase voltage integration is computed with the timestamp of the timer board. During each time step, each phase of the induction motor is connected to the positive voltage of the DC link (V^+) or else to ground (V^0).

For each time step, let the

t_{up} : time the upper IGBT of a branch is on.
The corresponding phase is connected to V^+ .

t_{low} : time the lower IGBT of a branch is on.
The corresponding phase is connected to V^0 .

t_{dt} : time both IGBTs are off. One anti-parallel diode connects the phase to V^0 or V^+ , depending on the phase current.

then the integrated stator voltage, at each phase, during each time step is:

$$\int_t^{t+h} V_s dt = V^+ * t_{up} + V^0 * (t_{low} + t_{dt}) \quad (2)$$

(for current entering the motor phase)

$$\int_t^{t+h} V_s dt = V^+ * (t_{up} + t_{dt}) + V^0 * t_{low} \quad (3)$$

(for current going out of the motor phase, i.e. causing the upper diode to turn ON)

C. Effect of IGBT firing pulse time stamp resolution

Precise determination of the IGBT turn on-off times is important for accurate simulation of the complete drive apparatus. Figure 2 shows the effects of the precision of the time stamp resolution on the simulated machine electrical torque when the simulation integration time step is set at 80 μ s. The figure shows that a 2 μ s time stamp resolution may be adequate for this off-highway vehicle applications with a PWM base frequency of 680 Hz. A time stamp resolution of 2 μ s produces a 0.2% non-characteristic torque ripple. A time stamp resolution of 5 μ s (curve g) produced a less acceptable ripple of about 1% at 60 Hz on the electrical torque. This ripple can initiate control instability or simply lead to false control performance evaluation. The question here is: "How to distinguish between a real problem caused a controller instability or a problem caused by the simulator?" Of course, the result without time stamp compensation

(bottom curve) is totally unacceptable. But again, non-experienced engineers may believe that an unstable controller causes this oscillation.

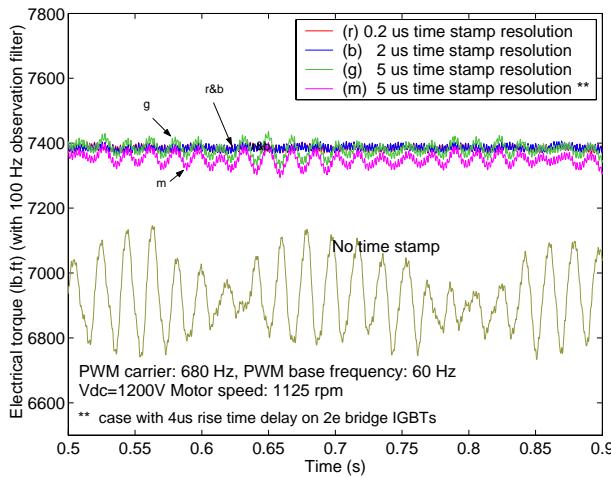


Figure 2 Effect of time step resolution on the torque

Table 1. Machine parameters

Inertia	12 lb.s ²
Stator leakage inductance	0.217 mH
Rotor leakage inductance	0.274 mH
Mutual inductance	8.617 mH
Stator resistance	9.3 mΩ
Rotor resistance	8.7 mΩ
Pair of poles	3

D. Real-time distributed simulation under RT-LAB

RT-LAB software[1] from OPAL-RT Technologies inc. enables real-time simulation of Simulink models on low-cost target PC clusters with QNX operating systems for maximum reliability. High-end single-, dual- or quad-Pentium processors boards are supported on each node of the PC clusters.

The IGBT induction motor drive model has been implemented in a PC-cluster configuration composed of 3 Pentium III processors running at 1 GHz. Two of those processors are installed on a dual-CPU computer with shared memory while the other one is connected through a fast FireWire 400 (Mbits/s) real-time link.

The first CPU of the dual-CPU unit computes the machine model, interphase transformer model and the time-stamp based voltages of the two IGBT bridges. The second CPU reads the IGBT gate signals from the I/O and outputs model variable values to D/A cards. The third CPU computes low-rate thermal models used to compute IGBT switching delays and machine winding resistance evolution. This processor can also be used to implement the control algorithm, if fully digital simulation is desired.

Figure 3 shows the hardware configuration of the RT-LAB Electrical Engineering Simulator used in this paper. It can be seen that the actual hardware controller is

connected to the simulator through fiber optic interface and National Instruments NI6602 timer cards.

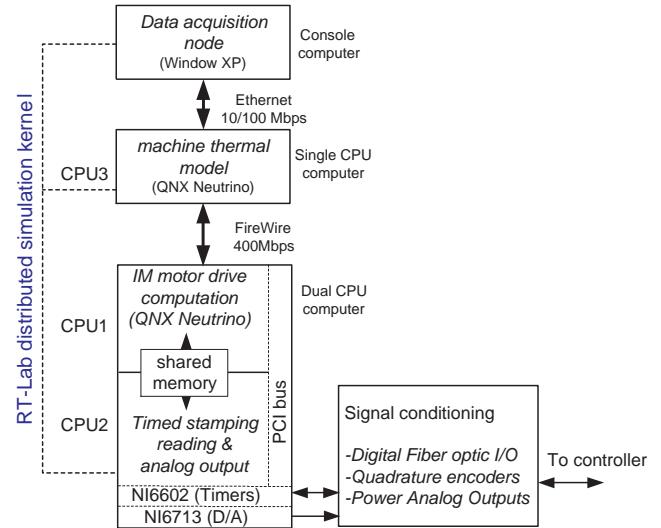


Figure 3 Hardware configuration of the RT-Lab simulator

III. VALIDATION OF SIMULATOR

The section presents validation tests made on the IGBT induction motor drive model. The tests are made on a induction motor with the characteristic listed in Table 1. *Hardware-in-the-loop* tests were conducted on the simulator with IGBT gate signals captured from the simulator's I/O. The gate signals are generated by a high-precision pulse generator implemented in hardware. Other tests were conducted off-line with RT-Events blockset [7] generated IGBT gate signals for accurate sub-usecond resolution of the switching events.

A. Test 1: Effect of Diode voltage drop and IGBT switching delays

The proposed IGBT bridge model can finely simulate the IGBTs and diodes voltages drops and switching delays. Figure 4 shows the effects on the simulated machine electrical torque of the bridges device voltage drops and switching delays. In the proposed model, the following parameters can be individually set for each device in each bridges:

- V_f, V_{ce} : voltages offset for IGBT and diode.
- R_{on} : ON resistances of IGBT and diodes
- T_{don} : IGBT turn on delay (fixed)
- T_r : IGBT turn on delay due to current rise in the device
- T_{doff} : IGBT turn off delay (fixed)
- T_F : IGBT turn off delay due current fall in the device
- T_{rr} : Anti-parallel diode turn off delay due to reverse recovery

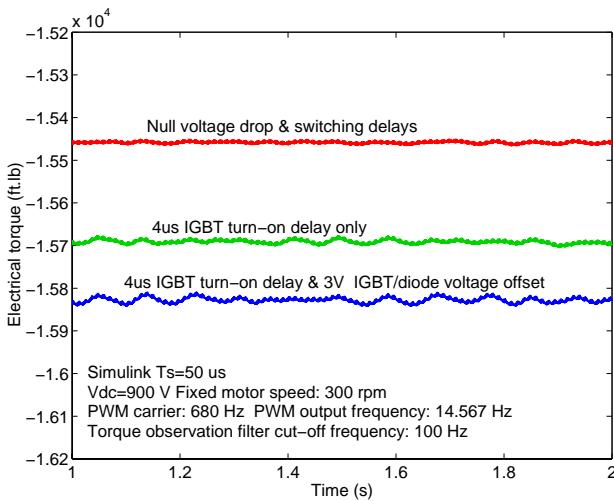


Figure 4 Influence of IGBT parameters on motor torque

It is important to point out that all simulation results of Figure 4 were made with a fixed time step of 50 μ s. These results demonstrate that the time stamped bridge algorithm is able to take in account switching delays that are a fraction of the time step.

B. Test 2: Effect on small bridge characteristic unbalances

An important aspect of the parallel IGBT bridge configuration is the current mismatch between bridges caused by difference in the IGBT voltages drop and switching delays. The IGBT bridge models are designed to take into account all individual IGBT and diode voltage drop, switching delays. The model also takes in account those parameters dependence on device currents.

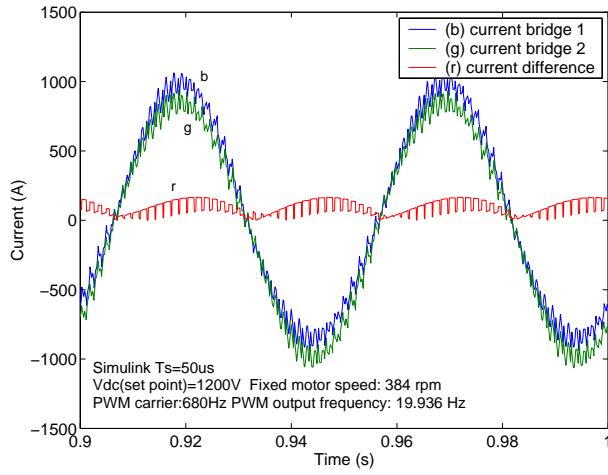


Figure 5 Bridge currents with unbalanced IGBT characteristics

This test was made off-line with PWM time stamped gate signals generated from within Simulink and is made to demonstrate the ability of the bridge model to take into account fine variation in individual IGBT characteristics. Those small unbalances cause abrupt voltage spikes at the interphase transformer terminal and cause currents imbalances into it.

Table 2 lists the switching devices parameters taken into account by the bridge model. The second bridge, for the current test, has its upper and lower IGBT/diode characteristics inversed (i.e. the cause of the imbalance).

Table 2 First bridge parameters

	Bridge No. 1 voltage drops and switching delays	
	Upper	Lower
Diode params		
V_f (V)	1.5	1.0
R_{on} ($m\Omega$)	1.5	1
T_{rr} (μ s)	1.0	1.0
I_{rr} (A) (at T_{rr})	1000	1000
IGBT params		
V_{ce} (V)	1.0	1.4
R_{on} ($m\Omega$)	1.5	2.1
T_{don} (μ s)	1.0	1.5
T_{doff} (μ s)	1.5	2.4
T_r (μ s)	0.5	2.5
I_r (A) (at T_r)	1000	1000
T_f (μ s)	0.5	2.0
I_f (A) (at T_f)	1000	1000

Figure 5 shows the simulation at 50 μ s, with time stamps, of the bridges currents for the bridges parameters listed in Table 1. The same model simulated the VisSim [8] simulation software at a 0.1 μ s time step (not shown) closely matched the 164A peak current difference between phases A of both bridges.

C. Test3: Hardware-in-the-loop: Square wave IGBT pattern generated from external controller

This test makes a one-bridge simulation with a square wave modulation of the induction motor voltage. The resulting electrical torque is shown at Figure 6.

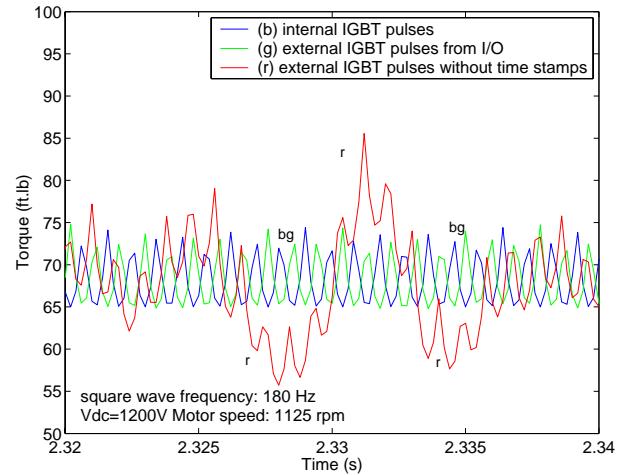


Figure 6 Electrical torque for square wave voltage modulation at the induction machine

The optical IGBT gate signals were generated from an external hardware card connected to I/O and compared

with an exact replica of the signals generated with the RT-Events toolbox. Figure 6 also shows the effects on the simulated machine electrical torque when neglecting the precise in-step timing information, i.e. time stamp, of the IGBT gate signals (trace *r* with excessive jitter). Test results show the importance of the time stamped averaging technique to accurately simulate the machine electrical torque.

D. Test 4: Hardware-in-the-loop with PWM pulse pattern generated from external space vector controller.

The simulator has been tested with an external PWM controller generating fiber optic IGBT gate pulse signals. The controller PWM algorithm is space vector type and has its dead time set to 4 μ s. Figure 7 shows the simulator simulation results (trace *g*) obtained with the external hardware space vector controller. One can observe a 2.5% ripple at 60 Hz on the electrical torque results that may be caused by the controller firing pulse unbalance or algorithm. The bridge-motor model runs at 80 μ s time step for all cases presented in Figure 7.

The trace *b* and *r* presents the result obtained with internally generated PWM firing sequence with sinusoidal-triangular technique. The internal PWM sequence generator is build with RT-Events blockset and is therefore fully compensated for in-step events. One can observe that the 60-Hz ripple has disappeared with the internally generated PWM pulses, demonstrating that the plant simulator provides good result and that the ripple measured in trace *g* is caused by the controller. Again, the worst case is when the time stamp information is not used (trace *m*)

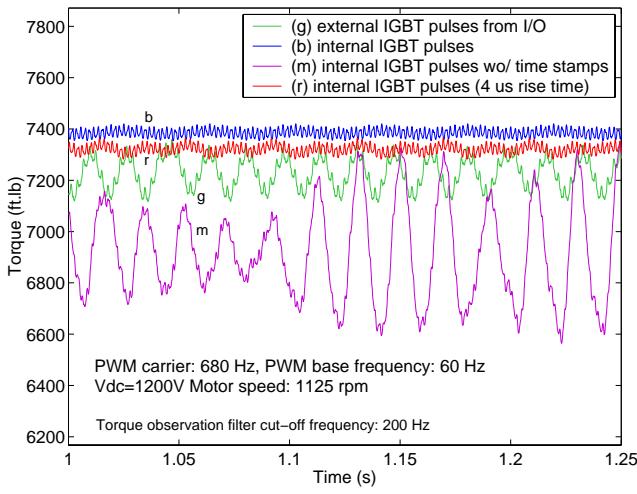


Figure 7 Electrical torque for PWM voltage pattern at the induction machine generated from the I/O

The difference between traces *r* and *g* can be explained in a number of ways. For example, internal and external IGBT patterns are generated with different algorithms, namely space-vector vs. sinusoidal-triangular method. For example, the space-vector algorithm sometimes generates rising and falling IGBT gate signals

within a single time step. Although the bridge algorithm is able to handle such events, the discrete-time RT-Events PWM internal algorithm was not able to generate them in the first place.

E. Test 5: Torque control characteristic accuracy and small signal linearity

An important aspect of the HIL simulation is the fidelity of interaction of the simulated model with the controller. In the case of an IGBT drive inverter, one critical aspect for the accuracy of simulation is the precise capture of IGBT gate pulse timings and their handling in model integration.

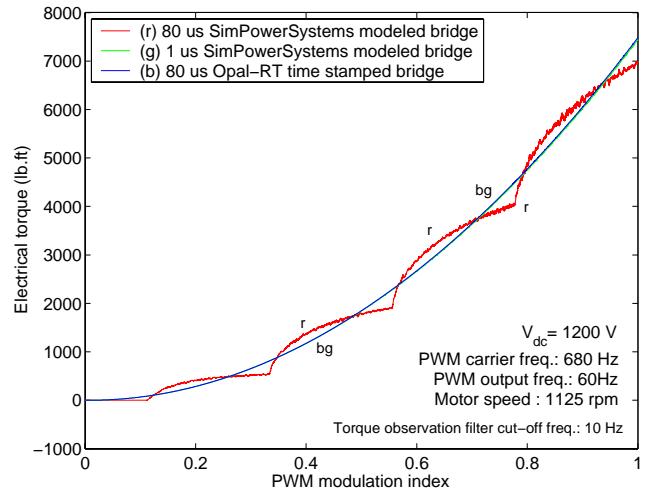


Figure 8 Electrical torque as a function of PWM modulation factor (680 Hz carrier)

To show the point, the time-stamped bridge is compared to the bridge model of SimPowerSystems blockset (PSB).

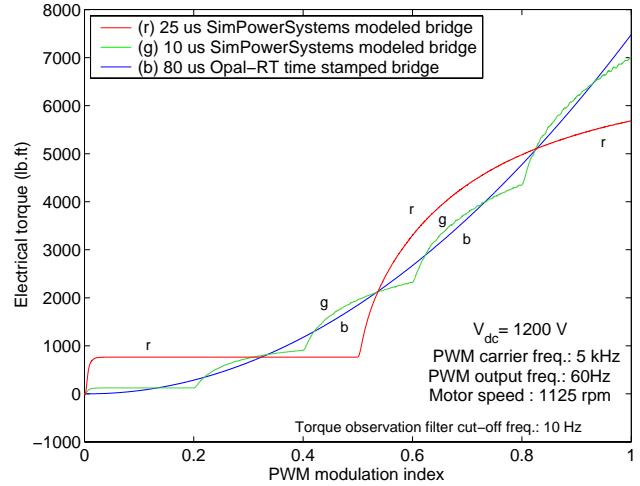


Figure 9 Electrical torque as a function of PWM modulation factor with 5 kHz PWM carrier

The PSB is not designed to compensate the system solution for in-step switching events. With the motor characteristics of Table 1, the PWM modulation index has

been scanned and the resulting electrical torque plotted in Figure 8.

Close exam of the results shows that the time stamping technique allows for accurate reproduction of the torque characteristic at time step compatible with HIL simulation. Sometimes even more critical for controller testing, **the small-signal linearity is preserved for the time stamped bridge** while the uncompensated bridge causes the characteristic to have rude slope discontinuities. Even with a PWM carrier frequency of 5 kHz (Figure 9), the Opal-RT Time-Stamped bridge still shows linearity in its torque control characteristic while uncompensated simulation is not linear even at smaller time steps (25 μ s).

F. Test 6: Measurement of time stamp resolution with the NI6602

The importance of the resolution of the time stamping of the voltage applications to the motor has been established in Section II.C. This test measures the actual precision of the NI6602 timing board used. The maximum resolution of the NI6602 running at 20MHz is 50 ns. But event occurring near the beginning or the end of the time step may hurt this specification because of the synchronization commands that are sent to the card at each time steps.

The test has been made with the IGBT motor drive with fiber optic IGBT gate input to measure the accuracy of the time stamp reading from the NI6602. At a 80 μ s time step, a square wave IGBT gate signal is sent through the fiber optic input and read by the Simulink drive model time stamp reading mechanism. If the square wave rising fronts occur at a rate that is exactly an integer multiple of the time step, then the time stamp read from the I/O will be constant in time.

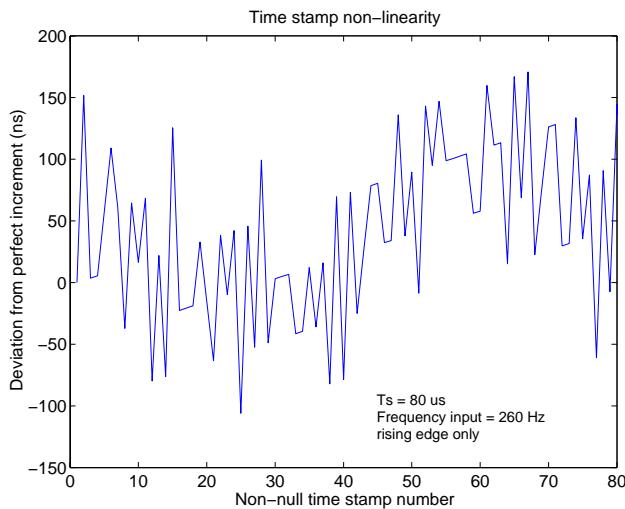


Figure 10 Time stamp deviation from constant increments

The test then consists of sending a square wave with a very small difference to the exact integer period ratio. This results in a scanning of the time stamp from 0 to 1 (in normalized value). In the ideal case, the increase of time stamp values is constant from an event to another. The read time stamp value can then be compared with the ideal

linear increase. This difference is shown in Figure 10. Results show that the NI6602 card has an effective time stamp resolution of ± 150 ns.

IV. COMPUTATIONAL SPEED UNDER RT-LAB

Table 3 shows the obtainable hard real-time step for two drive configurations running under RT-Lab on Pentium III, 1-GHz processors. In both cases, the IGBT gate signals are coming from the I/O.

Table 3: Real-time step size obtainable on 1 GHz PC

Bridge configuration	Hard real-time step
Dual bridge + IPT	80 μ s
Single bridge	65 μ s

In all cases, the computational time of the electrical part of the system (CPU1 in Figure 3: bridges, IPT, DC-link and d-q modeled induction motor) is under 20 μ s. In fact, the main computational burden comes from the I/O latency of the time stamp reading, through the PCI bus on CPU2, from the 5 NI6602 cards (3 for single bridge case) and analog outputs. Therefore, sampling times below 25 μ s are expected with faster FPGA-based I/O technology currently under development at Opal-RT Technologies.

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