Modeling of Series Voltage Source Converter applications with EMTP RV

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Abstract - This paper presents the design of a 3-phase Voltage Source Converter (VSC) that is suitable for series connected FACTS controllers. The proposed converter employs PWM techniques for dc/ac conversion, and by regulating the phase angle of the PWM an adjustable voltage is injected in series with the transmission line to regulate the power flow. The reference wave is obtained by using a symmetrical component transformation that is continuously synchronized with system level waveforms. A PI controller is applied to regulate the amount of injected voltage to the transmission line. The 3-phase VSC is analyzed for controller design, and steady state operation of Static Synchronous Series Compensator (SSSC) without any external energy sources. The operation of the series-connected VSC with the transmission line is verified by simulation with the program EMTP-RV. The results of simulation demonstrate that the converter is able to limit current with a balanced fault, regulate the transmission line reactance, and has low total harmonic distortion and a fast transient response.

Keywords: VSC, FACTS, SSSC

I. Introduction

Switching power converters are the basic building block of a new generation of Flexible AC Transmission System (FACTS) controllers. They are connected in series, parallel or a combination of them to the power system to influence the power flow. A Static Synchronous Series Compensator (SSSC) uses a series Voltage Source Converter (VSC), which injects a voltage with controllable magnitude and phase angle into the transmission line, so it has the capability to rapidly exchange reactive and/or active power with the power system.

The major function of the SSSC is series capacitive compensation of the transmission lines, but compared to a conventional series compensator the SSSC has the capability to rapidly provide both capacitive and inductive compensation. Furthermore, a VSC equipped with an energy storage device on the dc side can supply active power to the transmission line too. These advantages offer additional performance for a SSSC, such as damping out power oscillations, limiting fault current and increasing the transient stability of the power system.

This paper presents a detailed model of a series VSC by using the simulation package EMTP RV, which is a circuit-oriented simulator for power system modeling. The SSSC model is based on the work of Gyugyi in [4]. For the application here, a 2-level Pulse Width Modulation (PWM) technique is employed for dc/ac conversion. The synchronizing reference waves are obtained by use of an algorithm that was proposed in [1]. It provides very fast response to any distortion, and almost without any transient delay. The simulation results demonstrate the ability of a SSSC to regulate the transmission line impedance and limiting the fault current in a power system.

II. Voltage Source Converter

The series compensation scheme for a transmission line power controller, based on a series connected Voltage Source Converter (VSC), is shown in Figure 1. The VSC is connected to the transmission line by a 3-phase transformer. The VSC converts a dc voltage to a controllable set of symmetrical 3-phase voltages. Various types of PWM or multi-pulse control techniques can be employed to perform this power conversion and minimize the production of harmonics to produce a high quality sinusoidal output waveform. By adjusting (a) the angular position of the 3-phase injected voltages with respect to the transmission line currents and (b) the magnitude of the injected voltages, the VSC is able to exchange reactive and/or active power with the transmission line. However, it is pointed out that only a VSC equipped with a (substantial) energy storage device in the dc side can actually supply (steady state) active power to the transmis-

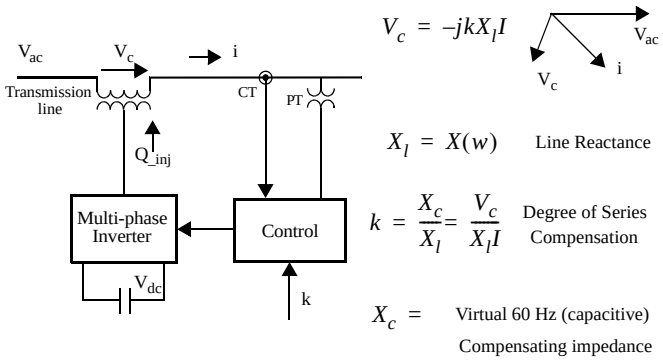

Figure 1: SSSC operates as a series capacitive compensator [4]

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sion line. The injected voltages can be controlled either directly by varying the converter's output to input ratio (modulation index) or indirectly by regulating the dc side voltage of the VSC. The indirectly controlled converters are simpler to implement than directly controlled converters. In indirectly controlled converters only the angular position of the injected voltages (with respect to the transmission line currents) are controlled and their magnitudes remain substantially proportional to the dc side voltage, and the converter is designed primarily to exchange reactive power with the transmission line. However, since the converter usually has some active power losses (i.e. due to imperfect switching devices and resistive losses) the dc voltage risks being depleted unless it can be supplied from either an external or an alternative source. A small amount of active power can be drawn from the transmission line if the injecting voltage is displaced in angular position to maintain the dc voltage.

For simplicity and rapid simulation reasons, only a single 2-level PWM VSC operating at 900 Hz switching frequency is employed. For this reason, a small low-pass output filter is employed with the converter. In practical schemes, 4 or 8 multiple converters with a transformer arrangement will be used to reduce the harmonics generated and produce a very high quality sinusoidal output waveform with either 24 or 48 steps respectively; in this case, no output filter is needed.

III. Power Circuit

In Figure 2, the power circuit of the VSC is shown. A six-pulse converter is used in a 2-level PWM topology. The resistor R in parallel with the dc capacitor C represents the VSC switching losses, and a low-pass delta connected filter (comprising of L_f and C_f) on the ac side eliminates the undesired harmonics generated by the converter. In a practical application, two or four such converters with a magnetic coupler would be used to elevate the pulse number and reduce the harmonics. For the moment, only a single bridge is used for academic purposes. Although the 2-level PWM topology used here offers a simple converter configuration, it has the following disadvantages [6]:

- High dv/dt ratio,
- High switching frequency harmonic, and
- Static and dynamic voltage sharing of series devices.

Consequently, snubber circuits and an output filter are needed. The snubber circuits and output filter are selected to minimize the output harmonics and switching stresses.

Figure 3a shows the switch model with snubber circuits that are used in the converter model. The equivalent switch, identified as “GTO”, and the anti-parallel diode D are represented as ideal switches in EMTP-RV. The small resistors r, in series with the GTO and the anti-parallel diode, represent the switch conduction losses and assist in avoiding any singularity on the inversion of the conductance matrix of the circuit. The polarized series R-L turn-on snubber circuit (consisting of R_{on}, L_{on} and D_{on}) limits the rate of rise of current, and the polarized parallel R-C circuit (consisting of R_{off}, C_{off} and D_{off}) limits the over-voltages during switch turn-off. The values of the snubbers were obtained from equation (1) [7] and fine tuned by trial and error.

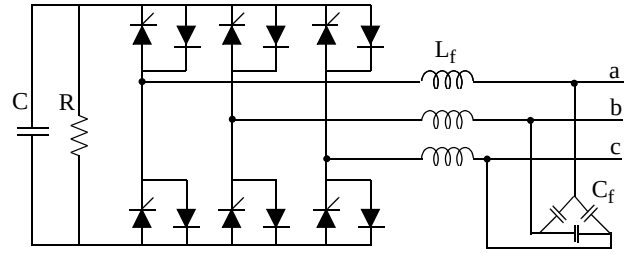

Figure 2: Power circuit of SSSC

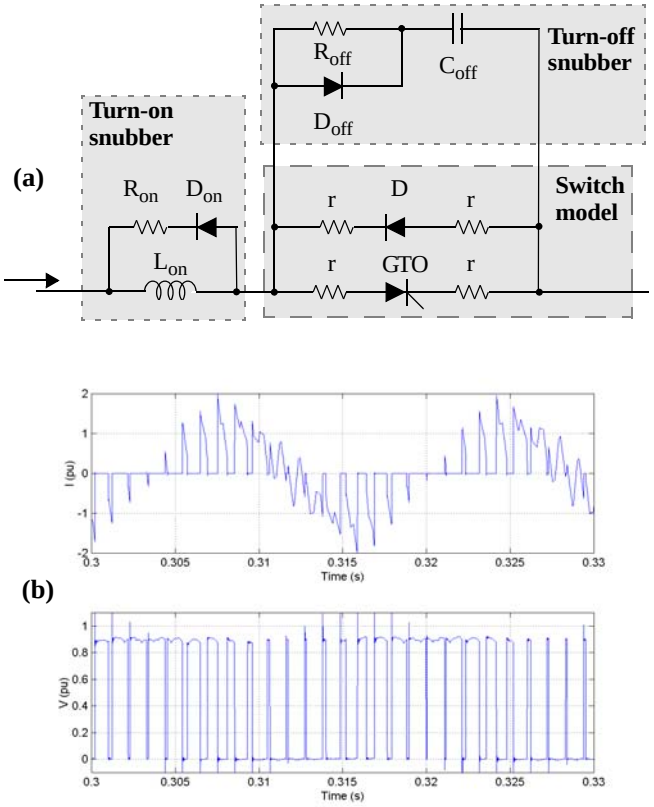

Figure 3: (a) Model of the switch and snubber circuits (b) Examples of the switch current and voltage

Figure 3b shows the current and voltage in a converter switch. The high quality of the switching is evident and the over-voltages are contained. The time-step used is 10 μs to provide a good simulation. With a smaller timestep, the waveform quality would be marginally improved but at the expense of a longer simulation time.

$$
\begin{aligned}
R_{on} &= \frac{\Delta V_{CE}}{I_o} \\
\Delta V_{CE} &= 10\% U_d \\
L_{on} &= \frac{\Delta V_{CE} * t_{ri}}{I_o} \\
C_{off} &= \frac{I_O * t_{fi}}{2 * U_d} \\
R_{off} &= \frac{5 * U_d}{I_O}
\end{aligned}
\qquad (1)
$$

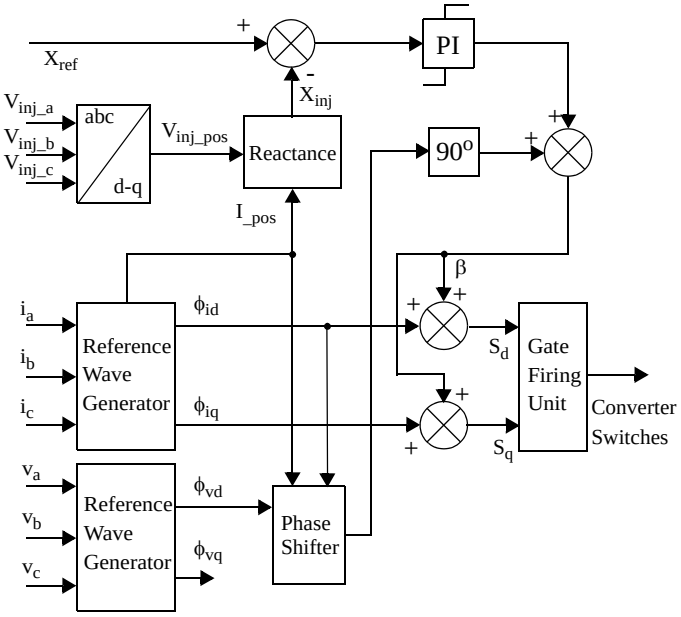

Figure 4: Indirect controller for series VSC

Where t_{ri} and t_{fi} represent the current rise time and current fall time of the switch, and ΔV_{CE} is the voltage drop during the turn-on across the switch. The used values of the present circuit can be found in Appendix.

IV. Control Philosophy

Figure 4 shows the overall control structure of a SSSC with an injected impedance controller. The main function of series reactance compensator is to regulate the power flow in the transmission line. This can be achieved either by controlling directly the power flow or current in the transmission line, or controlling indirectly the compensating (injected) voltage or injected impedance [2]. In some cases (i.e. such as in damping sub synchronous resonance (SSR)), impedance control may actually be preferred. The SSSC can operate either in capacitive or inductive mode. The injected reactance is the injected voltage divided by the transmission line current i.e.

$$X_{inj} = \frac{V_{inj}}{I_{pos}} \qquad (2)$$

The dc voltage of the VSC regulates the magnitude of the injected voltage. If the VSC losses are considered negligible, the injected voltage either lags or leads the transmission line current by exactly 90 degrees.

The Reference Wave Generator (RWG) provides the synchronizing signal, and the sign of the phase shifter determines the either leading or lagging operation of VSC.

To obtain the required phase displacement of the injected reactance, it is compared to a reference value, and a PI regulator amplifies this error. This small phase angle β regulates the dc capacitor voltage in order to keep the injected voltage to the transmission line at the desired value, and also supply the VSC losses.

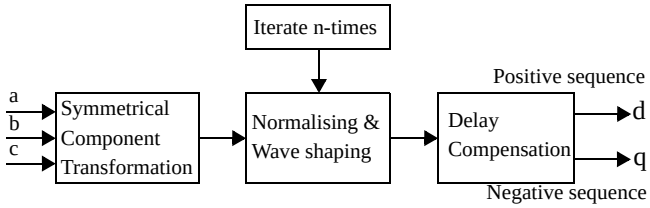

Figure 5: Block diagram for Reference Wave Generator [1]

Further details about individual blocks in the controller are given below.

A. Synchronizing technique

The 3-phase transmission line currents (i_a, i_b and i_c) are used as the reference signals by the controller to generate either lagging or leading voltages by 90 degrees in series with the transmission line voltages. In [1] a Reference Wave Generator (RWG) (Figure 5), based on symmetrical components transformation, was introduced. The 3-phase transmission line currents are transformed into positive, negative and zero sequence components, as indicated by eq. (3):

$$\begin{bmatrix} i_0 \\ i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \qquad (3)$$

Subsequently, a normalizing and wave-shaping block is applied to obtain the original wave under any conditions. And a delay compensation block is used to compensate for the delay caused by the previous wave-shaping block. The delay result of five iterations for a 60 Hz utility frequency and a 10 microsecond sampling time is 1.08 degrees.

The output reference waves (positive and negative sequences) are synchronized continuously with the 3-phase input original waves which could be distorted or contain harmonics. When this approach is compared to a conventional

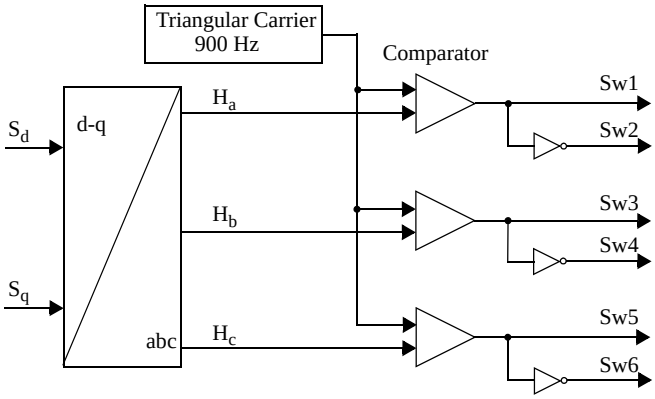

Figure 6: Gate firing unit block diagram

Phase Locked Loop (PLL) technique [5] for extracting distortion free reference waves, this method has a very fast response to any distortion, and is almost without any transient delay [1].

B. Gate Firing Unit (Figure 6)

This block provides the firing signals for the six VSC switches. First, the desired sinusoidal waveforms S_d and S_q are transformed from the d-q axes to 3-phase waveforms (H_a, H_b and H_c). Each phase waveform is then compared to a triangular carrier at 900 Hz, and produces the firing pulses to the six switches of the VSC.

C. Phase Shifter Unit (Figure 7)

This block determines the operational mode of the VSC i.e. whether it operates in capacitive or inductive mode. This decision is made based on either one of two factors:

- First, it senses the phase angle between the positive sequence component of the transmission line voltage ϕ_{vd} and positive sequence line current ϕ_{id}. Since the power system normally operates with an inductive load, the phase shifter output sign is negative, and sets the VSC to operate in the capacitive mode to compensate for the inductive load.
- Second, the positive sequence component of line current (I_pos) is compared to a fault current reference value (I_lim). This current reference value is pre-set as the condition of an over current limit. Should I_pos exceed this limit, the output sign of the phase shifter is made positive and sets the VSC operation mode in an inductive mode of operation.

V. Simulation Results

The power system (Figure 8) described in [3] was simulated with EMTP RV to evaluate the performance of the proposed series VSC. The operating voltage of sending end is 230 kV, and the transmission line impedance is (26 + j132) ohms. The controller is designed to compensate 60% of the transmission line reactance. Three tests are presented here to investigate performance of the system-controller:

- Impact of a step change of reference value of injected reactance,
- Impact of load variation on the series VSC performance, and
- Impact of a balanced fault at the receiving-end (bus B3) of the system.

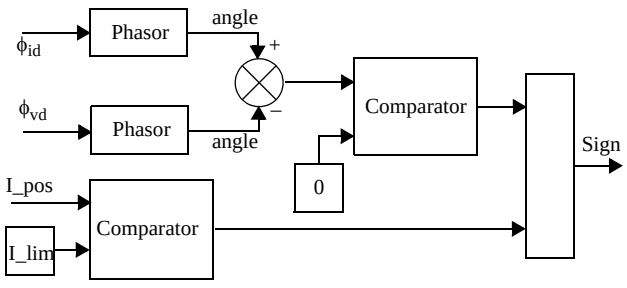

Figure 7: Phase Shifter block diagram

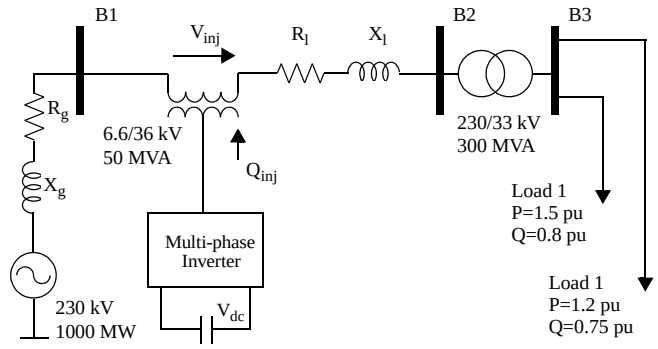

Figure 8: Single line diagram of power transmission system [3]

A. Impact of step change in reference of injected reactance

The dynamic behavior of the controller is verified by applying a 10% step change in the injected reactance at time t = 500 ms till 800 ms (Figure 9). The dc voltage reference is 1 pu at 10 kV. The signals are described below:

(a) This shows the reactance reference step and the response of the controller. The dynamic response is stable and takes about 50 ms for rise time and 100 ms for the settling time.

(b) This shows the dc voltage of the VSC. When the reactance step down is applied at 500 ms, the dc voltage increases to increase the magnitude of Vinj.

(c) This demonstrates the transmission line current. By injecting higher capacitive reactance to the transmission line at 500 ms the line current increases.

(d) This shows the three phase angles between the 3-phase injected voltages and transmission line currents. The angles are almost 90 degrees, at 500 ms. when the disturbance is applied, the phase angles decrease transiently and VSC absorbs more active power from the transmission line. At 800 ms the phase angles transiently increase over 90 degree for a short period of time (20 ms) to inject the active power back to the transmission line and discharge the dc capacitor.

(e) This illustrates the injected reactive power to the transmission line. When the reactance step down is applied at 500 ms, the injected reactance increases.

B. Impact of load variation

The dynamic behavior of the series VSC is verified by a 20% increase of the receiving-end load at time t=500 ms till 800 ms (Figure 10). The signals are described below:

(a) This shows the injected reactance to the transmission line. Even a 20% change in the load causes only a transient that is damped quickly and the steady state injected reactance stays constant.

(b) This shows the fluctuation of the transmission line currents.

(c) This shows the dc voltage of the VSC. When the load

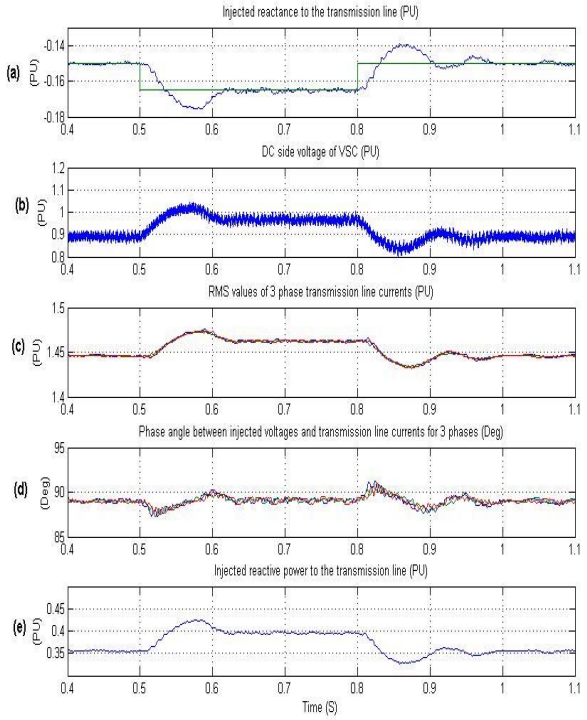

Figure 9: System response to step change in controller reference value (a) Injected reactance (b) Dc side voltage (c) Transmission line currents (d) phase angles (e) Injected reactance

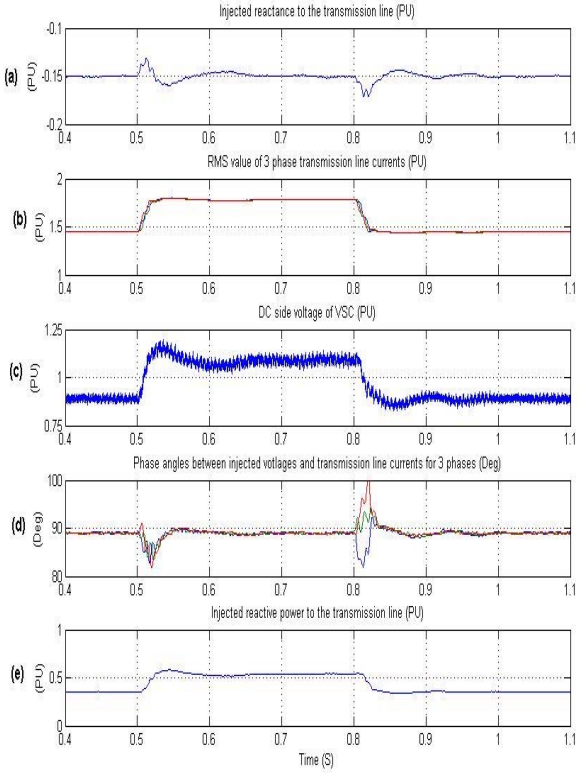

Figure 10: Impact of load variation (a) Injected reactance (b) Dc side voltage (c) Transmission line current (d) Phase angle (e) Injected reactive power

increases at 500 ms, the dc voltage increases to provide the required injected reactance.

(d) This shows the phase angles between 3-phase injected voltages and transmission line currents. The angle is almost 90 degrees, at 500 ms the phase angle transiently decreases and VSC absorbs more active power from the transmission line. At 800 ms the phase angle transiently increases over 90 degrees for a short period of time (20 ms) to inject the active power back to the transmission line and discharge the dc capacitor.

(e) This illustrates the injected reactive power to the transmission line. When the reactance step down is applied at 500 ms, the injected reactance increases in the order to keep injected reactance constant.

C. Impact of a balanced fault at bus B3 of the system

The capability of the series VSC in a balanced fault condition is tested by applying a 3-phase fault on bus B3 at t = 500 ms till 800 ms. The transmission line current increases to a peak of 2.5 pu during the fault. To limit the fault current the VSC injects an inductive reactance in series with the transmission line. Figure 11 shows the simulation results.

(a) This shows the injected reactance to the transmission line. At 500 ms the VSC operates in inductive mode, the dynamic response is stable and the settling time is about 50 ms. At 800 ms when the fault is removed, the VSC operates in capacitive mode the dynamic response is stable but it takes about 150 ms for settling time.

(b) This shows the rms values of the 3-phase transmission line currents. The peak fault current value is limited to 1.9 pu.

(c) This shows the phase angles between 3-phase injected voltages and transmission line currents. At 400 ms the angle is almost 90 degrees, at 500 ms during the inductive operation the phase angle changes to -90 degrees. At 800 ms the phase angle returns to 90 degrees.

(d) This shows the dc voltage of the VSC. When the reactance step down is applied at 500 ms, the dc voltage decreases.

(e) This illustrates the injected reactive power to the transmission line. At 400 ms the injected reactance is positive and VSC injects reactive power to the transmission line, when the VSC operates in inductive mode the reactance is negative and the VSC absorbs reactive power.

VI. CONCLUSION

The paper presents a detailed model of a Static Synchronous Series Compensator by using the EMTP RV simulation package. The series VSC regulates the transmission line impedance by using an indirect controller. The VSC generates a set of 3-phase voltages almost in quadrature with the transmission line currents, so it emulates a capacitive or an inductive reactance in series with the transmission line. The simulation results illustrate the ability of the controller to regulate the transmission line reactance and limit the line current following a balanced fault in the power system.

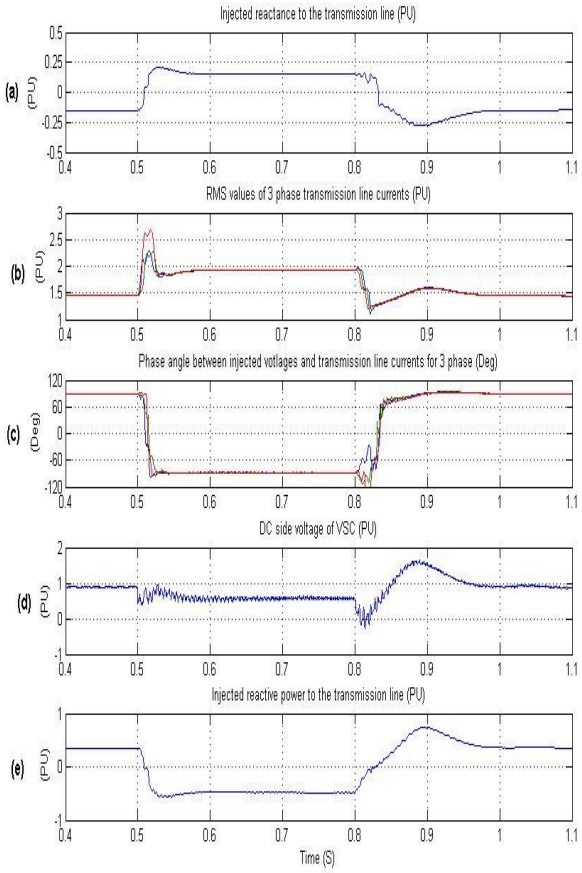

Figure 11: System responses to 3 lines-to-ground fault (a) Injected reactance (b) Transmission line currents (c) Phase angle between injected voltage and transmission line current (d) Dc side voltage (e) Injected reactive power

VII. ACKNOWLEDGEMENT

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VIII. APPENDIX

A. The system parameters of Figure 6 are:

S = 100 MVA base
V = 230 kV base

B. Transmission line:

Reactance X_l = 0.25 pu
Resistance R_l = 0.05 pu

C. Power transformer: (Y/Δ) Rated power: 300 MVA

Rated voltage: 230/33 kV
Leakage reactance: 0.01 pu

D. SSSC: Rated 50 MVA

Nominal dc voltage: 10 kV
Nominal ac voltage: 6.6 kV
Switches forward resistance: 1 milli-ohm
Total capacitance: 1 mF

E. Coupling transformer: Rated at 50 MVA

Rated Voltage: 6.6/36 kV
Resistance: 0.001 pu
Leakage reactance: 0.02 pu

F. Snubber circuit:

R_{on} = 0.1 m-ohm
L_{on} = 5 μH
C_{off} = 0.1 μF
R_{off} =10 ohms

IX. BIOGRAPHIES

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