Stochastic Approach For Modeling Arcing Faults In Cables From Experimental Data

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Abstract— **This paper discusses stochastic arcing fault models developed based on examination of test data conducted at shipboard system voltage levels by the US Navy at KEMA-Power Test, Inc. The arc model resistance had a typical mean value based upon physical parameters of the particular class of test and a random variation around this mean value. Models were developed for arcing faults on both on AC and DC systems. The models were developed using ACSL (Advanced Continuous Simulation Language) and verified with the test data results so the arcing fault models could be included in simulations of shipboard power systems for conducting fault studies to set protective devices and rate apparatus. The main objective of the model development was to match the ratio of arc voltage to fault current between the test data and the simulation results.**

Index Terms— **Arcing fault, Arc resistance.**

I. Introduction

THE design of a power system involves determining settings for the protective equipment, rating circuit breakers, and determining insulation ratings for cables and other equipment and similar tasks. Knowledge of the magnitude of fault current levels is needed a-priori to rate and set the protective equipment. Therefore, simulations play a key role in the design of a power system. Bolted faults, low impedance faults, and high impedance faults can be easily modeled as constant impedances. However, it is more difficult to build detailed models of arcing faults that include the arc behavior.

The complex behavior of arcs makes the modeling of arcing faults a challenging task [1-5]. Complicating factors include the variations of arc due to the conditions surface of the conductor, atmospheric conditions, etc, and it is often not practical to develop a model that incorporates random variations of these parameters.

This paper describes the development of a stochastic model that represents an arcing fault as a mean resistance with a randomly variation around this value. This model was used develop simulation cases to match the results of experimental tests on several classes of ac and dc cables proposed for use in shipboard power systems. The project sponsors will insert the resulting arcing fault models into simulation models that include detailed representatiions of the shipboard power system and conduct fault studies. The results of these studies will be used to determine magnitudes of fault currents and resulting voltages on system components to rate circuit breakers, rate insulation and overvoltage devices, and to set protective devices. The Advanced Continuous Simulation Language (ACSL) [6] was used for the detailed shipboard power system model, so the arcing fault models are developed in ACSL as well. The models have also been implemented in using FORTRAN statements in the control system modeling language in an emtp-type program as well.

Section II of the paper provides background on the high voltage hardware testing. Section III describes other methods for modeling arcing faults. Section IV introduces the stochastic model. Sections V and VI describe the power system representation in the simulation model and show simulation results for several cases. Section VII describes the model verification.

II. Background

At present, the main shipboard power distribution systems used by the U.S. Navy are ungrounded, 450V, 60Hz systems. Future generations of ships will see substantial increases in loads, with additions such as electric propulsion systems, electromagnetic launch systems to replace steam catapults and rail guns in place of cannons. As a result, the Office of Naval Research is studying the feasibility of increasing the voltage levels to 4160V ac (presently used in some applications already) or as high as 13.8kV ac. The use of dc distribution is also under consideration.

At the same time the electrical loads are increasing, there is also an increased concern with the sensitivity of existing and projected loads to voltage sags due to faults that result during normal operation or from battle damage. The tripping of critical loads such as weapons control systems under such conditions could leave the ship unprotected until the systems reboot.

The higher fault current levels possible at higher operating voltages makes it more imperative to be able to detect and interrupt faults quickly. In addition, the physical design of the system requires circuit breakers capable of interrupting these fault currents, plus the equipment must be able to withstand

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the physical forces applied by the fault currents. As an early part of this study, the US Navy conducted a series of short circuit tests were performed at KEMA Power Test on ac and dc systems in the medium voltage range. Several different methods were used to initiate these faults, such as driving nails into the cable housing or stringing piano wire between the conductors. However, each test run had the fault present when the system was energized. The tests implemented three phase and phase-to-phase faults. Since the shipboard systems are ungrounded, single-phase-to-ground faults were not tested at that time. Most of the tests fell into the following categories:

- Three-phase fault initiated by #34 wire (cable insulation removed in faulted section).
- Three-phase fault with two of the phase conductors are touching the third phase conductor that was bolted to a support.
- Three-phase or phase-to-phase faults where holes were drilled through the insulation and nails were placed in the holes.
- Three cable conductors and cable shields bolted together and tied to cell ground.

The results of these tests, which included the voltage across the arc and the current through the arc in all of the phases, were used to build the fault models.

The system designers next wanted to incorporate the results of these tests into computer simulation models of the shipboard power system and their protection schemes. The objective of the work presented here was to develop a simulation model for them in ACSL to be compatible with the full shipboard power system model.

III. Existing Arc Models

Over the years much research has been done in developing fault models. However, much of this work has concentrated on models of arcs in circuit breaker contacts. Some of the models that are relevant to modeling arcing faults are discussed below:

A. Instantaneous Arc Model

An instantaneous arc model was developed by Matthews [1] for a resistive-inductive system. He described the model using the following differential equation:

$$V_{max}\sin(\omega t) = Ri_{arc} + L\frac{di_{arc}}{dt} + V_{arc}. \qquad (1)$$

where V_{max} is the system voltage, and R and L are the resistance and inductance between the arc and the source. This model is limited by an arc voltage, V_{arc} which is assumed to be a known constant. It is an insightful tool for analyzing electrical systems in buildings.

B. Arc Voltage Models

Other models were developed based on the arc voltage, which is a function of current. Among these models, the first model incorporates a current dependent arc voltage based on an equation formulated by Stokes and Oppenlander [2] for instantaneous arcing voltage. The equation used for this model is:

$$V_{max}\sin(\omega t) = Ri_{arc} + L\frac{di_{arc}}{dt} + (20+534g)\, i_{arc}^{0.12}, \qquad (2)$$

where g is the arc's electrode gap, V_{max} is the system voltage, and R and L are the resistance and inductance between the arc and the source.

A second arc voltage model incorporates an arc voltage based on the product of arc current and Fisher's equation for the arc's resistance [3]. The equation used for this model is:

$$V_{max}\sin(\omega t) = Ri_{arc} + L\frac{di_{arc}}{dt} + \left(25\sqrt{39.37g}\right) i_{arc}^{0.15}. \qquad (3)$$

Again, g is the arc's electrode gap, V_{max} is the system voltage, and R and L are the resistance and inductance between the arc and the source.

C. Arc Conductance Models

A model by D.L. Hickery, E.J. Bartlett and P.J. Moore [4] classifies arcing faults as strong arcs and weak arcs. Strong arcs, often referred to as primary arcs, are high current arcs that produce short arc paths that are typically a few meters in length and have a very large cross section. The strong arc path carries a heavy arc current and so is not elongated by external factors, its dynamic arc characteristic is represented by:

$$\frac{dg_p}{dt} = \frac{l}{2.85\times10^{-5}I_p}\left(\frac{|i|}{15l} - g_p\right), \qquad (4)$$

where g_p is the conductance of an arc of length l, and i is the arc current with a peak value of I_p.

Weak arcs are often referred to as secondary arcs which carry a small current, typically up to 55A, whose arc paths have a relatively small cross-section. Therefore, physical factors, such as the wind, do significantly affect the path of the arc and so must be taken into account when modeling the weak arc. This dynamic arc characteristic is represented by:

$$\frac{dg_s}{dt} = \frac{l_s(t_r)}{2.51\times10^{-3}I_s^{1.4}}\left(\frac{|i|}{75I_s^{-0.4}l_s(t_r)} - g_s\right), \qquad (5)$$

for arc conductance g_s, arc length l_s, and an arc current i with a peak value of I_s.

IV. Stochastic Model

As discussed earlier, while modeling an arcing fault, concentration on the interaction with the system is of prime concern. In this case one needs to model arcs formed between cables or between a cable and ground. While modeling arcs for systems with short three phase cables, as is the case in this study, the main parameter controlling the arc current is the source impedance since the conducting path for the arc is relatively short. The voltage across the arc is dependent on the arc's resistance and varies as the arc resistance varies. Frequency domain transformations of the test data from KEMA showed mean 60 Hz energy and a wide band noise floor in the voltages and currents. By taking the ratio of voltage to current the 60 Hz component of the arc's resistance was obtained.

Next a sliding time domain window was used to examine the instantaneous arc resistance values for the test data. The window was one 60 Hz cycle in length and was stepped forward in one tenth of a cycle increments. The window's moving average was used to extract the arc resistance information in the frequency domain, which was then put into the simulation models. All of the above analysis was performed in Matlab. This analysis was used to compute the standard deviation of the resistance around the mean value. The standard deviation seen was typically 5% to 10% of the mean resistance.

The arc resistance was seen to have a typical or non-varying mean value (the 60Hz component computed above) and a random time variation around this mean value. Analysis of the time varying term showed a normal (Gaussian) distribution around the mean value. Therefore, the random time varying term was modeled by a normal distribution sampled at each simulation time step. This was implemented by calling a normally distributed random number generator at each time step (not that it may be necessary to convert a uniform random number generator output to a normally distributed one). The resulting number was multiplied by the standard deviation value computed above for the specific class of tests and then added to the (constant) mean value for that class to comprise the model's total arc resistance. This resulted in the simple arc resistance formula of

$$R_{arc} = R_{mean} + R_{std}\ x(G), \tag{6}$$

where $x(G)$ is a the output of a random number generator with time sampled Gaussian distribution. This model was developed using ACSL as specified by the project sponsor. The model has also been implemented using TACS commands in ATP. The model's stochastic properties are demonstrated in the analysis shown in Figure 1. The first plot shows the arc resistance versus the number of time steps. The second plot shows the distribution of the resistance values. Note that the resistance values show a Gaussian distribution. The experimental results show a similar variation.

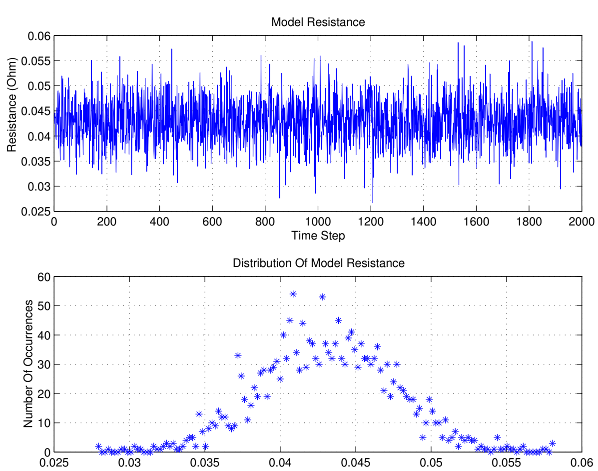

Fig. 1. Quantitative analysis of the stochastic model.

V. Test Setup

The basic layout for the testing allowed for each of the desired voltage and current measurements to be made in an environment safely removed from the test area. The arcs were produced in a closed metal container fed through the walls by electrical bushings. Outside the container the source was cabled to the bushings. Two data acquisition systems, each consisting of eight channels capable of a 0.1 msec sampling period, fed by fiber optic isolation amplifiers were connected there also to record the arc voltages and currents (through CTs).

The source used for the AC tests was a 21 MW 3ϕ generator capable of either 4160 V AC or 13.8 kV AC line to line. The generator fed a PCM-4 2 MW converter to create the source for the DC tests. The 4160 V tests were conducted using ten T400 cables that were each 100 ft. long. The 13.8 kV tests were conducted using four T400 cables that were also 100 ft. long.

Figure 2 shows the test circuit for the 3ϕ AC tests and simulations, with cable impedances of $R_L = 0.000775\Omega$ and $X_L = 0.000725\Omega$, and a source impedance $X_s = 0.5\Omega$ for the 13.8kV tests and $X_s = 0.162\Omega$ for the 4160V tests. Figure 3 is the test circuit for the DC tests and simulations where the source has the following parameters $V_{dc} = 1000V$, $R_s = 0.1333\Omega$, $L_s = 8.0mH$, and the cables have the following parameters $R_L = 0.000775\Omega$, $L_L = 1.923\mu H$,

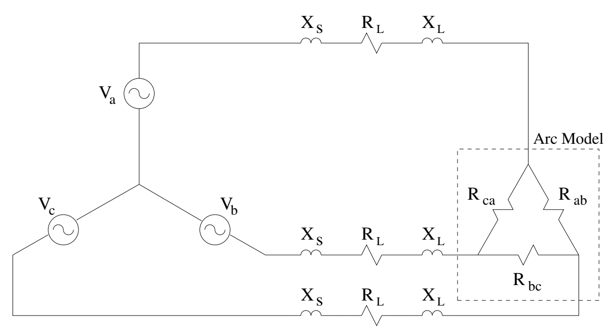

Fig. 2. Schematic of the 3ϕ AC test setup.

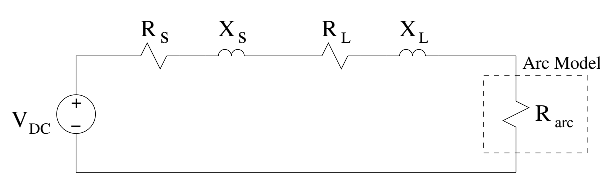

Fig. 3. Schematic of the DC test setup.

VI. Simulation Results

Comparison of 3ϕ AC phase-to-phase fault current waveforms from the simulation results shown in Figure 4, to the test data shown in Figure 5 show proximity of the current amplitudes as do the corresponding voltage waveforms in Figures 6 and 7. Note that there is visible noise present on the voltage waveform but not in the current. This is due to the current smoothing effect of the dominant source reactance.

Note also, that the experimental voltage waveforms show steps as the voltage crosses thresholds in the analog to digital converter used to record the measurements (the arc voltages are small compared to the rated phase-to-phase voltages). This behavior limits the accuracy of the models. Some cases had more detailed voltage measurements.

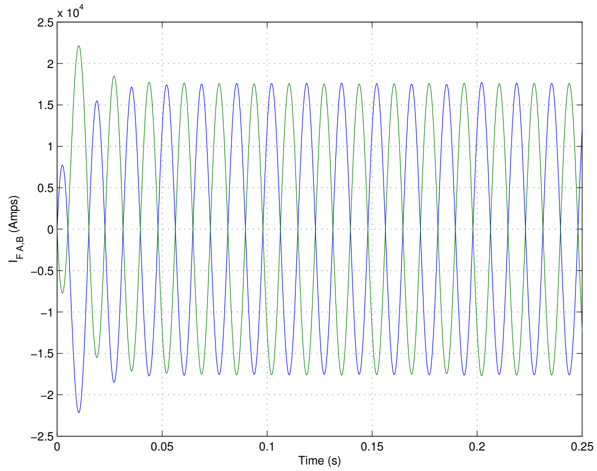

Fig. 4. Current waveforms of line to line fault simulation results.

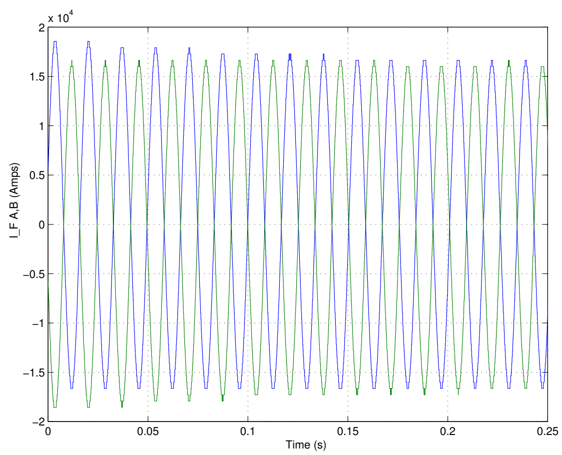

Fig. 5. Current waveforms of line to line fault KEMA test results.

Comparison of simulation and test currents and voltages for a 3ϕ delta fault is shown in Figures 8, 9, 10, and 11. The simulation model did not include the transient and subtransient reactances of the generator since they were not provided, so the currents in the experimental results are initially much larger than those in the simulation results. The simulation results are close to the steady-state currents experimental results. The arcing fault model will be plugged into simulation models that include detailed machine models.

Note that the measured voltages in this case show more detail than in the phase-to-phase case above. Also, note that the conductors started to move apart in the experimental test, causing the arc voltage to vary. The sliding window method used to derive the simulation model averages this behavior and does not show variations in arc length due to conductor movement.

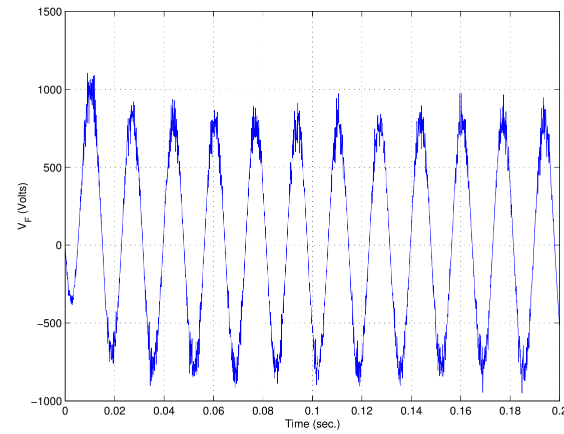

Fig. 6. Voltage waveforms of line to line fault simulation results.

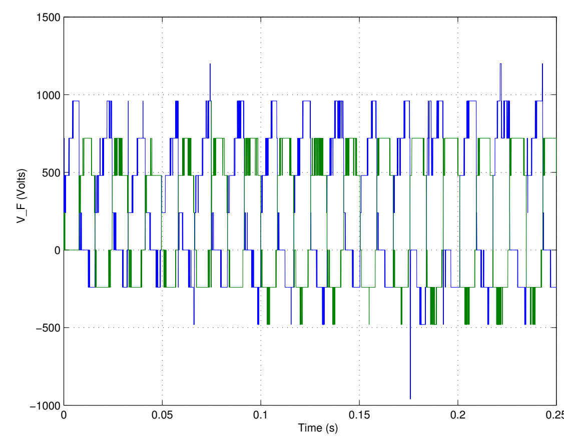

Fig. 7. Voltage waveforms of line to line fault KEMA test results.

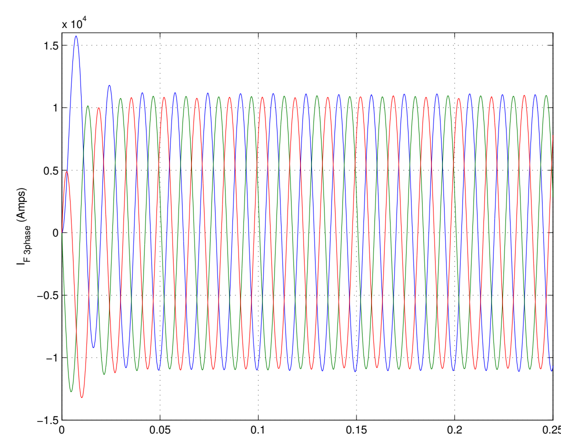

Fig. 8. Current waveforms of 3ϕ fault simulation results.

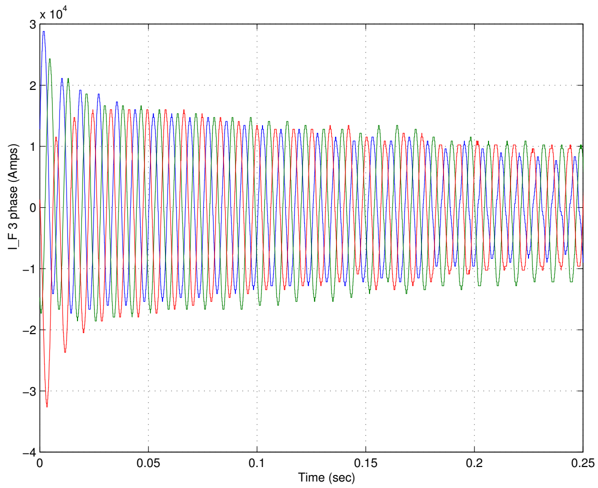

Fig. 9. Current waveforms of 3ϕ fault KEMA test results.

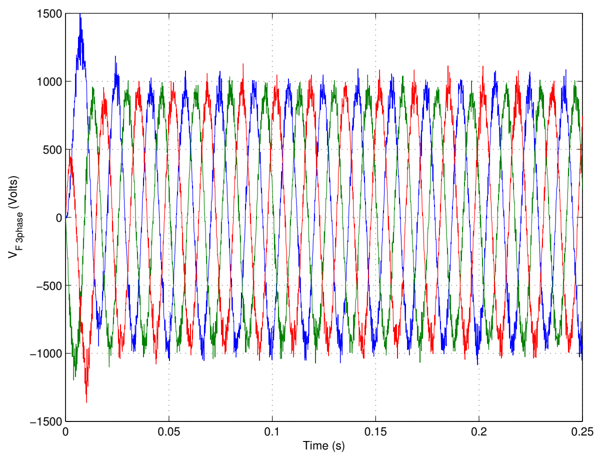

Fig. 10. Voltage waveforms of 3ϕ fault simulation results.

Plots of DC fault simulation currents and voltages are shown in Figures 12, and 13. Notice that the currents are again smooth with all of the variation present in the voltage. The test set up for these cases had a large inductive filter on the dc source.

VII. Spectral Comparison

In order to provide additional simulation model parameter adjustment, and another type of model validation, the spectral energy density of the simulation results were compared to that of the test data. This was done by performing a Fast Fourier Transform on the voltage and then on the current during the fault period of the data. Then the frequency domain voltage and current vectors were multiplied by each other to obtain an energy spectral distribution.

A spectral analysis of the test data for a three phase fault studied is shown in Figure 14 and a spectral analysis of the corresponding simulation result is in Figure 15. From a visual comparison it is evident that the simulation has a little less randomness than the test data but a slightly larger 60 Hz component. However they are similar in magnitude.

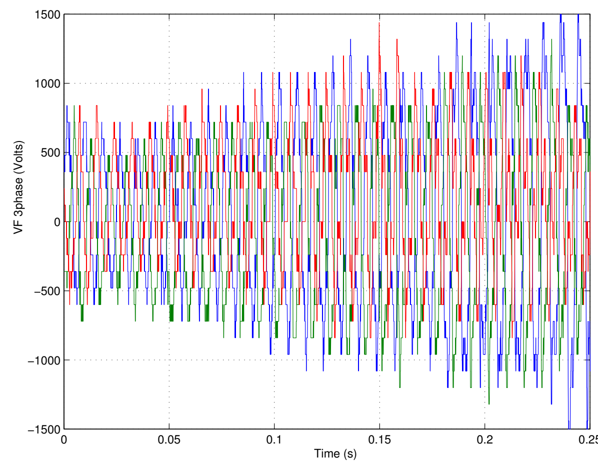

Fig. 11. Voltage waveforms of 3ϕ fault KEMA test results.

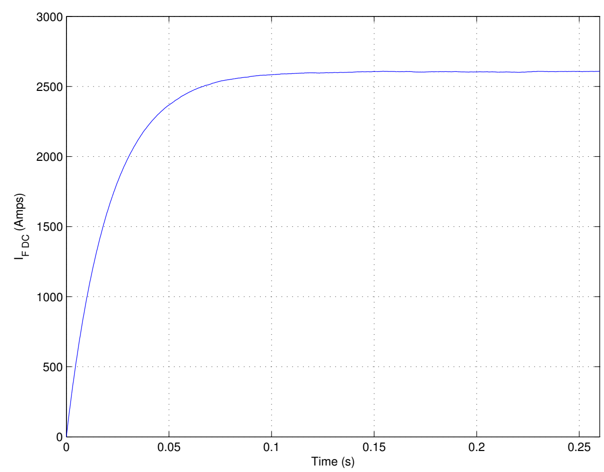

Fig. 12. Current waveforms of DC fault simulation results.

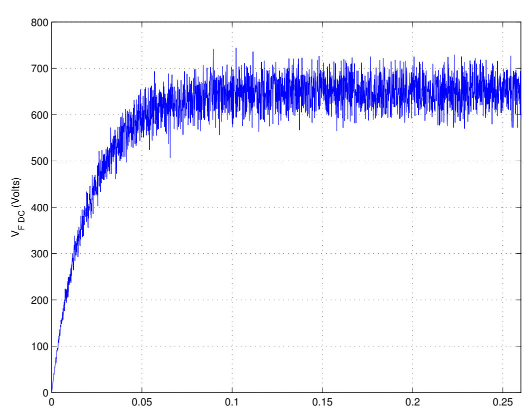

Fig. 13. Voltage waveforms of DC fault simulation results.

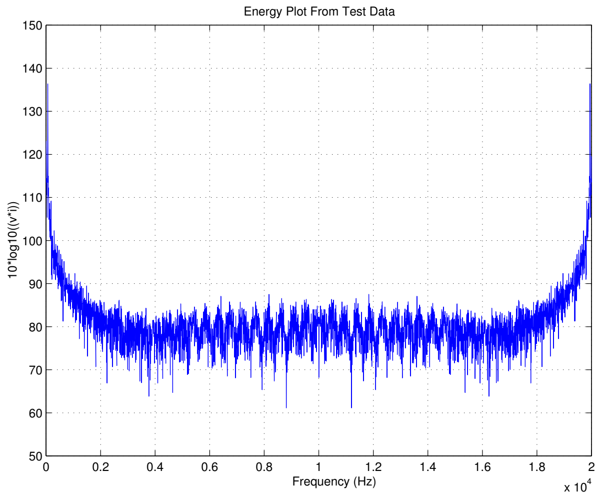

Fig. 14. Spectral analysis of the test data.

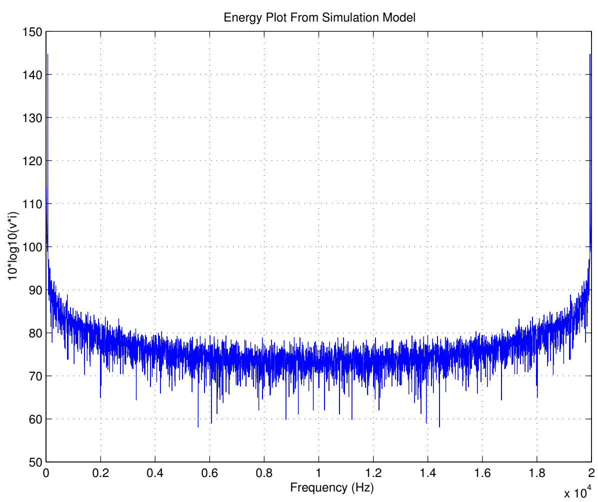

Fig. 15. Spectral analysis of the simulation results.

VIII. Conclusion

A stochastic arcing fault model with mean arc resistance plus a random variation was developed. The model was implemented in ACSL and simulation results are compared to experimental measurements on medium voltage cables. Review of the simulation and test results shows that the model succeeding in reproducing the overall electrical effect of the arcing fault. It was not intended to duplicate detail such as conductors swinging around due to the fault arcing, which, due to the complex and varied physical conditions surrounding each individual fault occurrence, would be an unrealistic task. The function of the arcing fault model, therefore, is to bind the ratio of current to voltage at the fault point in a circuit simulation, within the limits of a random variation. The actual respective magnitudes of these currents and voltages are set by the equivalent open circuit voltage and impedance of the network that feeds the fault model. The models presented here were developed for performing short circuit studies to determine equipment current ratings and test protection schemes. The model can be also used to examine the interaction between arcing faults and the power system, similar to the presentation in [7].

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IX. Biographies

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Brian K. Johnson received the PhD. in Electrical Engineering from the University of Wisconsin-Madison in August 1992. He is currently a professor in the Department of Electrical and Computer Engineering at the University of Idaho. He is a member of the Board of Governors for the IEEE Intelligent Transportation Systems Society. His interests include HVdc transmission, power system protection, the application of power electronics to utility systems, and real-time simulation of traffic systems.