An FPGA-based Real-Time Digital Simulator for Power Electronic Systems

Mahmoud Matar, Reza Iravani

Abstract--Testing digital controllers for power electronic systems in real-time using a real-time digital simulator presents a problem, due to the discrete nature of the controller outputs which are not necessarily in synchronism with the time-step of the simulator. Reducing the simulation time-step resolves the issues resulting from the lack of synchronism between the digital simulator and the hardware controller under test. The simulation time can be reduced by distributing the computational burden among a number of parallel processors. However, the reduction in time is not directly proportional to the number of processors due to the interprocessors communication overhead.

However, the simulation time can be greatly reduced if the simulator's hardware is custom configured. This paper is an effort to introduce and develop a reconfigurable hardware simulator using FPGAs to simulate power systems that contains power electronic switching elements. The simulation time-step for this simulator is less than 100ns. A new time domain model for power electronic switching elements is also presented in this paper. The new model is very convenient for real-time simulation purposes due to its simplicity and the elimination of numerical oscillations associated with other models.

Keywords: Real-time simulation, Switching, Modeling, Field Programmable Gate Array (FPGA)

I. Introduction

Power systems are rapidly developing and getting more hybridized with the inclusion of power electronic converters that serve to control power flow and to improve dynamic behavior and reliability of supply. Controllers are the heart of a power electronic converter and insure its proper functionality. Since prudent utility practice forbids experimenting with the actual systems, these controllers have to be tested and their functionalities be verified before commissioning.

To test controllers under actual network conditions or simulate their in-operation behaviors, closed loop testing is required to attain the objective. Closed loop testing allows accurate study and evaluation of component interactions due to the action taken by the device under test.

In the past, analog simulators, based on scaled down models of power system components were used for testing controllers and protective devices. However, due to complexity, cost, size limitations and inherent practical limitations they have been replaced by software-based digital simulators, especially after the advancements in digital processing devices.

Digital simulation of power systems is essentially a step-by-step numerical solution of the system's differential equations. Hence, digital simulators can not give a continuous history of the system's variables, e.g. voltages and currents, but rather a sequence of snapshots at discrete time intervals. The simulation time-step (Δt) directly defines the fastest transient that can be accurately represented. Smaller time-steps allow representation of higher frequency phenomena. However, as the time-step is decreased the computation time required to complete the required calculations increases.

A primary distinction between different types of digital simulators is the speed at which the calculations are performed to generate corresponding data points of the waveforms. If the time required for computation of each data point is less than the time-step, the computation is said to be in real-time, and if the computation time is greater than the simulation time-step, the waveforms are generated off-line.

The use of software based simulation tools have become largely accepted for simulating power systems. However, one of the main limitations of these programs is that they primarily operate in non-real-time (off-line). That is, the CPU time required to compute the response of the modeled system might take several seconds, minutes, or orders of magnitude longer than the actual time response. Off-line simulation can verify the physical and mathematical concepts behind a certain controller or a protective device. However, its non-real-time operation precludes interfacing external equipments to the simulator and therefore limits application of such simulators for testing physical control/protection platforms.

To close the loop, it is necessary that the simulator be able to accept input information from the hardware based control/protection platform under test, and to incorporate this information into the ongoing simulation run. The system's equations need to be solved fast enough, so that the outputs are available before the arrival of the next sample, or mathematically

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$$t_c \le \Delta t \quad (1)$$

where t_c is the computation time and Δt is the simulation time-step.

The hardware of a real-time digital simulator is usually based on computers with parallel processors [1] – [6]. Each processor may represent a different section in the power system under study and a master processor is used to control the communication between the other processors. The simulation time of these simulators is usually dependant on the processors speed, number of processors and the efficiency of the software code.

The main problem associated with simulation of power systems containing power electronic switches is the inter-simulation time-step switching. Digital controllers for power electronic systems present a problem when testing in real-time using a digital simulator due to the discrete nature of their outputs which are not necessarily in synchronism with the time-step of the simulator. Since the simulator, unlike an actual system, can not respond instantaneously to the switching event, errors are introduced to the simulation results. The error can result in occurrence of switching mistakes, incorrect power flows, and noncharacteristic harmonics. The error can grow considerably large with the growing number of switching elements. Also the larger the simulation time-step the larger will be the error.

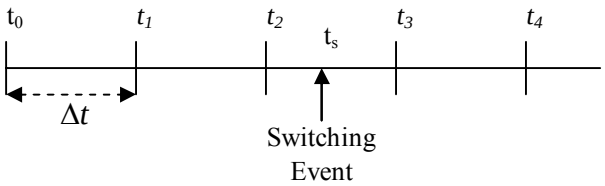

Fig. 1. Inter-Simulation Time-Step Switching

Fig. 1 illustrates the problem of inter-simulation time-step switching. The firing signal is issued at time t_s, but is accounted for at time t_3 when the simulator has already calculated the incorrect state of the system at t_3.

The existing real-time simulators that typically use a 50 μs simulation time-step fail to accurately simulate power systems containing power electronic switches. Techniques have been developed to deal with inter-simulation time step switching. These techniques are based on interpolations/extrapolations [7]-[10]. However, as switching frequencies go higher, the probability of occurrence of multiple switching events within a simulation time-steps will increase. Thus, with the occurrence of multiple switching events within simulation time-steps, multiple interpolations/extrapolations are needed. Hence, the computation time per simulation time-step increases and violation of real-time constraints may occur.

Reducing the simulation time-step improves the accuracy of the simulator as the error due to inter-simulation time-step switching is reduced. If the simulation time-step is hundred times less than the switching period, there is no need to synchronize the simulator and the controller under test, as the error due to asynchronous operation can be neglected.

Due to the sequential nature of processors (either General Purpose Processors or Digital Signal Processors), the simulation time-step of the existing processor-based real-time digital simulators cannot be small enough to simulate switching networks with the desired accuracy. Moreover, the enhancement in performance by increasing the number of parallel processors is not directly proportional to the number of processors as interprocessors communication-time imposes additional overhead time that can severely limit the performance. However, the simulation time can be greatly reduced if the simulator's hardware is custom configured. The objective of this research is to develop a reconfigurable hardware simulator using Field Programmable Gate Arrays (FPGAs) to simulate power systems that contain power electronic switching elements. The modeled power system is implemented in an FPGA chip such that the calculation time is smaller than the simulation time-step.

An FPGA is an integrated circuit that contains identical logic cells that can be viewed as standard components. The logic cells are interconnected by a matrix of wires and programmable switches. A user's design is implemented by specifying a logic function for each cell and selectively closing the switches in the interconnect matrix. Complex designs are created by combining these basic blocks to create the desired circuit.

An FPGA, unlike a digital signal processor (DSP), is a parallel device and its hardware is custom configured for the job at hand. FPGAs are very efficient in performing mathematical operations, and especially multiplication operations. Parallel hardware multipliers can be implemented as required, allowing simultaneous calculations. FPGAs have also the advantage of flexible word size, therefore precision is not lost and no extra resources are consumed [11], [12].

II. Modeling of Power Electronic Switches

Aside from inter-simulation time-step switching issue, time domain modeling of power electronic elements is a challenge in itself. Switch models can cause various problems. They may introduce numerical oscillations to the simulation results, cause convergence errors and lead to the formation of singular system of equations.

There are quite a number of power electronic elements models with different levels of complexity. The level of complexity of the model is a function of the required level of detail of the study/simulation being conducted [13]-[15].

At the system level simulation, much more simplified models for power electronic elements are used. These models are derived from the fact that a switch has a small impedance when ON and a large impedance when OFF.

Of the system level simulation tools are real-time digital simulators. The simulation time-step of a real-time digital simulator should be fairly low to provide accurate results and at the same time the system's equations need to be solved fast

enough, so that the outputs are available before the arrival of the next sample, i.e. the computing time is less than the simulation time-step. Thus, for the sake of shortening the computing time, it is better to use simplified time domain models to replace power electronic elements rather than using more accurate complex models.

Simplified models for power electronic elements range from ideal switch representation where switches are represented by a short circuit when ON and an open circuit when OFF, to two valued resistors where a switch is represented by a small resistance when ON and a large resistance when OFF, to discrete-time switch models where a switch is represented by a conductance G_s in parallel with a dependant current source as shown in Fig. 2 [16]-[18].

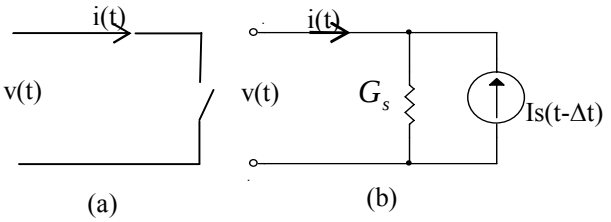

Fig. 2 Discrete Time Switch Model

In both the ideal switch model and the two valued resistors model, the system's admittance matrix is not fixed. The admittance matrix changes with each switching event. Thus the admittance matrix has to be inverted every simulation time step or at least, whenever the topology of the network changes. This adds additional computational burden on the simulator's hardware. This fact motivated the development of the discrete time switch model where the admittance matrix is kept constant irrespective of switching events. As the switch conductance G_s is the only part of the switch model that appears in the admittance matrix and thus, it is kept constant regardless of the switch state. The change in the switch state is reflected only by the value of the shunt current source.

Several discrete-time switch models have been presented. However, most of these models represent a switch by a small inductance when ON and by a small capacitance when OFF. A problem associated with L/C based switch models is the introduction of numerical oscillations to the simulation results and it is common to have artificial voltage spikes in the simulation results. One way to solve this problem is to add a damping resistance to the switch model. However, adding this damping resistance introduces two challenges. First, you have to properly calculate the value of the damping resistance to provide the right amount of damping, and second, introducing this damping resistance adds to the complexity of the power system model being simulated and thus the simulation time (and/or) the hardware resources of the simulator increases.

A. New Switch Model

The new model presented in this work is from the discrete-time switch models category. In this switch model, a switching device is also represented by a fixed conductance Gs in parallel with a dependant current source as shown in Fig. 2. Thus, the admittance matrix is kept constant irrespective of the topology of the system. The change in the switch state is reflected only by the value of the shunt current source. The value of the shunt current source is calculated as follows:

If the switch is OFF, the value of the current source is given by

$$I_S(t) = G_S.V(t) \qquad (2)$$

If the switch is ON, the value of the current source is given by

$$I_S(t) = -G_S.V(t) \qquad (3)$$

By careful inspection of (2) and (3), it is obvious that they are the same except for a sign change. Thus, it is clear that the changes in a switch states are reflected only by the sign of the shunt current source. This model eliminates the problem of numerical oscillations that occur in the other discrete-time switch models based on L/C representation of switches.

Moreover, since the problem of numerical oscillations is inherently solved by the new model, there is no need to add damping resistors as in the other models. Thus, this model is much simpler than the other discrete-time switch models.

This model is an artificial model and thus its parameters cannot be related to the parameters of the actual power electronic element being modeled. One way to determine the value of the switch conductance Gs is to compare the simulation results with other benchmark simulation and optimize the value of Gs to minimize the error. This model is especially developed to be used in real-time simulators, so prior knowledge of Gs is not required. You can always optimize the value of Gs on an offline simulator before you use this value to conduct real-time simulations. From the experience gained from conducting several simulation scenarios, a value of unity for Gs can always give accurate simulation results for practical power systems. Setting Gs equal to unity greatly reduce the switch model. Thus, when this model is used, it can end up by just determining the value of the voltage drop across the switch and use it with the proper sign to represent the switch in both the ON and OFF states.

This paper contains two case studies, the first one is a simulation of a step down chopper and the second one is a simulation of a three phase voltage sourced converter (VSC). Matlab Simulink is used as the benchmark simulation tool to compare the simulation results.

The first case study shows the modeling and implementation of the step down chopper shown in Fig. 3

The second case study shows the modeling and implementation of a three phase voltage sourced converter (VSC) shown in Fig. 4. Fig 5 shows the external AC system

connected to the VSC terminals.

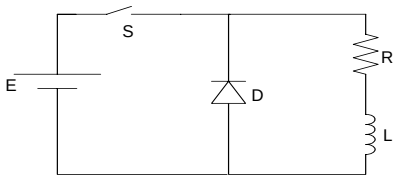

Fig. 3 Step Down Chopper

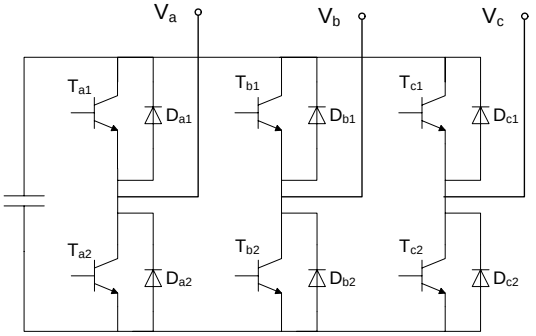

Fig. 4 Three Phase Voltage Sourced Converter

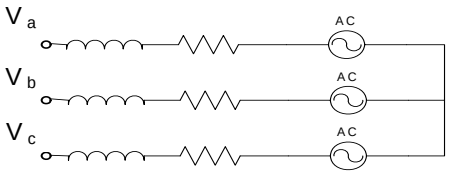

Fig. 5 External System

III. FPGA IMPLEMENTATION

By replacing each element by its time domain model, we obtain an equivalent network for the power system under study consisting only of resistive elements and current sources [19]. The node voltages at all nodes of the power system are calculated by the nodal equation

$$[Y].[v(t)] = [i(t)] - [I] \quad (4)$$

where $[Y]$ is the nodal conductance matrix, $[v(t)]$ is the column vector of the node voltages, $[i(t)]$ is the column vector of current sources and $[I]$ is the column vector of history current sources.

It is clear that the system to be simulated is reduced to a set of discrete algebraic equations, which are used to calculate the values of the current sources standing for the previous states of the elements and the voltage at each node.

Separate units will be implemented on the FPGA chip, where each unit is dedicated for the evaluation of a single equation. Each of the discrete equations either for the calculation of voltages or currents, comprises mainly two mathematical operations, multiplication and addition. Therefore, hardware multipliers and adders will be implemented in each unit.

After the completion of the implementation phase, the following units should exist on the chip as shown in Fig. 6:

- M modules dedicated for calculating the voltage at different nodes of the system.
- N modules dedicated for updating the values of equivalent current sources representing the history states of the system.

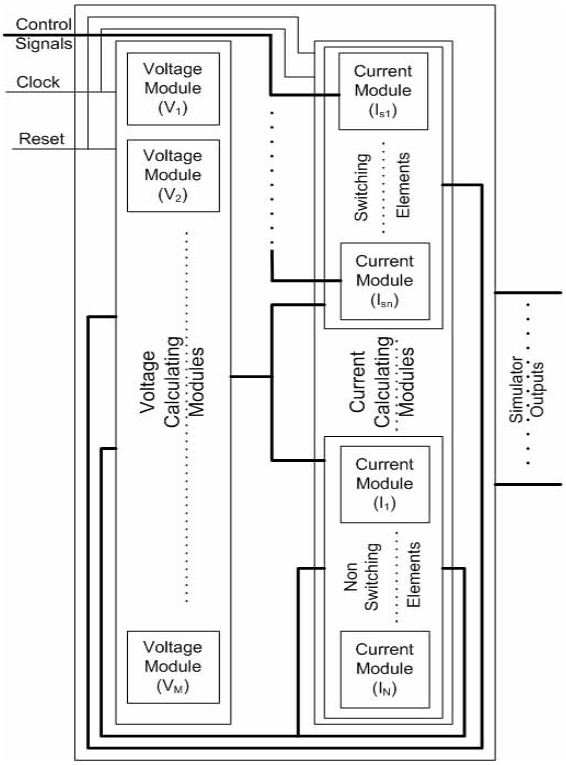

Fig. 6 Schematic of the FPGA Implemented model

During each clock cycle, the previous states of the system, which is represented by the current sources, are used to calculate the node voltages at different nodes, and then the new values obtained for the voltages is used to update the values of the current sources. To perform these dependant operations in one clock cycle, the calculations are split into two stages, the first stage is triggered by the rising clock edge and the second is triggered by the falling clock edge as shown in fig. 7.

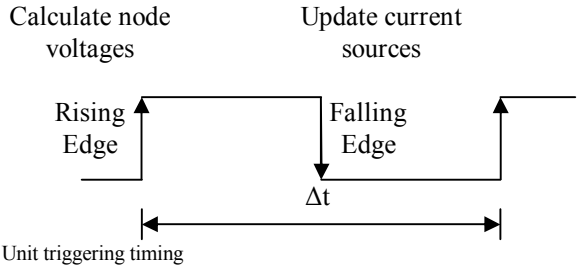

Fig. 7 Unit triggering timing

Each of the implemented units is equipped with an edge detecting unit that triggers the unit when the proper edge is detected such that

- The rising clock edge triggers the voltage-calculating modules.
- The falling clock edge triggers the Current sources updating modules.

IV. Case Studies

The step down chopper shown in Fig. 3 is implemented and simulated using Altera Quartus II version 6.0. The test system is implemented on an Altera Stratix EP1S10F484C5 FPGA chip. The chip's inputs are the battery voltage and the control signal of the chopper. The chip can output the voltages at any node and the currents at any branch.

The chopper is loaded with an inductance L = 100 mH and a resistance R = 10 Ω. Two time-domain models were implemented; one using an L/C discrete time switch model and the other using the new switch model. The digital time domain models are formulated based on a selected simulation time-step Δt of 500 ns.

This system can be simulated with a maximum clock frequency of 29.89 MHz, i.e. the minimum simulation time step is 33.5ns. Table 1 is the utilization summary of the selected chip for both of the implemented models.

TABLE 1. FPGA Utilization Summery

L/C discrete time switch model	
Total Logic Elements	649 out of 10570 (6%)
Logic Elements for Power Electronic Switch models	252
New switch model	
Total Logic Elements	521 out of 10570 (5%)
Logic Elements for Power Electronic Switch models	88

Figure 8 compares between the simulation results for the inductor voltage of the test system obtained from Simulink and that of the FPGA implementation for both switch models.

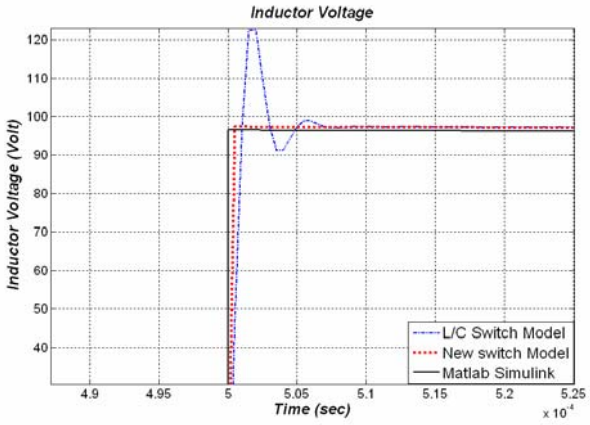

Fig. 8 Simulation results for the inductor voltage of the step down chopper

It is clear from fig. 8 and fig. 9 that the new switch model resolves the problem of numerical oscillations and that the simulation results using this model is within the desired accuracy. Moreover, comparing the number of logic elements needed for FPGA implementation for both models, shows that the new switch model greatly reduce the required hardware resources for implementation. A reduction of up to 65% is achievable using this new model.

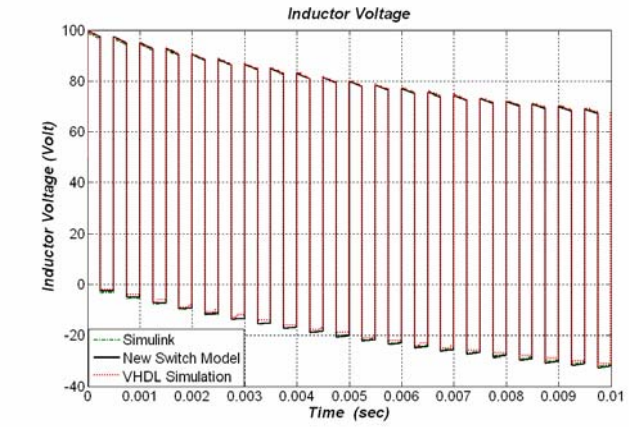

Fig. 9 Comparison between the simulation results obtained from Simulink and that obtained with the new switch model for the inductor voltage

Table 2 gives the parameters of the three-phase VSC system shown in Fig. 4 and Fig. 5. The digital time domain model is formulated based on a selected simulation time-step Δt of 500 ns.

TABLE 2. Test System Parameters

DC Voltage	100 V
Three-phase AC Voltage	110 V - 50Hz
DC Source Impedance	0.0156 Ω
External System Inductance	10 mH
External System Resistance	10 Ω

The test system is implemented and simulated using Quartus II version 6.0. The test system is implemented on an Altera Stratix EP2S15F672C3. The three-phase VSC along with the external system consumes 31% from the selected FPGA chip. It is found that the computation time per simulation time-step is 29.812 ns. Thus, this system can be simulated with a maximum clock frequency of 33.54 MHz, i.e. the minimum simulation time- step is 29.812 ns.

Figure 10 compares between phase (a) inductor current generated from Matlab simulation and the simulation results of the FPGA implemented simulator for an SPWM switching scheme. The SPWM carrier frequency is 2 kHz.

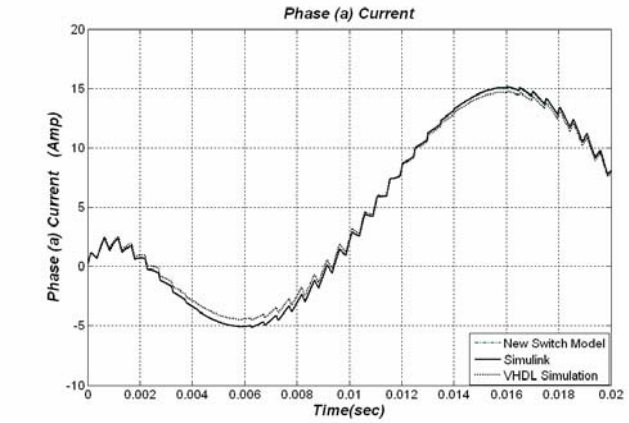

Fig. 10 Simulation results for phase (a) inductor current of the VSC system

As can be noticed there are slight discrepancies between

Matlab simulation and the simulation results of the FPGA implemented simulator. This due to the quantization error associated with this kind of proposed FPGA simulators. As the coefficients of the system's equations along with the signal variables can only take discrete values within a specified range since the registers where they are stored as well as the buses for transferring data are of finite length. This error can be reduced by increasing the number of bits of the simulator's registers. However, this leads to consuming more resources from the FPGA. A compromise is done between the size and accuracy depending on the accuracy required from the simulator.

V. Conclusions

FPGAs have an excellent potential to become the implementation medium for mathematical models of power systems by virtue of their low price and very high speed resulting from its parallel structure. Computation time per simulation time-step is as low as 30ns. Thus, very small simulation time-steps can be used, allowing the interfacing of digital controllers with the simulator without concerning about inter-simulation time-step switching issue.

A new model for power electronic switches has been developed and verified. The new switch model enables the formulation of constant admittance matrix for systems containing power electronic switches, irrespective of the state of the switches. Moreover, the new switch model solves the problem of numerical oscillations associated with the other available models.

The new switch model is well suited to be used in real-time digital simulators due to its simplicity. This model is especially suitable to be used in FPGA-based real-time digital simulators as it greatly reduces the required hardware resources needed to implement the switch model.

VI. Acknowledgment

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VIII. Biographies

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