Impact and characterization of voltage transients as a problem to sensitive loads

Hugo Ribeiro, Victor Anunciada

Abstract - In the last three decades, the loads connected to the mains network had been changing. Due to constant progress in electronic equipments, the number of electronic and sensitive loads increases considerably in domestic and industrial environment. Short duration voltage transients can have a several economic impact in these equipments. The authors identify the sensitive loads connected to the mains network and realize a study of their susceptibility to transient voltage perturbations in the mains network.

Key words: Switch Mode Power Supplies, Susceptibility, Voltage Events, Electronic Equipment, Sensitive Loads.

I. INTRODUCTION

The economic impact in industrial environment as a consequence of an electrical failure imposes the study of power quality. The main preoccupation of producers and consumers is the avoidance of any electrical energy failure and the maintenance of the RMS mains voltage inside the range of ±10% of the nominal voltage, according to the limits defined by standard EN50160.

In the past, loads like lamps, 50Hz transformers, induction motors and heating resistances represent the main loads linked to the mains network. The concepts of power quality presented in standards are related with their susceptibility. Due the constant progress made in electronic areas, the number of electronic and sensitive loads increases considerably in domestic and industrial environment. These equipments are much more sensitive than the ones referred. Voltage transients, with short duration, less than 10ms, in the mains voltage can damage these equipments. It is true that an electrical failure may represent a severe economic impact. However, the damage on sensitive equipment, present in the production process, can have the same or even worse impact as consequence of voltage transients, particularly if this equipment remains damaged. In function of this approach, this paper presents a study of the sensitive loads to the mains network together with the identification of the voltage transient events present in the mains network that are related with their susceptibility.

II. SENSITIVE EQUIPMENT

Nowadays a great part of the electric loads have an electronic circuit in their conception. This electronic circuit can be a controller, a power converter, etc. The interface between the mains network and these electronic circuits is usually a power supply or an AC-DC converter. In the last three decades these power supplies were built with a 50Hz transformer to reduce the amplitude of the mains voltage and to guarantee galvanic isolation, and also with a single phase rectifier and a filter capacitor, to obtain output continuous current. To achieve output regulation a linear regulator was used. Fig. 1 shows this type of power supply, where I_O represents the current in the load and V_I the mains voltage amplitude.

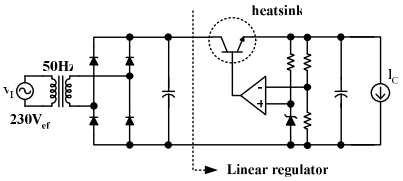

Fig. 1 Configuration of a traditional AC-DC power supply.

This solution presents the disadvantages related with the low frequency (50Hz) transformer: large dimensions, high weight and cost. In addition, due to linear regulation the overall efficiency was low (<50%). To solve these problems, this type of power supply has been replaced by switch mode power supplies (SMPS). The SMPS realizes isolation with a high frequency ferrite transformer actuated with a DC-AC square wave converter, or inverter, and due to the switching process presents higher efficiency. Fig. 2 shows the basic building blocks of a SMPS.

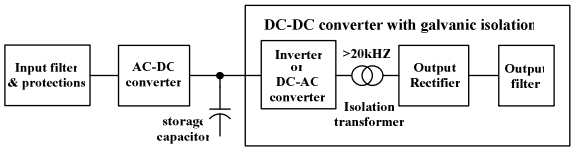

Fig. 2 Building blocks of a SMPS.

The SMPS with their good characteristics, high efficiency, low cost and weight and reduced dimensions, are extensively used in industrial, professional and domestic environment. There are still other loads as inductive motors, lamps or heating resistances that do not use a SMPS in their conception. Due to their associated inertia, these loads are not sensitive to voltage transients. The SMPS constitutes, therefore, the main and the most sensitive load that is present in the mains network. This way, the study of the susceptibility of sensitive loads to perturbations in the mains network is based on the study of the SMPS.

H. Ribeiro is with Instituto politécnico de Tomar and Instituto de Telecomunicações, 2300, Portugal, hugo@ipt.pt.
A. Anunciada is with Instituto de Telecomunicações and Instituto Superior Técnico, Lisboa 1000, Portugal, Victor.Anunciada@lx.it.pt.

III. SWITCH MODE POWER SUPPLIES (SMPS)

This section describes the functions of the building blocks presented in Fig.2.

A. DC-DC converters

The DC-DC converter regulates the output voltage and guarantees the galvanic isolation between the input and output voltages of the SMPS. As an example, Fig. 3 shows a full-bridge DC-DC converter with galvanic isolation.

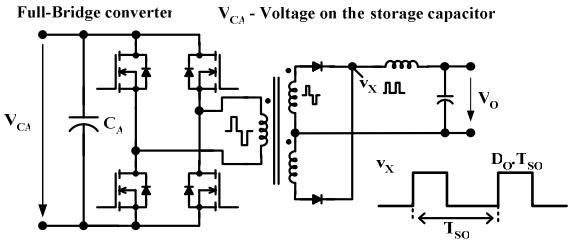

Fig. 3 Isolated full-bridge converter with output rectifier and LC filter – the power circuit topology is used in medium and high power SMPS.

For medium power (P < 500W) the switching frequency, f_S, is normally less than 100kHz. The output LC filter is designed to obtain a good attenuation at the switching frequency. In general, the output ripple voltage is less than 1% of the output voltage. This condition constrains the cutoff frequency, f_C, of the output filter. Typically, the cutoff frequency is 30 or 100 times less than the switching frequency, f_S, in order to guarantee a good attenuation.

Equivalent series resistor (ESR) and equivalent series inductance (ESL) present in the output capacitor must be considered in the output filter design. Sometimes it is necessary to use a double LC filter due the effect of the ESR and ESL. Fig. 4 shows the influence of the ESR in the attenuation of a double LC output filter. The values presented in Fig. 4 results from a commercial PC SMPS, with an internal switching frequency of 66 kHz. The value of ESR is 68mΩ, measured with an impedance analyzer HP4294.

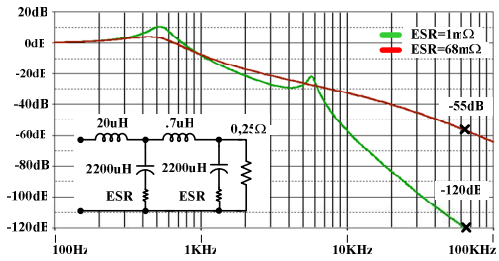

Fig. 4 Influence of ESR in the attenuation of the output filter.

The output voltage control is usually achieved by a pulse width modulator PWM and PI regulator and may be realized in voltage mode or current mode control. The current mode control presents better performance but is more expensive and is used only in high performance equipments or industrial equipments. Alternatively, the voltage mode control is the most common voltage controller used in domestic applications.

Fig. 5 shows an output voltage controller working in voltage mode.

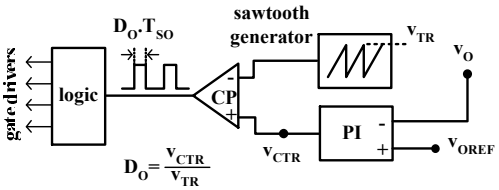

Fig. 5 Output voltage controller in voltage mode.

To guarantee the stability of the controller and the high gain at low frequency (<1kHz), the time response of the control is quite slow (0,2 - 1ms). The output duty ratio D_O adopted is normally 0,5 to 0,7, to allow a low-volt transient in V_{CA}.

Several topologies of DC-DC converters are used in SMPS. All of them present a high frequency transformer that is required in order to obtain galvanic isolation and voltage adaptation, as well. The physical size of those transformers is an important factor on the SMPS manufacturing costs. The size reduction and leakage induction minimization imply a considerable leakage capacitance between primary and secondary. The number of primary turns is minimized. Typically, the transformer has a safety security of 25% into the magnetization current.

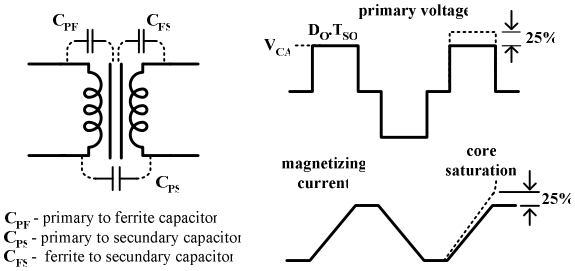

Fig. 6 Transformer leakage capacitors and core saturation.

B. AC-DC conversion

The AC-DC conversion is usually obtained with a diode bridge and capacitive filtering, C_A. The output voltage is approximately equal to the peak voltage of the mains input. The storage capacitor is designed to guarantee a voltage interruption of 20ms up to 30ms (hold-up time or stand-on time), without any variation in the output voltage, V_O. These criteria result on a residual AC component less than 5% of the peak value in C_A. The storage capacitors are large electrolytic capacitors, performing a good filtering effect at 100Hz. Their ESR and ESL are very large. Consequently, their impedance raises for frequencies above some few kHz (1-10kHz), resulting in a very poor filtering at higher frequencies.

When the storage capacitor is discharged, and the power supply turned on, the peak value of the input current is extremely high and must be limited. Most manufacturers use a Negative Thermal Coefficient (NTC) resistor prior to the AC-DC converter (Fig.7). During the first seconds of operation the NTC warms up and its resistance decreases considerably and

does not affect the SMPS efficiency (typically 1% of losses).

Some equipments complying with EN61000 standard, use a boost converter, Fig. 7, in order to perform input current waveshapping. In this case the DC voltage is 15% to 25% higher than the mains input voltage peak value (360-400V, for 230V AC input).

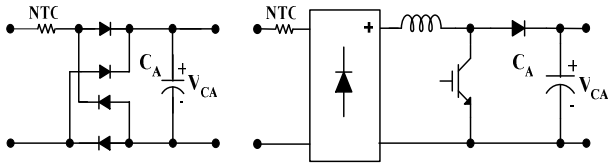

Fig. 7 AC-DC conversion in a SMPS, without and with input current waveshaping.

The use of this auxiliary converter introduces the regulation of the storage capacitor voltage, which remains almost independent of the mains voltage. The boost converter permits the operation of the SMPS in the extended range input (80-240Vrms). This converter is very insensitive to the input voltage disturbances.

C. Input filter and protections

The input filter (RFI filter) is intended to suppress radio frequency noise that results from transistor switching in the DC-AC converter. Typically, it presents an attenuation of 30 to 50dB, at frequencies above 1 to 5MHz and is designed to operate with noise amplitudes up to 1 to 5mV. Fig. 8 shows some topologies of RFI filters.

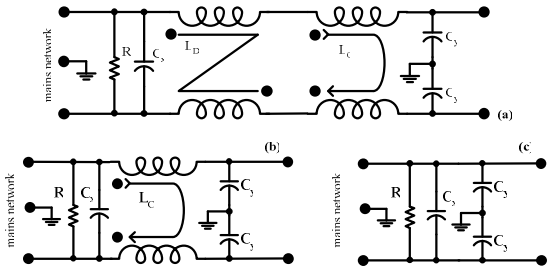

Fig. 8 Topologies of RFI filters.

The transformers formed by the inductances L_D and L_C, presented in Fig.8, are for differential mode and common mode noise rejection, respectively. The capacitors C_X and C_Y are very small, typically C_X<100nF and C_Y<10nF. These capacitors are designed to present low impedance at frequencies higher than 1MHz and to supported high voltage transients. These capacitors are subject of several tests, described in the standards IEC60384-14 and EN132400. For steady state operation, the C_X and C_Y capacitors support 135% and 185% of V_I, respectively.

The topology of the RFI filter and the components values are dependent of the noise emitted by the SMPS. As a consequence, the topologies and the components values can be different in identical SMPS. In domestic applications, the topologies (b) and (c) of Fig.8 are extensively used. The topology (a) is used more in industrial applications.

Usually, the input protections of the SMPS include over-voltage protections. Fig. 9 presents four different protections utilized in SMPS.

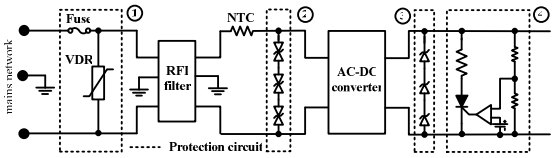

Fig. 9 Over-voltage protection circuits: (1) VDR; (2) bipolar Zener; (3) unipolar Zener; (4) voltage controller thyristor.

A Voltage Dependent Resistor (VDR), bipolar and unipolar Zener diodes (suppressor diodes) and a voltage controller thyristor circuit can be used. The circuits have the same operation principle, when the clamping voltage, V_{CLP}, is passed, the circuit conducts and blows the input fuse for excess of current. The correct over voltage protection requires the use of the VDR and one of the other circuits. In industrial SMPS, the VDR and the bipolar Zener diodes are normally used. Contrarily, in domestic applications only the VDR is used. Fig. 10 shows the voltage and current characteristic curves of these two devices.

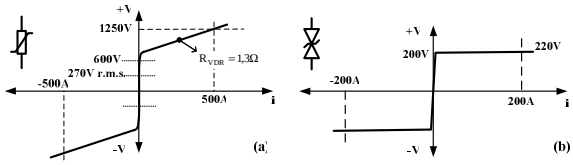

Fig. 10 Voltage and current characteristic curves: (a) 250Vrms VDR; (b) 200V bipolar Zener diode.

In SMPS the VDR presents typically a conduction voltage, V_{CON}, 120% of V_I and a clamping voltage of 185% V_I. This way, a low leakage current above some few μA (50 - 200μA) is guaranteed. This device can support energy dissipation greater than 10J to 100J. The Zener diodes have a clamping voltage well defined and present low dynamic conduction resistance, but can only support low energy dissipation, typically less than 10J. The correct operation of these two circuits, simultaneously, requires that the Zener clamping voltage is superior to the VDR conduction voltage, to guarantee the main dissipation energy in the VDR. Normally, the Zener diodes clamping voltage is defined for 125% of V_I.

The Zener diodes are connected after the NTC resistor connection, in order to perform a current limiter. The use of the Zener diodes, limits the transients to 125% V_I, but only if these have low energy. High energy transient blows the Zener diodes and will damage the converters. The voltage controller thyristor circuit has a characteristic identical to the VDR, but with a conduction voltage well defined and presents zero leakage current. The zener diodes are more expensive than the VDR and, therefore, are less utilized in domestic SMPS. The voltage controller thyristor is the most expensive protection circuit and is only used in expensive and ultra sensitive equipments.

IV. Susceptibility Analysis Of The SMPS

The susceptibility analysis of the SMPS (to voltage transients) is normally based in concepts developed to conventional loads, which are not valid to the SMPS. The standard CBEMA defines voltage tolerance curves based on the amplitude and duration of the transient voltage.

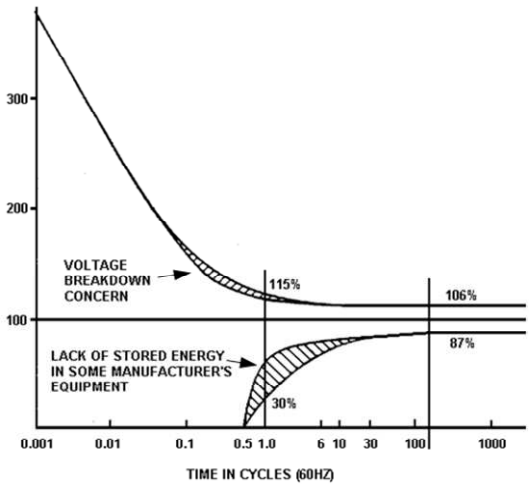

Fig. 11 CBEMA curve.

These curves have some drawbacks: they neither specify the slew-rate of the voltage transient nor refer voltage transients between neutral to ground and between phase to ground. These aspects are very important in the study of the susceptibility of the SMPS [1]. To realize the present analysis of the SMPS, the worst case is considered: the over voltage circuit protection utilizes only the VDR; the attenuation of the RFI filter for mains voltage transients is not considered (because the topologies used are very different in identically SMPS); the AC-DC converter is a diode bridge and capacitive filter (because this solution is extensively used and it is more sensitive than the boost rectifier). Some analysis requires some measures in a real power supply, therefore, a commercial PC SMPS is used.

A. Input filter and protections

In a protection circuit that uses only the VDR, the protection offered is strongly dependent to the mains network impedance and to the fuse time action (greater than 1ms when the current is 10X greater than the nominal value). We consider prejudicial to this circuit, transient voltages, between phase and neutral, v_{FN}, with a duration greater than 1ms and amplitude greater then >120% of V_I.

The susceptibility of the input filter is related with the C_X and C_Y capacitors. Considering the several tests, described in the standards IEC60384-14 and EN132400, is possible to define limits to the voltages between phase to neutral, v_{FN}, and neutral to ground, v_{NT}, which guaranteed the safety operation of the C_X and C_Y capacitors.

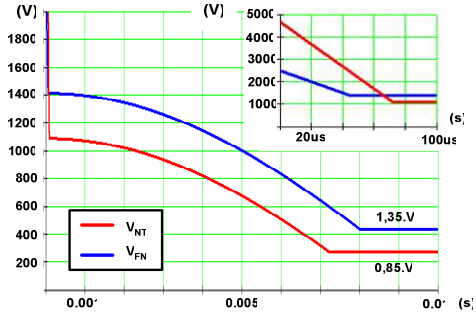

Fig. 12 v_{FN} and v_{NT} voltage limits which guaranteed the safety operation of the C_X and C_Y capacitors.

B. AC-DC converter

The presence of short duration over voltage transient between phase and neutral can provoke some several effects in the AC-DC converter: damage of the rectifier diodes due the current peak present in the charge of the capacitor C_A; damage of capacitor C_A due to the excess of charge; blowing of the input fuse due to the VDR conduction. Fig. 13 shows the influence of the dv/dt present in a notch, in the input current, i_I, of the SMPS.

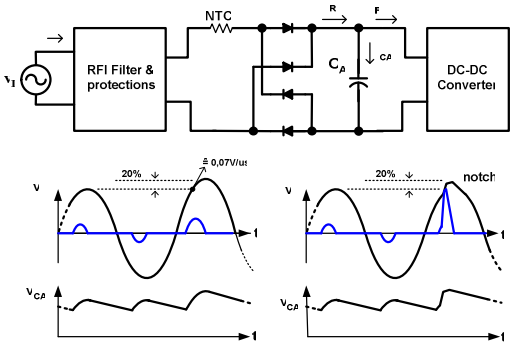

Fig. 13 Influence of the notch dv/dt in the SMPS input current, i_I.

Different SMPS have several differences in the rectifier diodes and capacitor C_A, this way, we not define a dv/dt prejudicial to the AC/DC converter, instead notches with 120% of V_I and with a duration of 10us to 10ms, (which normally results in high dv/dt transients) are considered.

C. DC-DC converter

In this section we present two analysis: influence of V_{CA} voltage transients in the output voltage and in the transformer magnetizing current; influence of the neutral to ground and phase to ground voltage transients in the output voltage. For the first analysis is necessary to define some parameters. As a reference SMPS, we consider the PC SMPS with the following specifications: VI_{RMS}=230V, V_O=5V, D_O=0.8, I_O=20A, f_S=66kHz and the output filter presented in Fig. 4 with ESR and ESL effects (measured in a impedance analyzer HP4294). For the output voltage controller we consider the circuit present in Fig.5 with V_{CTR}=10V. Due to the high ratio between the switching frequency and the output cutoff frequency, state space average models can be used in this analysis, Fig. 14.

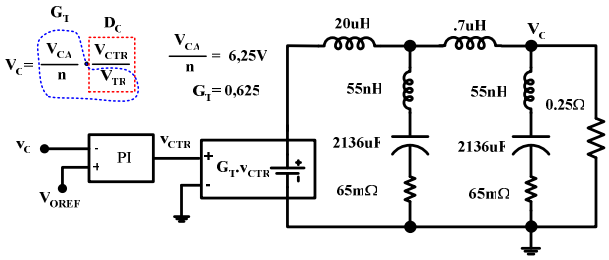

Fig. 14 State space average model of a SMPS.

The proportional integral controller is designed to guarantee a phase margin greater than 45 degrees (30 a 60 degrees - typical values in commercial SMPS). Fig. 15, shows the output voltage transient, when V_{CA} suffered a 20% voltage perturbation with two different slew rates, 1V/us and 0,1V/us.

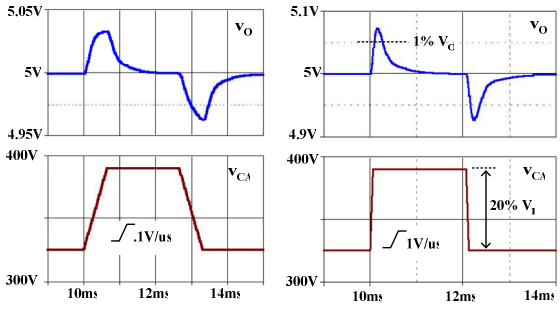

Fig. 15 Simulation results of a 20% V_{CA} voltage transient.

As represented in Fig. 15 a voltage transient in V_{CA} with a slew rate of 1V/us results in an output transient greater than 1% of V_O (typical value assumed in the design). This way, we consider as prejudicial to the DC-DC converter, voltage transients between phase and neutral with a dv/dt greater than 1V/us.

The peak of the magnetizing current is directly proportional to the V_{CA} voltage and to the output duty ratio. Considering this relations and the average model presented in Fig.5, the value of dv/dt of V_{CA} that provokes saturation of the transformer is 2V/us (when the perturbation in V_{CA} is grater than 25% of V_I).

Voltage transients in phase to ground and neutral to ground can provoke several effects in the output voltage of the SMPS due to the leakage capacitances present in the isolation transformer. To make this study, we create a high frequency impedance model, Fig. 16, obtained with an impedance meter HP4294 and a PC commercial SMPS.

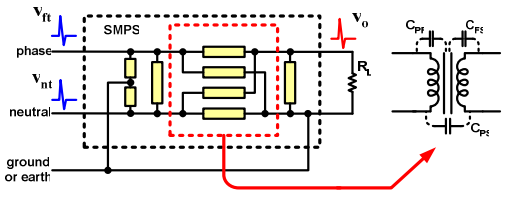

Fig. 16 High frequency impedances present in a SMPS.

The frequency characterization of those impedances results in two impedance models: (1) a model for common mode voltage transients (v_{ft}=v_{nt}); (2) a model for voltage transients between phase to ground and neutral to ground when v_{ft}≠v_{nt}. In the models presented in Fig. 17, the impedance of the transient source is despised and R_L is considerd to be infinite (worst case).

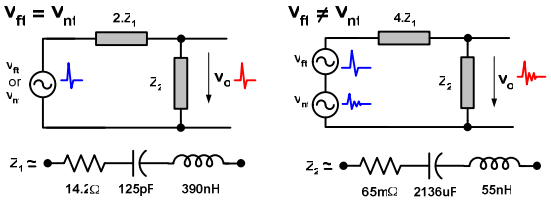

Fig. 17 High frequency impedance models for vft=vnt and vft≠vnt.

To verify the influence an impulsive voltage transients, v_{ft} or v_{nt}, into the output voltage, a voltage ramp waveform is applied into the common model input. Only this model is considered, because their attenuation is minor than the other one. To define a prejudicial dv/dt in v_{nt}, the ramp waveform dv/dt is adjusted in order to obtain 1% of V_O (50mV) in the output voltage transient.

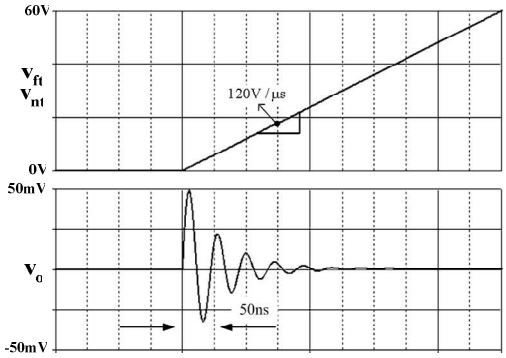

Fig. 18 Adjust of the ramp dv/dt, to obtain 50mV in the output voltage.

As we can see in Fig.18, an impulse voltage transient with a 120V/us dv/dt, present in neutral to ground voltage or phase to ground voltage results in significant transient in the output voltage. Different SMPS have different impedance models, which means that the value presented is only indicative of the dv/dt magnitude that can provoke disturbances in the output voltage of a SMPS. According to this we define two prejudicial events: neutral to ground voltage transient with a 120V/us dv/dt; and neutral to ground 50V spike transients with a 10us<t<10ms duration. The spike event is defined to allow a family of different high dv/dt present in neutral to ground voltage that may have significant impact in the output voltage.

When v_{ft} and v_{nt} impulsive voltage transients are different, they are also present in the phase to neutral and neutral to ground voltages. This way, it is not necessary to consider these transients because they are already included in the other transients defined as prejudicial.

Considering a sinusoidal transient in the input of the common mode model, it is possible to define the amplitude and frequency of this transient to result in a 50mV output voltage transient.

Considering the relation between the maximum dv/dt, amplitude and frequency of the oscillatory transient, it is possible to demonstrate, if the oscillation frequency is minor than 10MHz, that the maximum dv/dt is always greater than 120v/us. According to this, it is not necessary to consider the oscillatory transients as prejudicial, because their maximum dv/dt is already contemplated in the impulsive transient event.

D. Resume of prejudicial events

In resume, the susceptibility analysis of the SMPS results in four voltage events defined as prejudicial to the SMPS (TABLEI)

TABLE I

Event	**Characteristic**	**Impact in the SMPS**
Notch	phase to neutral > 120% V_I 10us < t < 10ms	damage the rectifier diodes, output voltage transients, blows of the input fuse
Spike	neutral to ground > 50V 10us < t < 10ms	output voltage transients
$\mathbf{v_{nt}}$ **Transient**	> 120V/us - neutral to ground	output voltage transients
$\mathbf{v_{fn}}$ **Transient**	> 1V/us - phase to neutral	output voltage transients, transformer saturation

V. CONCLUSIONS

The authors developed a systematic study of SMPS in order to understand the effects of power quality disturbances in the operation of electronic equipments. Five voltage events related with the susceptibility of the electronic equipment to voltage perturbations in the mains network were defined.

VI. REFERENCES

[1] Victor Anunciada, Hugo Ribeiro, “Power Quality as a Reliability Problem For Electronic Equipment”, ICREPQ05.

VII. BIOGRAPHIES

Hugo Ribeiro was born in Barquinha, Portugal, in 1975. In 1998 he received the degree of Electrical Engineer from Instituto Politécnico de Tomar. Is now a Research of Instituto de Telecomunicações - Instituto Superior Técnico - Lisboa.