Simulation and controller design of an Interline Power Flow Controller in EMTP RV

Sasan Salem (Member IEEE) and V. K. Sood (Fellow IEEE)

***Abstract* - An Interline Power Flow Controller (IPFC) is a converter-based FACTS controller for series compensation with capability of controlling power flow among multi-lines within the same corridor of the transmission line. It consists of two or more Voltage Source Converters (VSCs) with a common dc-link. Real power can be transferred via the common dc-link between the VSCs and each VSC is capable of exchanging reactive power with its own transmission system. In this paper, a control scheme of an IPFC system with two VSCs to compensate the impedances of two similarly dimensioned parallel transmission lines is presented. The model is simulated with the EMTP-RV program to demonstrate the system behavior of the IPFC.**

***Key words* - FACTS, SSSC, IPFC, Series Compensation**

I. Introduction

Flexible AC Transmission Systems (FACTS), based on either Voltage or Current Source Converters (VSC/CSC), can be used to control steady-state as well as dynamic/transient performance of the power system. Converter-based FACTS controllers, when compared to conventional switched capacitor/reactor and thyristor-based FACTS controllers such as Static Var Compensator (SVC) and Thyristor-controlled Series Capacitor (TCSC), have the advantage of generating/absorbing reactive power without the use of ac capacitors and reactors. In addition, converter-based FACTS controllers are capable of independently controlling both active and reactive power flow in the power system [1].

Series connected converter-based FACTS controllers include Static Synchronous Series Compensator (SSSC), Unified Power Flow Controller (UPFC), and Interline Power Flow Controller (IPFC). A SSSC is a series compensator with ability to operate in capacitive/inductive modes to improve system stability [3,4]. The UPFC includes a Static Synchronous compensator (STATCOM) and a SSSC that share a common dc-link. The IPFC consists of two or more SSSC with a common dc-link; so, each SSSC contains a VSC that is in series with the transmission line through a coupling transformer, and injects a voltage - with controllable magnitude and phase angle - into the line. IPFCs provide independent control of reactive power of each individual line, while active power could be transferred via the dc-link between the compensated lines. An IPFC can also be used to equalize active/reactive power between transmission lines, and transfer power from overloaded lines to under-loaded lines [2].

This work was supported by Natural Sciences and Engineering Research Council of Canada under Grant 4518.

S. Salem was with the Department of Electrical Engineering, Concordia University, Montreal, QC, H3G 1M8, (e-mail: s_salem@ece.concordia.ca).
V.K.Sood is with the Department of Electrical Engineering, Concordia University, Montreal, QC, H3G 1M8, Canada (e-mail: vijay@ece.concordia.ca).

Presented at the International Conference on Power Systems Transients (IPST'07) in Lyon, France on June 4-7, 2007

Since its introduction in 1998 [2], relatively only a few research papers exist about IPFC configurations as compared to other types of FACTS controllers. In [5,6,7], the control design and steady-state operation of an IPFC is presented. In [8,9], the utilization and steady-state operation of the ±200 MVA Convertible Static Compensator (CSC) installed by New York Power Authority at its Marcy 345 kV substation is described. The CSC is capable of controlling voltage, increasing power transfer and enhancing the dynamic performance of the power system. It includes two VSCs, and by means of different circuit configurations, can function either as a STATCOM, SSSC, UPFC or IPFC.

This paper presents EMTP-RV based models of the IPFC which are based on [1,2]. In section II, the model of a 3-level Neutral-Point-Clamped (NPC) VSC - used as the basic building block of an IPFC - is presented. In section III, the IPFC control scheme for two identical transmission lines is studied. The controller is designed to regulate the transmission line impedance (R and X) and balance the dc-link capacitor voltages of the IPFC. The simulation results are used to assess the ability of the IPFC to regulate the transmission line impedance in the power system.

II. Methodology

A. Power Circuit

An IPFC (Fig. 1) uses two or more VSCs that share a common dc-link. Each VSC injects a voltage - with controllable amplitude and phase angle - into the power transmission line through a coupling transformer. Each VSC provides series reactive power compensation for an individual line and it can also supply/absorb active power to/from the common dc-link [1,2]. Thus, an IPFC has an additional degree of freedom to control active power flow in the power system when compared to a traditional compensator. This capability makes it possible to transfer power from over- to under-loaded lines, reduce the line resistive voltage drop, and improve the stability of the power system.

The coupling transformer primary windings of the master and slave converters are (pseudo) star-connected while their secondary windings are connected in series with each phase of the transmission line. In addition, the transformer leakage reactance allows regulation of the output voltage magnitude and phase angle, with respect to the transmission line current, and offers stable control of the VSC power output.

Fig. 1 shows the scheme of an IPFC having two VSCs. In this scheme, a master control system is used to compensate both resistive and inductive impedances of the Line 1 power system, and the slave control system is used to regulate the reactance of Line 2 and maintain the common dc-link voltage.

B. Converter model

The VSC is the fundamental building block of the IPFC. Various types of pulse-width modulation (PWM) or multi-pulse con-

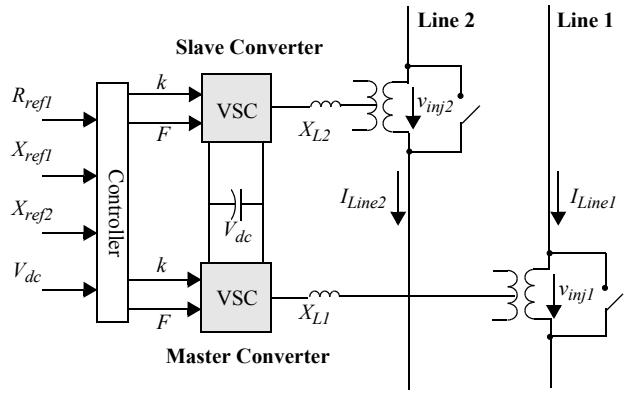

Fig. 1. Schematic of an IPFC

verters [13] i.e. multi-level converters, are feasible for power conversion. Irrespective of the VSC topology, a large number of switches must be connected in series to provide the required valve voltage rating. Therefore, appropriate snubber circuits are used to minimize the switching stresses on each device. In this study, a 3-level Neutral Point Clamped (NPC) PWM VSC is employed. This topology is suitable for high power applications and, when compared to a 2-level topology, it produces fewer harmonics, has smaller dc capacitors, lower switch blocking voltages and lower switching losses [10]. The drawbacks, however, of the 3-level NPC topology are: requirement for a large number of switches, different duties for semiconductors switches and a requirement for balancing the dc capacitor voltages.

For the converter model, a 3-phase 3-level NPC VSC with a switching frequency of 900 Hz is used. Each converter consists of 12 valves and 2 dc capacitors C1 and C2. Each valve consists of a switch with turn-off capability and an anti-parallel diode. The diodes ensure bi-directional current flow and, therefore, the converter can operate in either rectifier or inverter modes.

Fig. 3 shows the current and voltage in a converter switch. The switch model consists of two snubber circuits to limit *dv/dt* and *di/dt* in the VSC switches.

If the VSC losses are neglected, the injected voltage from the

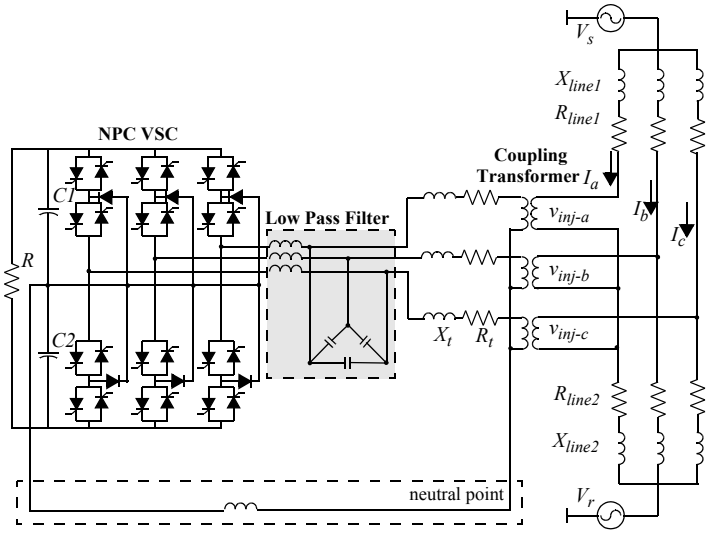

Fig. 2. Schematic of 3-level Neutral Point Clamped VSC

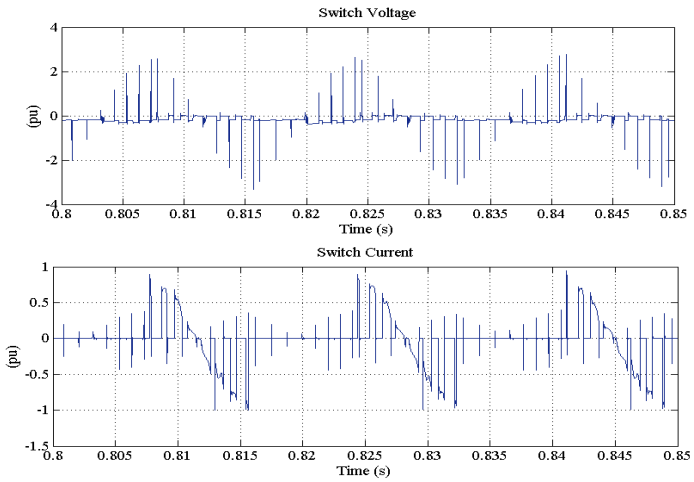

Fig. 3. Examples of switch current and voltage

converter can be set to either lead or lag the transmission line current by exactly 90°, depending upon the requirement of the reactive power. The neutral point of the coupling transformer and dc-link of the slave system VSC are connected with a large inductor L_o. This path is employed to equalize the dc capacitor voltages of the VSC. However, the master converter system of the IPFC (that regulates the resistive and inductive impedances of the transmission line) has no such connection between the neutral of the coupling transformer and dc-link of the IPFC (Fig. 2).

Since the output voltage of the VSC contains high-order harmonic components, low-pass and tuned filters are used to provide a clean sinusoidal waveform in both master/slave systems.

III. Control Scheme of IPFC

The IPFC is designed to maintain the impedance characteristic of the two transmission lines. The IPFC consists of two converter systems: (a) a master converter system that is capable of regulating both resistive and inductive impedances of Line 1; and, (b) a slave converter system that regulates Line 2 reactance and keeps the common dc-link voltage of the VSC at a desired level. So, each VSC is independently controllable.

Balancing the dc voltages V_{dc1} and V_{dc2} on the capacitors C1 and C2 respectively, is an important concern in multi-level converters (Fig. 2). Uneven voltage charging on the capacitors can cause over-voltages on the switching devices and that could be destructive for them. The problem may be solved by either (a) a modified PWM switching pattern [11], (b) by a voltage regulator for each level using an additional charge balancing leg [12], or (c) separate dc sources. In order to maintain an equal voltage in the dc-side, the voltage of the neutral point must be regulated. Here, based on [15], the zero sequence current i_0 is used to equalize voltages on the dc-link capacitors of the VSC.

Fig. 4 shows the control diagram of the slave IPFC system. It consists of three control loops: (a) for regulating the injected reactance, (b) for regulating the dc-link voltage, and (c) for balancing the voltages on the dc side capacitors.

Block 1 is used to transform the 3-phase voltages (v_{inj_a}, v_{inj_b}, v_{inj_c}) into the α–β–0 coordinates and obtain the positive sequence voltage V_{inj_α}, as per (1).

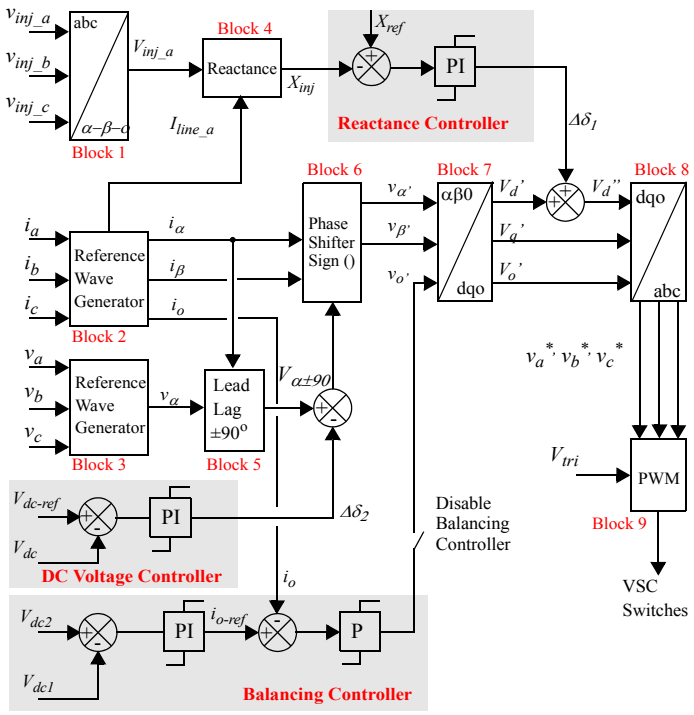

Fig. 4. IPFC slave converter system controller

$$\begin{bmatrix} v_{inj-\alpha} \\ v_{inj-\beta} \\ v_{inj-o} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{-1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} v_{inj-a} \\ v_{inj-b} \\ v_{inj-c} \end{bmatrix} \quad (1)$$

Block 2 is used to transform the 3-phase line currents (i_a, i_b and i_c) to the *α–β–0* coordinates using the RWG block; this block will be described in more detail later. For generating reference waveforms for control purposes, the 3-phase currents are transformed from *a-b-c* to *α–β–0* coordinates, by using (2). The i_α and i_β components are fed to the Phase Shifter (Block 6) while the i_0 component is fed to the Balancing Controller. If the 3-phase current waveforms in *a-b-c* coordinates are balanced, then i_α and i_β components are sinusoidal and orthogonal, and i_0 represents the zero sequence component.

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_o \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{-1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (2)$$

Block 3 is used to transform the 3-phase line voltages v_a, v_b and v_c to the v_α, v_β and v_0 coordinates using another RWG block with a transformation similar to (2). Only the v_α component of this block is fed to the Lead/Lag Block (Block 5); the two other outputs v_β and v_0 are not required.

Block 4 receives the positive sequence of the injected voltage V_{inj-a} from Block 1 and the positive sequence of the line current I_{line-a} from Block 2. It then computes the injected line reactance X_{inj} and sends it to the Reactance Controller.

Block 5 (Lead/Lag Block) receives the reference signal of the line voltage v_α from Block 3 and the reference signal of the line current i_α from Block 2 and computes the 90° phase shift and its sign, whether leading (+1) or lagging (-1) of this angular displacement. This information is summed with the output angle $\Delta\delta_2$ from the DC Voltage Controller.

Block 6 (Phase Shifter Block) receives the i_α and i_β reference signals from Block 2 (RWG). These signals are modulated by the sum of the signals from the DC Voltage Controller and Lead/Lag Blocks to generate the modified reference signals v_α' and v_β'.

Block 7 is the *α–β–0* to d-q-0 transformation block used to convert the input 3-phase reference components v_α', v_β' and v_0' to v_d', v_q' and v_0' coordinate system by using (3). These signals are then fed to the PWM trigger unit (Block 9) which is described in more detail later.

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} \cos wt & -\sin wt & 1 \\ \cos\left(wt - \frac{2\pi}{3}\right) & -\sin\left(wt - \frac{2\pi}{3}\right) & 1 \\ \cos\left(wt + \frac{2\pi}{3}\right) & -\sin\left(wt + \frac{2\pi}{3}\right) & 1 \end{bmatrix} \begin{bmatrix} V_d \\ V_q \\ V_0 \end{bmatrix} \quad (3)$$

To regulate the injected voltage amplitude, the Reactance Controller is employed. The injected reactance X_{inj} is compared to a reference reactance value X_{ref} and a PI controller is used to amplify the error. The resultant is added to the *d*-component of the desired reference waveform V_d', and that modulates the reference signals v_a*, v_b* and v_c* of the PWM controller. The active power exchange is regulated by the phase angle φ of the injected voltage in response to an error in the dc-link voltage via a PI controller. The dc-link voltage V_{dc} is maintained constant and is equal to $V_{dc\text{-}ref}$, and by changing the converter dc/ac gain, the injected voltage amplitude is controlled.

The slave control system must not only absorb enough active power to compensate for the VSC losses, but it must also supply the required active power for the master system. Consequently, the slave system provides a constant dc voltage for the master system and acts as an Energy Storage System (ESS).

Fig. 5 shows the overall control structure of the master IPFC system. This block diagram is similar to the block diagram of the slave IPFC system, and has many of the same blocks except for two major differences: (a) the dc voltage controller and (b) the balancing controller. Since the dc-link voltage is controlled by the slave system, the dc voltage controller and balancing controller are no longer needed. However, here two control loops are required to regulate the *d*- and *q*-components in the synchronous reference frame in order to regulate both the reactance and resistance of the Line 1.

To regulate the injected reactance, a Reactance Controller is used. The injected reactance $X_{inj\text{-}1}$ is compared to a reference

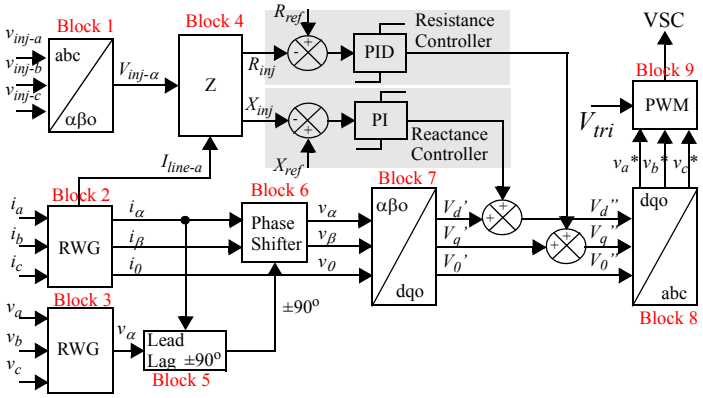

Fig. 5. IPFC master converter system controller

value X_{ref} and the error is fed to a PI controller. The resultant is added to the d-component of the desired reference waveform v_d', to generate v_d''. Similarly, the injected resistance - defined as the real part of (V_{inj}/I_{line}) - is regulated by a Resistance Controller. For this purpose, the injected resistance R_{inj-1} is compared to reference value R_{ref} and the error is amplified by a PID controller. The result is added to the q-component of the desired waveform V_q' and generates V_q''. In this particular case, a PID controller is applied to reduce the oscillations of the time response.

Block 8 receives the modified *d*- and *q*-components V_d'' and V_q'' and transforms them to 3-phase coordinates; these signals are used as the reference signals v_a^*, v_b^*, and v_c^* of the PWM controller. And the PWM Block provides firing pulses for the 3-level NPC VSC switches. Since the master converter system regulates the dc-link voltage to a fixed level, theoretically it is capable of injecting a voltage with a phase angle in the range of 0-360°.

C. Reference Wave Generator (RWG) (Fig. 6)

The 3-phase transmission line currents are used as the reference signals by the controller to generate either lagging or leading voltages by a 90° phase shift with respect to the transmission line current. A RWG was introduced [14] to generate clean synchronizing signals by a technique similar to a Phase Locked Loop (PLL). The synchronizing signals are based on symmetrical component transformation. The transmission line currents i_a, i_b, and i_c are transformed into positive i_α, negative i_β and zero i_0 sequence components, as indicated in (1). Subsequently, a normalizing and wave-shaping block is used to obtain the original waveform even under severe system distortion conditions. A delay compensation block is used to compensate the delay caused by the previous block. The delay result of five iterations for a 60 Hz system and a 10 micro-second time-step is 1.08°. The output reference waves are synchronized continuously with the original input waveforms (that could be distorted or contain harmonics). This method, when compared to a conventional PLL, has a fast response to any distortion and suffers very little transient delay.

D. PWM Block

This block provides the firing pulses for the 3-level VSC switches. The 3-phase input to the PWM block (Block 9) is:

$$V_n = V_m \cdot \sin(wt + \varphi_n) \qquad (5)$$

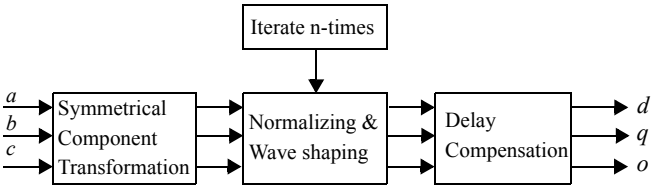

Fig. 6. Block diagram of Reference Wave Generator (RWG) [14]

Where $n = \{a,b,c\}$ and V_m is the peak value of the waveform.

The PWM also uses two 900 Hz triangular carrier input waves V_{tri-H} and V_{tri-L}. The modulation index k is defined as:

$$k = \frac{V_m}{V_{tri}} \qquad (6)$$

Where V_{tri} is the maximum value of the two triangle carrier waveforms. The "φ" indicates the desired phase angle of the 3-phase waveform in the PWM block. The 3-phase waveforms v_n are compared to two triangular waveforms $\pm V_{tri}$ to produce the firing pulses for the 12 switches of the VSC. A single-arm version for generating these switching function type waveforms for the four switches (S_{a1}, S_{a2}, S_{a3}, and S_{a4}) per a-phase or arm-a of the VSC is shown in Fig. 7. The 3-level output voltage waveforms are created according to the rules below:

- If $v_a > V_{tri-H}$, S_{a1} is ON, else S_{a1} is OFF.
- If $v_a > V_{tri-L}$, S_{a2} is ON, else S_{a2} is OFF.
- Only two series devices can be ON at the same time, so:
  - S_{a1} and S_{a3} have opposite functions, and
  - S_{a2} and S_{a4} have opposite functions.

E. Balancing Controller

The zero sequence current is used to balance the voltages of the dc-link capacitors in a 3-level Neutral-Point-Clamped (NPC) VSC [15]. This is achieved by connecting the neutral points of the slave system's coupling transformer and the dc-link of the IPFC through a large inductor L_o (Fig. 2).

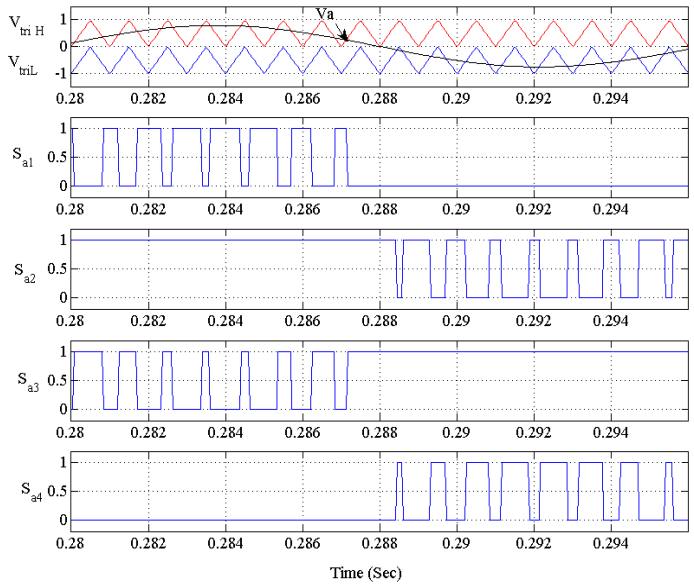

Fig. 7. Modulation wave and switching signals of a 3-level PWM

If the dc-link capacitor voltages are unbalanced, a zero sequence current is generated. The generated zero sequence current $i_{0\text{-}ref}$ is compared to the actual zero sequence current of the converter's output i_0 (neutral points of the coupling transformer), and amplified by a proportional controller. The zero sequence component v_0' joins v_α' and v_β' components of the controller and are then converted to the 3-phase reference components v_a^*, v_b^* and v_c^* (Fig. 4) that are used as the reference signals for the PWM controller. Consequently, the Balancing controller generates a zero sequence current that passes through the connection of the neutral point of the coupling transformer and the dc-link to equalize the voltage on the two capacitors.

IV. Simulation Results

The simulated power system (Fig. 8), modelled with EMTP RV, consists of two identical transmission systems; their characteristics are given in the Appendix. In the master system, the controller is designed to compensate 0.4 pu of the transmission line reactance and 0.2 pu of transmission line resistance. In the slave system, the controller is designed to compensate 0.4 pu of the transmission line reactance and to keep the dc-link voltage of the IPFC constant. Three test results are presented below to evaluate the performance of the related control systems.

F. Impact of step change in reference values of the injected reactance and resistance on IPFC performance (Fig. 9)

The dynamic behavior of the controller is verified by applying a 0.2 pu step change in the reference values of injected reactance and resistance in the master system, and a 0.2 pu step change in the reference values of the injected reactance and dc-link voltage in slave system. The IPFC is designed to compensate 0.4 pu of the line reactance and 0.2 pu of the line resistance in the master system and 0.4 pu of the transmission line reactance in the slave system. Therefore, X_{ref}= 0.4 pu, X_{inj} = -0.1 pu and R_{ref}= 0.2 pu, R_{inj} = -0.01 pu (where X_{line} = 0.25 pu, and R_{line}= 0.05 pu). The dc-link voltage is 1 pu at 10 kV.

Four different step disturbances are applied consecutively, as follows:

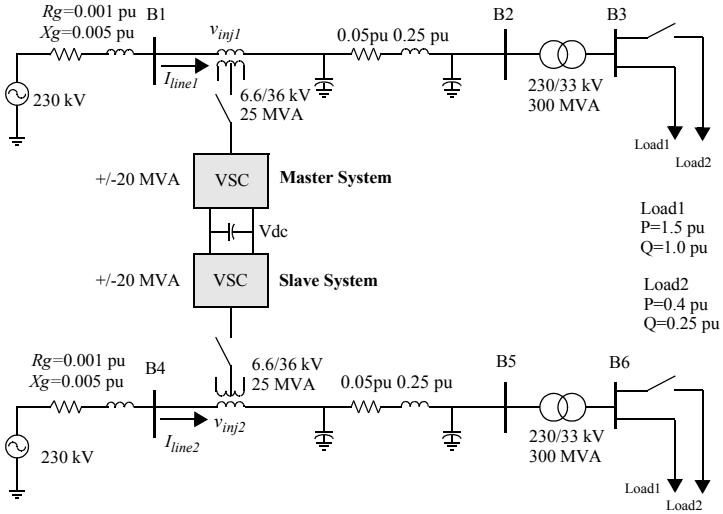

Fig. 8. Single line diagram of the power system used for simulation

1. Between 0.5-0.8 s, a 0.2 pu step change in the dc link voltage reference from 0.4 to 0.48 pu is applied,
2. Between 1.0-1.3 s, a 0.2 pu step change in the injected reactance reference from -0.1 to -0.12 pu into Line 1 is applied,
3. Between 1.5-1.8 s, a 0.2 pu step change in the injected resistance reference from -0.1 to -0.12 pu into Line 2 is applied,
4. Between 2.1-2.5 s, a 0.15 pu step from -0.01 to -0.015 pu in injected reactance reference into Line 1 is applied.

Results from the above perturbations are shown in Fig. 9.

Fig. 9a shows a 0.2 pu step change in dc-link voltage reference of the IPFC applied from 500-800 ms i.e. the dc-link voltage reference increases from 0.4-0.48 pu. The dynamic step response is stable and takes 100 ms for settling down. The step changes in reference value of injected reactance and resistance in Lines 1 and 2 cause only a small transitory variation in dc-link voltage. Variation of injected resistance R_{inj} has a greater effect on the dc-link voltage, since it extracts active power from the dc-link.

Fig. 9b shows the step change in the reactance of Line 1 and its controller response. At 500 ms, the dc-link voltage step change causes a transient that is damped after 200 ms. At 1 s, the step change in reference of the reactance in Line 1 is applied and the injected reactance is changed from -0.1 pu to -0.12 pu. The dynamic behavior is stable and damps out in 200 ms.

Fig. 9c shows the reactance reference step and the controller response in Line 2. At 500 ms, the dc-link voltage step change causes a transient that is damped after 100 ms. At 1.5 s the reactance reference step change is applied and the injected reactance is changed from -0.1 pu to -0.12 pu. The dynamic behavior is stable and takes about 100 ms for the settling time.

Fig. 9d illustrates the resistance reference step and the response of the controller in Line 1. At 2.1 s the step change is applied and the injected resistance is changed from -0.01 pu to -0.015 pu. The dynamic behavior is stable and takes about 200 ms for the settling time. The injected resistance controller is sensitive to any disturbances within the controller system.

Fig. 9e shows the injected ac voltage in Line 1. By increasing the amount of compensation by 0.2 pu between 0.9-1.2 s, the peak value of the injected voltage increases from 0.1 to 0.12 pu. Fig. 9f shows the injected voltage in Line 2. By increasing the degree of compensation by 0.2 pu between 1.5-1.8 s, the peak value of the injected voltage increases from 0.1 pu to 0.12 pu.

Fig. 9g illustrates the phase angle between the injected voltage and the transmission Line current in phase (a) of Lines 1 and 2. The phase angle in Line 1 is around 95^o that shows the active power injection into Line 1. The phase angle in Line 2 is around 83^o. At 1.7 s, when the reference value of injected resistance in the Line 1 is stepped down, the phase angle in Line 2 decreases to 80^o to transfer more active power from Line 2 to Line 1.

Fig. 9h shows the transmission line currents of Line 1 and Line 2. The step change of the dc-link voltage at 500 ms causes a transient in both lines. In Line 1, the settling time is longer than Line 2. The increment of the injected reactance at 1.0 s in Line 1 and 1.5 s in Line 2 increases the transmission line currents. At 2.1 s, when the resistance reference step down is applied, the transmission Line 1 current increases.

G. Impact of load variation on IPFC performance

The dynamic behavior of the IPFC is verified by varying the receiving-end load in Lines 1 and 2 (Fig.10). Between 500-800 ms, a load with active power P = 0.4 pu and reactive power Q = 0.25 pu is added to the master Line 1. And between 1.0-1.3 s, a load with P = 0.4 pu and Q = 0.25 pu is added to the slave Line 2.

Fig. 10a illustrates the dc-link voltage of the IPFC. The dc-link voltage remains virtually constant, apart from some transients that last for about 100 ms when the loads are changed. Fig. 10b shows the injected reactance into Line 1. Adding Load 2 causes a transient with a relatively high overshoot but is damped in 100 ms. In steady state, the injected reactance stays constant. Fig. 10c shows the injected reactance into transmission Line 2. Adding Load 2 into Line 2 causes a transient that is damped in 100 ms. In steady state, the injected reactance stays constant. The slave control system is slightly better damped to a load variation than the master control system. Fig. 10d illustrates the injected resistance into Line 1 and Line 2. The injected resistance into Line 1 is constant since the master system regulates the injected resistance and compensates a portion of the Line 1 resistance. However, the injected resistance into Line 2 is not controlled by the slave system, and any increase in the current results in more losses in the converter as is demonstrated by the R_{inj} into Line 2. Fig. 10e illustrates the current in Line 1 and its rms value; due to the load variation between 0.5-0.8 s, the current increases around 0.2 pu. Fig. 10f shows the behavior of the voltage, and its rms value, injected into Line 1. Due to an increasing load, the injected voltage rises to keep the injected impedance constant. Fig. 10g shows the current, and its rms value, in Line 2. Due to load variation between 1.0-1.3 s, a current increase of about 0.2 pu is observed. Fig. 10h shows the injected voltage, and its rms value, into Line 2. Due to the increasing load; the injected voltage rises by 0.2 pu to keep the injected impedance constant.

H. Impact of dc capacitor voltage balancing circuit

The dc capacitor voltage balancing circuit behavior for two disturbances is shown Fig. 11. First, a 0.2 pu step change in its reference value is applied between 1.0-1.5 s. And second, the dc voltage balancing circuit is disabled from 2.25-2.75 s.

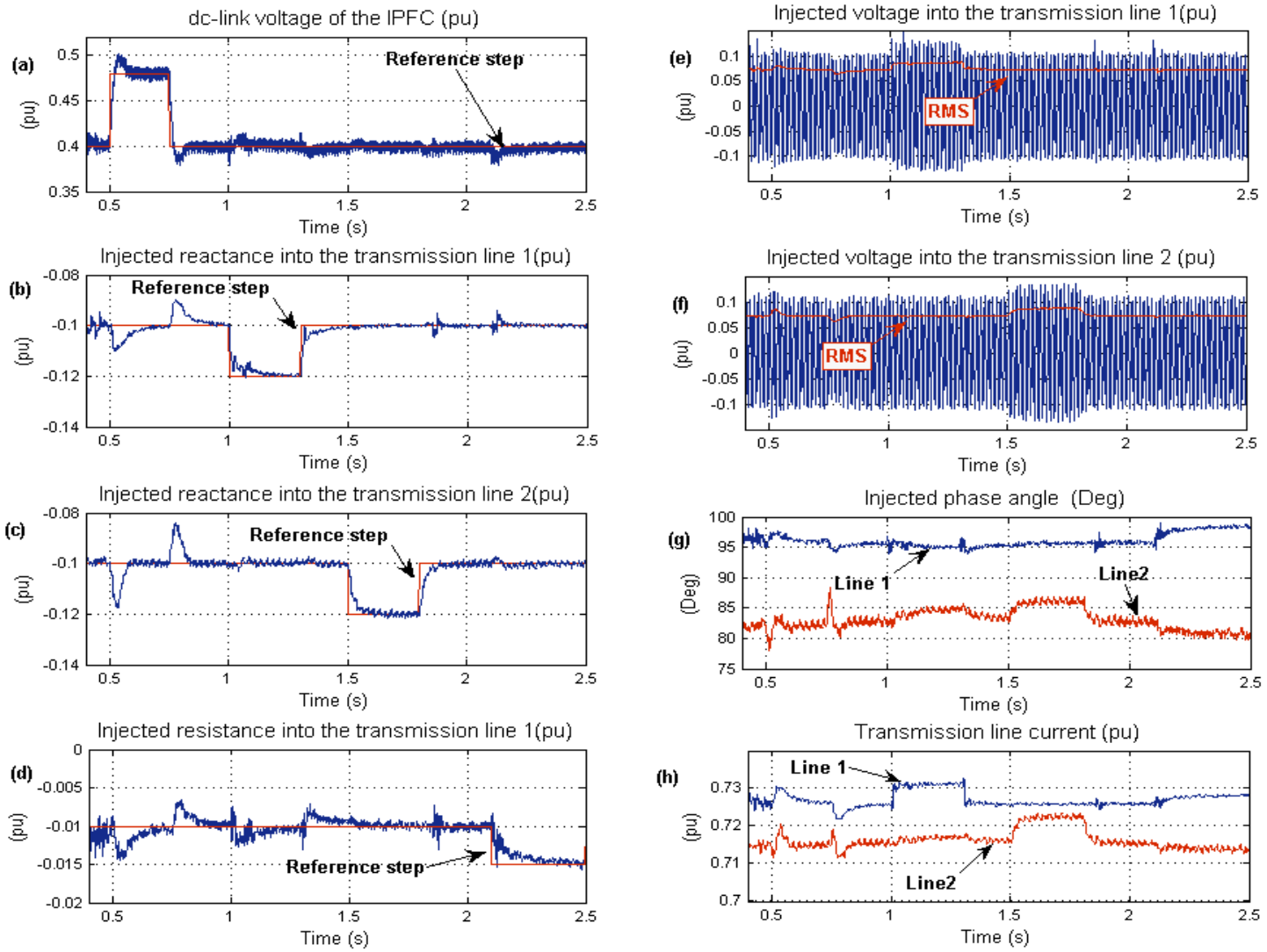

Fig. 9. System response to step change of the controller reference values (a) Dc-link voltage (b) Injected reactance into the Line 1 (c) Injected reactance into the Line 2 (d) Injected resistance into the Line 1 (e) Injected voltage into the Line 1 (f) Injected voltage into the Line 2 (g) Phase angle between the injected voltage and the transmission line current (h) Receiving-end reactive power in Line 1 and Line 2.

Fig. 11a shows the dynamic response of the controller to the reference step change in the dc voltage. The dc voltage difference is able to track the reference value within 200 ms. When the balancing controller is disabled (from 2.25-2.75 s), a small error is observed between the actual value and the reference value and shows the influence of the balancing controller to equalize the dc voltages V_{dc1} and V_{dc2}. Fig. 11b, the reference step change (1.0-1.5 s) causes the two dc capacitor voltages V_{dc1} and V_{dc2} to be affected in opposite manners such that the net influence of the step will be negated on the overall dc voltage, as shown in Fig. 11b. The disabling of the balancing controller (from 2.25-2.75 s) shows the influence of the balancing controller to equalize the dc voltages V_{dc1} and V_{dc2}. Fig. 11c shows the zero sequence current into the VSC; the dynamic response follows the reference step. Fig. 11d shows that the net dc-link voltage is virtually stable although some high frequency oscillations are observed. Fig. 11e shows the injected reactance into the transmission line. As expected, very little disturbance is observed due to the step change. Fig. 11f shows the phase angle of the injected voltage into the transmission line. The angle in the master system is stable although some high frequency oscillations are observed. In the slave system, the angle decreases during the reference step.

V. Conclusion

The study of an IPFC system with two parallel lines has demonstrated the flexible control of active/reactive power to assist in the transmission system. The behavior of the system under various transient and load changes at the receiving-end of the transmission system are presented and analyzed. The results of an IPFC system with two 3-level NPC VSCs in EMTP-RV have validated the conceptual design presented in [1,2]. The simulation results demonstrate the capability of the IPFC in compensating both resistance and reactance of the transmission line, and maintaining the dc-link voltage of the IPFC. A balancing circuit based on zero sequence current is employed to equalise the dc link capacitor voltages.

VI. Appendix

System data is referred to a per unit system with P_{base}=100 MVA and V_{base}=230 kV. The value of C_{dc}= 30,000 micro-Farad. The controller parameters are:

For Line 1:

Reactance controller K_p = 10 and K_i = 220

Resistance Controller K_p = 4, K_i = 80, and K_d = 0.005

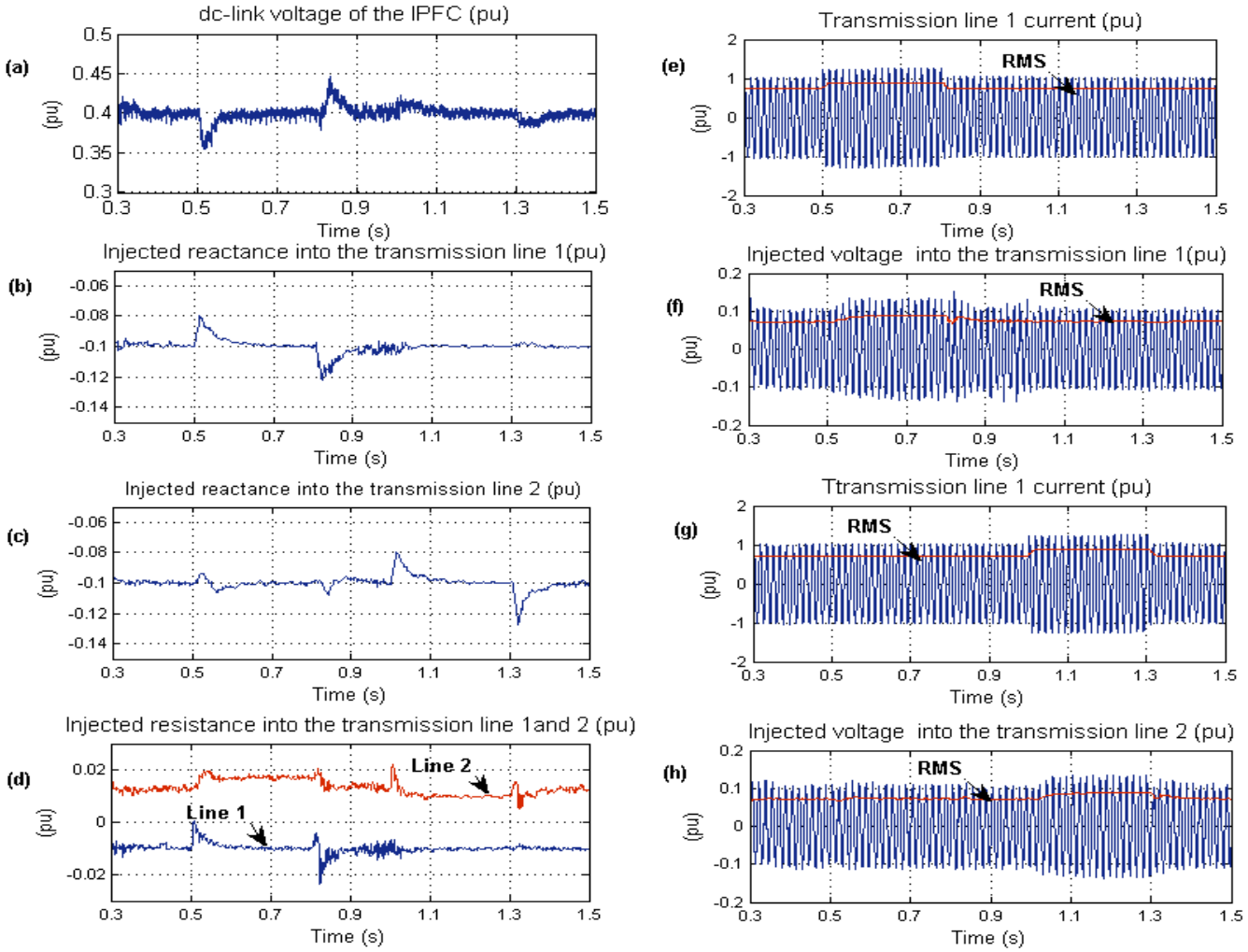

Fig. 10. Impact of load variation (a) Dc-link voltage (b) Injected reactance into the Line 1 (c) Injected reactance into the Line 2 (d) Injected resistance into the Lines 1 and 2 (e) Current in Transmission Line 1 (f) Current in Transmission Line 2 (g) Injected voltage into the Line 1 (h) Injected voltage into the Line 2

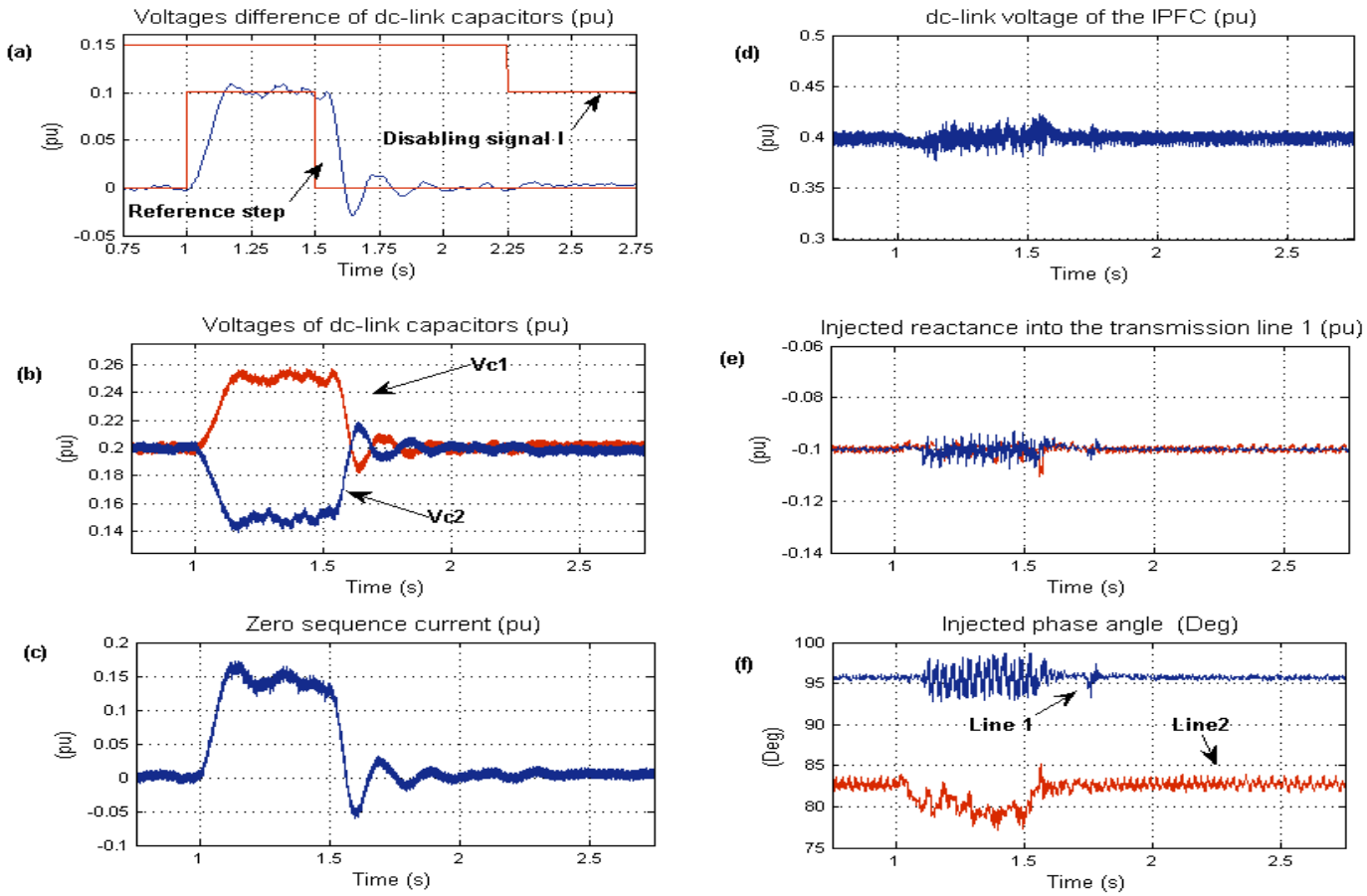

Fig. 11. Impact of dc voltage balancing circuit (a) Voltage difference of two dc-link capacitors (b) dc-link voltages V_{dc1} and V_{dc2} (c) Zero sequence current (d) Net dc-link voltage (V_{dc1}+V_{dc2}) (e) Injected reactance into the transmission line (f) Phase angle of injected voltage

For Line 2:

Reactance Controller $K_p = 2$ and $K_i = 250$.

DC-link voltage regulator $K_p = 80$ and $K_i = 2500$.

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