Modeling, Control and Simulation of a Chain Link STATCOM in EMTP-RV

N. M. Shah, V. K. Sood, V. Ramachandran

Abstract--This paper describes an alternative STATic synchronous COMpensator (STATCOM), by connecting a number of Gate Turn Off (GTO) thyristor converters in series on the ac side of the system. Each GTO converter forms one 'link' of a 1-phase, full-bridge Voltage-Source-Converter (VSC) and is referred to as a 'Chain Link Converter' (CLC). Each GTO of a CLS, is switched 'ON/OFF' only once per cycle of the fundamental frequency by using a Sinusoidal Pulse Width Modulation (SPWM) technique. Approximate models of a 3-phase Chain Link STATCOM (CLS) using *dq*-transformation are used to design two controllers for controlling reactive current and ac voltage to stabilize the system voltage at the Point of Common Coupling (PCC). A novel technique, called the Rotated Gate Signal Pattern (RGSP), is used for balancing the voltages of the link dc capacitors. The performance investigation of the CLS system when used in a radial line is carried out under steady- and transient-state operating conditions by means of the simulation package; EMTP-RV and the results are presented.

Keywords: Chain link converter, VSC, SVC, STATCOM, FACTS, EMTP-RV.

I. INTRODUCTION

An advanced static VAR compensator (ASVC), using a VSC, popularly known as a STATCOM, has been acknowledged as the next-generation reactive power controller in power systems. This controller's capability is analogous to that of a rotating synchronous condenser and it is used in a similar way to provide dynamic voltage compensation, increased transient stability and damping for the power transmission system [1, 3]. Several STATCOMs, based on GTOs and a special zigzag transformer, have been put into operation [4, 5]. These STATCOMs have advantages over conventional SVCs of lower harmonic generation, improved performance and smaller reactor size. However, zigzag transformers used in these STATCOMs are bulky, expensive and as yet unreliable.

An alternative method to eliminate the zigzag transformer and to increase the rating with a corresponding reduction in harmonics is to use a multilevel converter [6], which produces a 'multi-stepped' output voltage waveform. A relatively new multilevel converter application has been developed by connecting a number of GTO based VSCs in series to form a chain [1, 7, 8]. This chain link STATCOM (CLS) has advantages compared to more conventional versions of the STATCOM i.e. good harmonic performance, lower losses, reduced number of diodes-capacitors and lower cost. Moreover, the packaging and physical layout is much easier due to a modular structure. The first CLS application is in service in the National Grid Company, East Claydon substation, UK, since mid 1990s [8].

A 3-phase CLS having 3-links per phase is presented in this paper. Three links are used here, since the model exemplifies an adequate degree of complexity without incurring the excessive computational burden of a larger number of links. The proposed CLS, with its controller, is modeled using *dq*-transformation and is connected at the end of a radial transmission line, and across the load to support the voltage at the PCC. This CLS system is simulated with the digital simulation software package EMTP-RV for performance investigation. Results of the simulation tests in steady- and transient-states are presented.

II. CHAIN LINK STATCOM: THEORY

A. Basic circuit arrangement and principle of operation

A CLS comprises of a number of GTO converter 'links' connected in series on their ac side to form a separate 'chain' per phase (Fig. 1a). Each 'link' is a 1-phase, 3-level, full bridge VSC comprised of four GTO-diode pairs as switches and an independent self-controlled dc capacitor, C_{dc} for energy storage (Fig. 2a). In this arrangement, the dc capacitors are floating with the voltage, V_{dc} on each of them. Consequently, no real power needs to be supplied, other than the losses that are represented by the parallel resistor, R_{dc}. The principle of operation of a CLS is explained in [9]. By switching each GTO-diode pair "ON/OFF" once per cycle of the fundamental frequency, a 3-level output voltage waveform is synthesized for each link (Fig. 2c). Therefore, with N links in series (where N is a positive integer), the CLS output voltage contains ($2N$+1) voltage levels (Fig. 1b) that can give a good approximation to a sine wave. The total (fundamental frequency) output voltage of the CLS is thus the sum of the individual link ac voltages (Fig. 1b), and similarly for the total CLS VAr rating.

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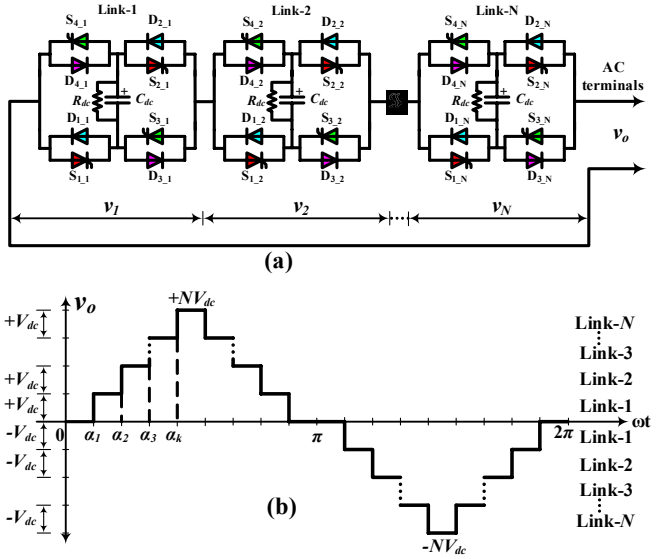

Fig. 1. (a) Basic circuit arrangement and (b) (2*N*+1) level output phase voltage waveform of a CLS with '*N*' links per phase.

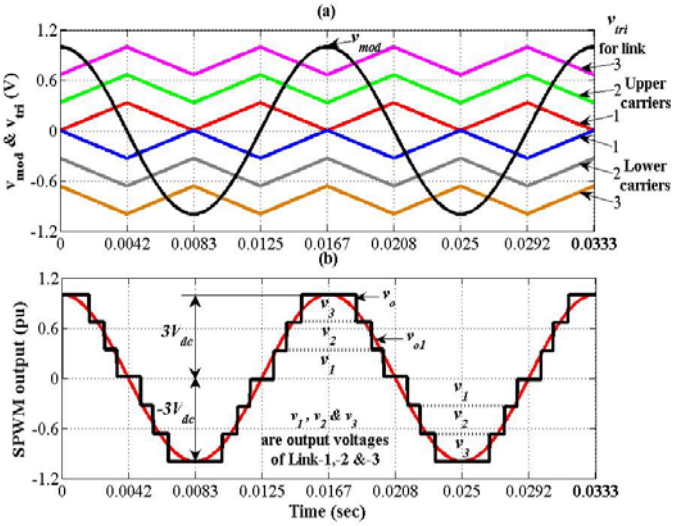

Fig. 3. (a) SPWM technique and (b) 7-level output phase voltage and its fundamental frequency component of a CLS with 3-links per phase.

B. Gating strategy

In a CLS, a good approximation of the sinusoidal voltage waveform in the CLS can be produced by a set of triangular carrier signals and a sinusoidal modulating signal using a technique known as "Sinusoidal Pulse Width Modulation (SPWM)". The principle of switching is similar to that of a 1-phase, 2-level converter [10]. For the CLS, there are two triangular carriers per link and one modulating signal for all the links. Therefore, in a CLS having *N*-links, a total of 2*N* triangular carriers are required [9]. The frequency of the triangular carriers (f_c) is selected to be twice the fundamental (or system) frequency (f_o) so that each GTO-diode switches "ON/OFF" only once per cycle of the fundamental frequency. The frequency of the modulating signal (f_m) is chosen as the fundamental frequency. The intersection points of the triangular carrier signals and the modulating signal determine the switching instants $\alpha_1 < \alpha_2 < \alpha_3 < \ldots < \alpha_k$ (Fig. 1b), where k is a positive integer. Figure 3 shows the SPWM waveforms used for the chain link STATCOM with 3-links. The upper carrier signals switch the GTO-diode pairs S_1/D_1 and S_2/D_2 to contribute $+V_{dc}$ to the output voltage. The lower carrier signals switch the GTO-diode pairs S_3/D_3 and S_4/D_4 to contribute $-V_{dc}$. When the carrier does not intersect the modulating signal, the link is in a non-contributing state. For the CLS, the amplitude modulation index, m_a is defined as the ratio of the peak value of the sinusoidal modulating signal, to the sum of the peak-to-peak values of all the upper (or lower) carriers:

$$m_a = \left(\hat{V}_{\text{mod}} \Big/ \sum_{1}^{N} \hat{V}_{tri} \right) \qquad (1)$$

For the proposed STATCOM with 3-links, the sum of the peak-to-peak values of all the three upper (or lower) carriers is arbitrarily chosen as 1 (Fig. 3a). The harmonic analysis of per phase modulated CLS output voltage (Fig. 1b for *N*-links & Fig. 3b for 3-links) is done by using the Double Fourier Series (DFS) technique [11]. For simplicity, the fundamental Fourier series component of the output voltage of the CLS having *N*-links per phase is approximated by:

$$v_o \approx V_{dc}\, N\, m_a \cos(\omega_o t) \qquad (2)$$

Where, the peak magnitude of the output voltage is $\hat{V}_o = \sqrt{2}\, V_o = N m_a V_{dc}$. Hence, for $N = 3$ and $m_a = 1.0$ (Fig. 3b) $v_o \approx 3V_{dc} \cos(\omega_o t)$ and $\hat{V}_o = 3V_{dc}$. However, instead of being a single term, the fundamental component, v_o is made up of an infinite number of terms [11].

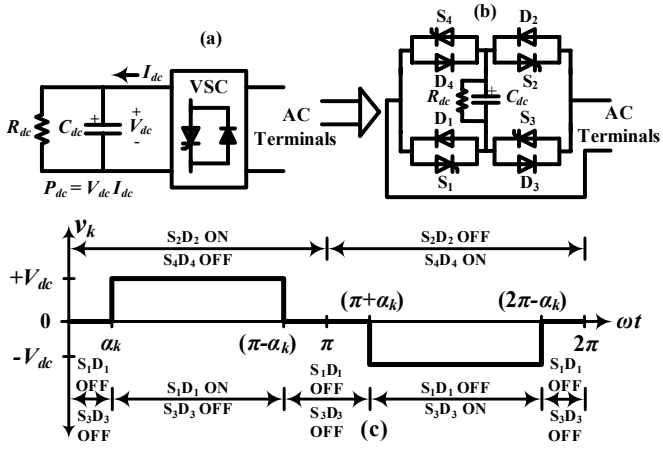

Fig. 2. (a) Block diagram (b) simplified circuit diagram and (c) 3-level output voltage (v_k) of a 1-ph VSC 'link'.

III. CLS POWER CIRCUIT, SYSTEM MODELING & CONTROL STRATEGIES

A 3-phase CLS having 3-links per phase is modeled in EMTP-RV to investigate its behavior under different power system operating conditions. The model of the CLS is comprised of three fundamental blocks: a switch, a VSC link and an SPWM circuit. Approximate mathematical models of the CLS system are also obtained in this section.

A. Power circuit of the CLS system

For the proposed CLS model validation, a 3-phase radial

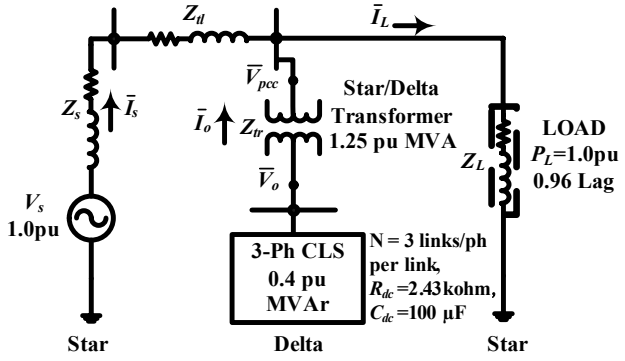

Fig. 4. Single line diagram of the CLS system.

transmission test system is considered (Fig. 4). The measurements are referred to a per unit system with a base rating of 10 MVA and a primary/secondary voltage rating of 400/15.1 kV. The sending end of the transmission line is connected to a 3-phase star-connected supply, represented by a Thevenin equivalent voltage source (v_s) of magnitude 1.0 pu behind the source impedance (Z_s)=(0.0005+j0.05) pu. The supply system is assumed to keep v_s constant under all loading conditions. A 3-phase star-connected transmission line is represented by an equivalent transmission line impedance (Z_{tl})=(0.001+j0.1) pu in series with the power supply. A 3-phase star connected R-L load of rated active power (P_L)=1.0 pu at 0.96 power factor lagging (i.e. rated load reactive power, Q_L≈0.3 pu) and having load impedance (Z_L)=(0.921+j0.124) pu, is connected at the receiving end of the transmission line. The proposed CLS is connected in 3-phase delta-connection at the PCC across the load via a 3-phase star-delta coupling transformer of MVA rating 1.25 pu and leakage impedance (Z_{tr})=(0.0005+j0.05) pu. The coupling transformer reduces the transmission system high voltage to a level suitable for the design rating of the CLS, which in turn depends on the individual switch rating. In Fig. 4, $\bar{V}_o$ represents the voltage vector of the fundamental Fourier series component of the CLS output voltage (v_o). The terms $\bar{V}_s$ & $\bar{V}_{pcc}$ are the vectors of the Thevenin equivalent source voltage (v_s) and voltage at the PCC (v_{pcc}), respectively, whereas $\bar{I}_o$ & $\bar{I}_L$ are the STATCOM output and load current vectors (i_o & i_L), respectively.

The EMTP-RV models of a GTO-diode switch 'SW' and VSC link are shown in Figs. 5a and 5b [9]. The SPWM circuit modeled in EMTP-RV is for a 3-phase CLS having 3-links per phase. However, this principle can be extended for a CLS having any number of links per phase. The main blocks of the EMTP-RV model of the SPWM circuit are the triangular carrier generator (TCG) per VSC link (Fig. 5c) and comparator per switch (Fig. 5d). For the proposed CLS, the EMTP-RV model of the SPWM circuit is comprised of three TCGs and eight comparators per phase.

B. System modeling

Figure 6a represents the Thevenin equivalent circuit of the CLS system (Fig. 4). For an ideal 3-phase power supply, the instantaneous phase voltages at the PCC & CLS output terminals and the instantaneous CLS output phase currents are:

$$\begin{bmatrix} v_{pcc\_a} \\ v_{pcc\_b} \\ v_{pcc\_c} \end{bmatrix} = \sqrt{2}V_{pcc} \begin{bmatrix} \cos(\omega_o t + \theta) \\ \cos(\omega_o t + \theta - 2\pi/3) \\ \cos(\omega_o t + \theta + 2\pi/3) \end{bmatrix} \quad (3)$$

$$\begin{bmatrix} v_{o\_a} \\ v_{o\_b} \\ v_{o\_c} \end{bmatrix} = \sqrt{2}V_{o} \begin{bmatrix} \cos(\omega_o t + \theta - \delta) \\ \cos(\omega_o t + \theta - \delta - 2\pi/3) \\ \cos(\omega_o t + \theta - \delta + 2\pi/3) \end{bmatrix} \quad (4)$$

$$\begin{bmatrix} i_{o\_a} \\ i_{o\_b} \\ i_{o\_c} \end{bmatrix} = \sqrt{2}I_{o} \begin{bmatrix} \cos(\omega_o t + \theta + \varphi) \\ \cos(\omega_o t + \theta + \varphi - 2\pi/3) \\ \cos(\omega_o t + \theta + \varphi + 2\pi/3) \end{bmatrix} \quad (5)$$

Where, ω_o is the system (or fundamental) frequency. The complex voltage and current vectors can be expressed in the stationary ($\alpha\beta$-axis) and synchronously rotating reference frame (dq-axis) as per [12]:

$$\bar{V}_{pcc} = \sqrt{2}\, V_{pcc}\, e^{j\theta} = (v_{pcc\_d} + j v_{pcc\_q})\, e^{j\theta} \quad (6)$$

$$\bar{V}_o = \sqrt{2}\, V_o\, e^{j(\theta-\delta)} = (\sqrt{2}V_o\cos\delta - j\sqrt{2}V_o\sin\delta)e^{j\theta} = (v_{o\_d} + jv_{o\_q})\, e^{j\theta} \quad (7)$$

$$\bar{I}_o = \sqrt{2}\, I_o\, e^{j(\theta+\varphi)} = (\sqrt{2}I_o\cos\varphi + j\sqrt{2}I_o\sin\varphi)\, e^{j\theta} = (i_{o\_d} + ji_{o\_q})\, e^{j\theta} \quad (8)$$

Note that the positive/negative signs of the angle show that the vectors are leading/lagging the reference axis respectively. The space vector diagram for voltages and current is shown in Fig. 6b, where $\alpha\beta$-axis represent synchronous rotating reference frame. The d-axis is assigned to coincide with the space vector $\bar{V}_{pcc}$. When i_{o_q} is negative, the CLS supplies capacitive reactive power to the line and for positive i_{o_q}, it absorbs inductive reactive power. By writing the KVL

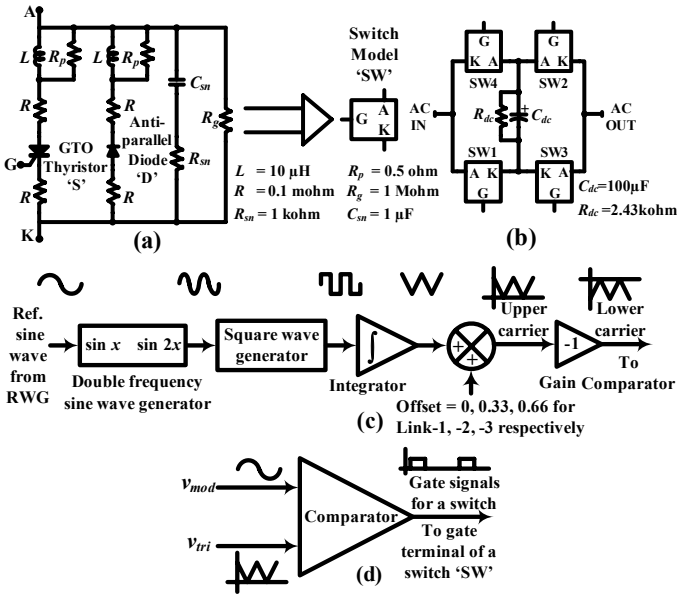

Fig.-5. Models in EMTP-RV (a) GTO-diode switch, 'SW' (b) VSC link (c) SPWM TCG per link and (d) SPWM comparator.

equation of the power system (Fig. 6a) in stationary reference frame ($\alpha\beta$-axis):

$$L\frac{d\bar{I}_o}{dt} + R\bar{I}_o = \bar{V}_o - \bar{V}_{pcc} \tag{9}$$

From (6), (7) and (8), the complex vectors can be transformed from $\alpha\beta$-axis to dq-axis by multiplying them with a unit space vector, $e^{-j\theta}$ and substituting (2) into (9). Rearranging the voltage equations for real part in the d-axis and for imaginary part in the q-axis:

$$\frac{di_{o\_d}}{dt} = -\frac{R}{L}i_{o\_d} + \omega_o i_{o\_q} + \frac{N m_a}{L}V_{dc}\cos\delta - \frac{1}{L}v_{pcc\_d} \tag{10}$$

$$\frac{di_{o\_q}}{dt} = -\omega_o i_{o\_d} - \frac{R}{L}i_{o\_q} - \frac{N m_a}{L}V_{dc}\sin\delta - \frac{1}{L}v_{pcc\_q} \tag{11}$$

The active power flows into the CLS can be described as:

$P_{DC} = P_{AC}$, where, $P_{DC} = 3NP_{dc}$ (12)

$$3NV_{dc}I_{dc} = \begin{bmatrix} v_{o\_a} \\ v_{o\_b} \\ v_{o\_c} \end{bmatrix}\begin{bmatrix} i_{o\_a} & i_{o\_b} & i_{o\_c} \end{bmatrix} = \frac{3}{2}(v_{o\_d}i_{o\_d} + v_{o\_q}i_{o\_q}) \tag{13}$$

Where, the dc current is the sum of the capacitor current and resistor current (Fig. 2a), i.e.

$$I_{dc} = C_{dc}\frac{dV_{dc}}{dt} + \frac{V_{dc}}{R_{dc}} \tag{14}$$

Substituting (14), $v_{o\_d} = N m_a V_{dc}\cos\delta$ and $v_{o\_q} = -N m_a V_{dc}\sin\delta$ into (13) and rearranging:

$$\frac{dV_{dc}}{dt} = \frac{m_a}{2C_{dc}}i_{o\_d}\cos\delta - \frac{m_a}{2C_{dc}}i_{o\_q}\sin\delta - \frac{V_{dc}}{C_{dc}R_{dc}} \tag{15}$$

By combining (10), (11) and (15) the CLS state equation can be formed as:

$$\frac{d}{dt}\begin{bmatrix} i_{o\_d} \\ i_{o\_q} \\ V_{dc} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & \omega_o & \frac{N m_a}{L}\cos\delta \\ -\omega_o & -\frac{R}{L} & -\frac{N m_a}{L}\sin\delta \\ \frac{m_a}{2C_{dc}}\cos\delta & -\frac{m_a}{2C_{dc}}\sin\delta & -\frac{1}{C_{dc}R_{dc}} \end{bmatrix}\begin{bmatrix} i_{o\_d} \\ i_{o\_q} \\ V_{dc} \end{bmatrix} + \begin{bmatrix} -\frac{1}{L} & 0 \\ 0 & -\frac{1}{L} \\ 0 & 0 \end{bmatrix}\begin{bmatrix} v_{pcc\_d} \\ v_{pcc\_q} \end{bmatrix} \tag{16}$$

From the above analysis, it is noted that either adjusting m_a or the phase angle δ of the CLS output voltage vector, the CLS output voltage could be controlled. For the proposed CLS, m_a is kept constant and only δ is regarded as a control input [12]. Consequently (16) becomes nonlinear. However, for small perturbations around the steady-state equilibrium point δ_o, the linear set of equations can be obtained. The linearization process yields the following perturbation equations:

$$\frac{d}{dt}\begin{bmatrix} \Delta i_{o\_d} \\ \Delta i_{o\_q} \\ \Delta V_{dc} \end{bmatrix} = [\mathbf{A}_\Delta]\begin{bmatrix} \Delta i_{o\_d} \\ \Delta i_{o\_q} \\ \Delta V_{dc} \end{bmatrix} + [\mathbf{B}_\Delta]\begin{bmatrix} \Delta v_{pcc\_d} \\ \Delta v_{pcc\_q} \\ \Delta\delta \end{bmatrix} \tag{17}$$

Where,

$$[\mathbf{A}_\Delta] = \begin{bmatrix} -\frac{R}{L} & \omega_o & \frac{N m_a}{L}\cos\delta_o \\ -\omega_o & -\frac{R}{L} & -\frac{N m_a}{L}\sin\delta_o \\ \frac{m_a}{2C_{dc}}\cos\delta_o & -\frac{m_a}{2C_{dc}}\sin\delta_o & -\frac{1}{C_{dc}R_{dc}} \end{bmatrix}$$

$$[\mathbf{B}_\Delta] = \begin{bmatrix} -\frac{1}{L} & 0 & -\frac{N m_a}{L}V_{dco}\sin\delta_o \\ 0 & -\frac{1}{L} & -\frac{N m_a}{L}V_{dco}\cos\delta_o \\ 0 & 0 & -\frac{m_a}{2C_{dc}}(i_{o\_do}\sin\delta_o + i_{o\_qo}\cos\delta_o) \end{bmatrix}$$

The STATCOM steady state model can be obtained from the dynamic model by setting all the derivative terms equal to zero. After transformation from *abc* to *dq* reference frame, the voltages and the currents become dc quantities. Therefore, substituting $v_{pcc\_d} = |v_{pcc}| = \sqrt{2}V_{pcc}$, $v_{pcc\_q} = 0$, $i_{o\_d} = I_{o\_d}$, and $i_{o\_q} = I_{o\_q}$, the STATCOM steady state model becomes:

$$\begin{bmatrix} -R & X & N m_a\cos\delta_o \\ -X & -R & -N m_a\sin\delta_o \\ m_a\cos\delta_o & -m_a\sin\delta_o & -\frac{2}{R_{dc}} \end{bmatrix}\begin{bmatrix} I_{o\_d} \\ I_{o\_q} \\ V_{dc} \end{bmatrix} = \begin{bmatrix} |v_{pcc}| \\ 0 \\ 0 \end{bmatrix} \tag{18}$$

Where, $X = \omega_o L$. By solving (18) for I_{o_d}, I_{o_q} and V_{dc}, the solutions are:

$$I_{o\_d} = \frac{2R - N m_a{}^2 R_{dc}\sin^2\delta_o}{N m_a{}^2 R R_{dc} - 2R^2 - 2X^2}|v_{pcc}| \tag{19}$$

$$I_{o\_q} = -\frac{(2X + N m_a{}^2 R_{dc}\sin\delta_o\cos\delta_o)}{N m_a{}^2 R R_{dc} - 2R^2 - 2X^2}|v_{pcc}| \tag{20}$$

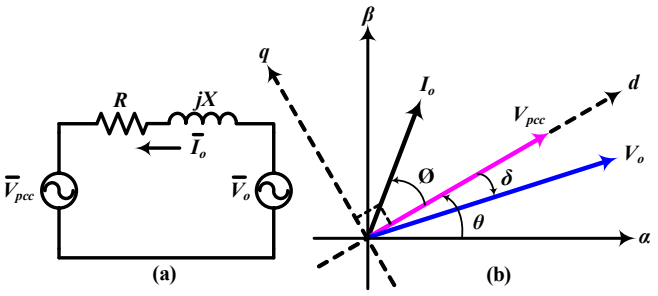

Fig. 6. (a) Thevenin equivalent circuit of CLS system, and (b) its space vector diagrams.

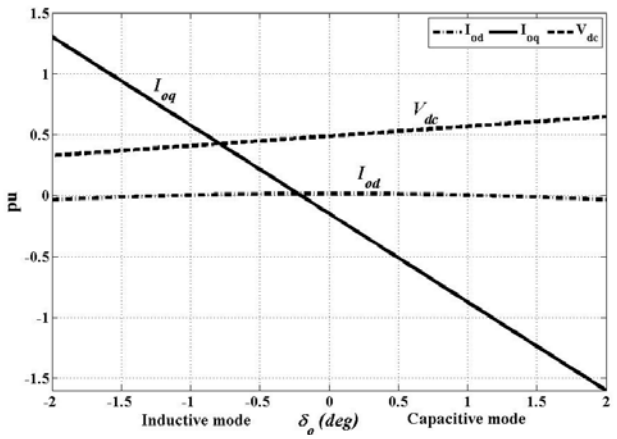

Fig. 7. Steady-state variation of I_{o_d}, I_{o_q} and V_{dc} against δ_o

$$V_{dc} = \frac{m_a R_{dc}(R\cos\delta_o + X\sin\delta_o)}{N m_a^2 R R_{dc} - 2R^2 - 2X^2} |v_{pcc}| \qquad (21)$$

From (19), (20) and (21), it is apparent that I_{o_d}, I_{o_q} and V_{dc} in steady state, do not depend on the size of the capacitor. The CLS system (Fig. 4), has Thevenin equivalent R=1.39 ohm and X=13.05 ohm (Fig. 6a). For the given system, the steady state variations of the operating points I_{o_d}, I_{o_q} and V_{dc} against δ_o are plotted in Fig. 7 with m_a=1.0. At steady state, the reactive current I_{o_q} varies almost linearly with respect to δ_o, and the range of δ_o for 1.0 pu swing in I_{o_q} is very small. For the delayed (or positive) value of δ_o, the CLS supplies (i.e. capacitive mode) the reactive power to the line, hence I_{o_q} is negative and for the advanced (or negative) value of δ_o, the CLS absorbs (i.e. inductive mode) VARs from the line, hence I_{o_q} is positive. The capacitor voltage, V_{dc} also increases almost linearly with δ_o from advanced to delayed δ_o. The active current, I_{o_q} is small and varies only a little with δ_o because it is required only to compensate the CLS losses and to maintain V_{dc} constant at the desired level.

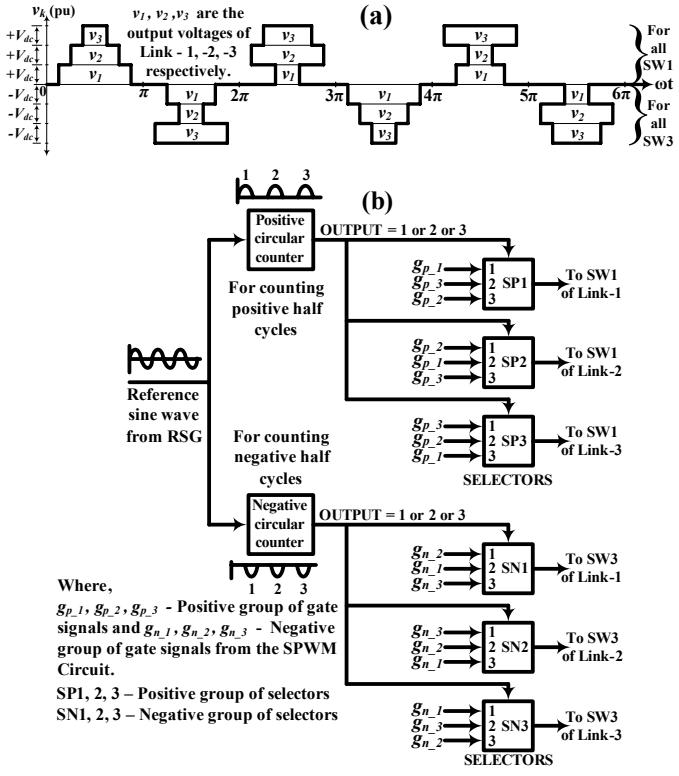

Fig. 8. (a) RGSP and (b) RGSP control logic scheme in EMTP-RV.

C. Control strategies

As shown in Figs. 1b & 3b, in a CLS, each link is assigned to contribute a 3-level ac voltage of different pulse widths to synthesize the multilevel CLS output voltage waveform. Consequently, each link faces unequal stresses and results in unbalanced dc voltages among the link dc capacitors. The unbalanced dc capacitor voltages cause more harmonics in the output voltage waveform and reduce the fundamental component. In order to overcome the above problem, the switching patterns are rotated among the links per phase, in every half cycle of the fundamental frequency [13]. This novel technique is called the rotated gate signal pattern (RGSP). By using RGSP, each switch is turned ON/OFF equally, which causes equal charging and discharging of all dc capacitors and consequently equal stress distribution among the links. However, by using RGSP, the link output voltages (v_k) have different pulse widths in every half cycle (Fig. 8a), the CLS output voltage still remains as shown in Fig. 3b. Figure 8b shows the EMTP-RV model of the control logic scheme used to obtain the RGSP for the CLS having 3-links per phase. Figures 9a & 9b show the simulated results of the instantaneous dc voltages and Figs. 9c & 9d show the dc capacitor voltage magnitudes of all three links per phase without RGSP (Figs. 1b & 3b) and with RGSP (Fig. 8a) respectively. The simulated results confirm that, in the CLS, with the use of RGSP, balanced dc voltages are obtained. As a disadvantage, the RGSP scheme introduces a low frequency ripple of the frequency approximately equal to $2f_s/N$ (here as N = 3 links per phase, the ripple is of 40 Hz frequency) super imposed on the second order (120 Hz) ripple. However the low frequency ripple can be minimized or eliminated by increasing number of links per phase in the CLS. In practical

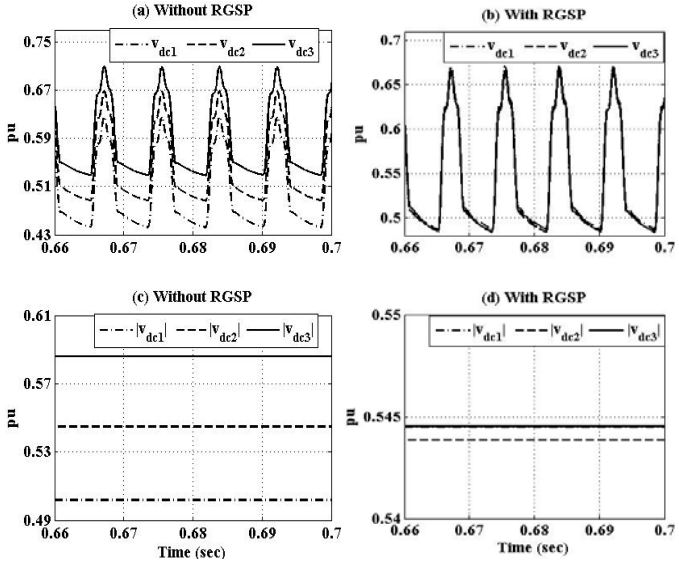

Fig. 9. Instantaneous dc voltages (a) without RGSP and (b) with RGSP and dc voltage magnitudes (c) without RGSP and (d) with RGSP.

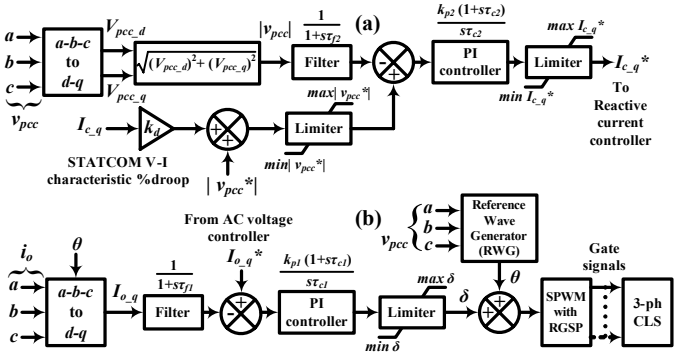

Fig. 10. (a) AC voltage, and (b) reactive current controllers.

scheme, a CLS having 12 to 14 links per phase is used [7, 8], which considerably reduces the low frequency ripple and the harmonics from the CLS output voltage.

From the preliminary evaluation of the 1-phase, 3-link CLS [9] and (17), it is clear that the control input $\Delta\delta$ influences the system states. Therefore, from (17), by neglecting the second-order terms and assuming that the equilibrium point is at $\delta_o \approx 0$, the corresponding approximate first-order transfer function relating Δi_{o_q} & $\Delta\delta$, is obtained as:

$$\frac{\Delta I_{o\_q}(s)}{\Delta \delta(s)} = -\frac{N m_a V_{dco}}{L(s+\frac{R}{L})} \qquad (22)$$

The control objective is to stabilize the voltage at the PCC by regulating the flow of i_{o_q}. The relationship between Δv_{pcc_d} & Δi_{o_q} is obtained by applying KVL in Fig. 6a, and neglecting the losses, as $R << X (= \omega_o L)$:

$$\frac{\Delta V_{pcc\_d}(s)}{\Delta I_{o\_q}(s)} = X \qquad (23)$$

Where, $\Delta V_{pcc\_d} = \Delta|v_{pcc}|$. Based on (22) and (23), two cascaded (reactive current or inner & ac voltage or outer) control-loops are developed by using PI controllers from the feedback of the transmission system voltage (v_{pcc}) and the CLS output reactive current (i_{o_q}) (Fig. 10). The block diagrams of both the control-loops are shown in Fig. 11. To simplify the controller design, it is assumed that the two control-loops are relatively independent of each other. The measurement system calculates the magnitudes of v_{pcc} and i_{o_q} in a synchronously rotating reference frame (dq-axis). The reference wave

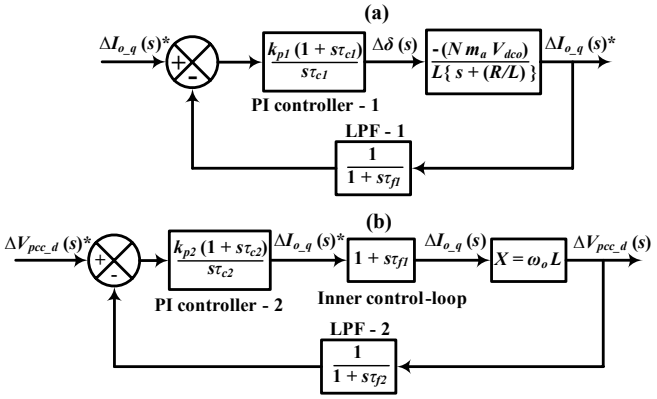

Fig. 11. Block diagrams of (a) inner (reactive current), and (b) outer (ac voltage) control-loops.

generator (RWG) calculates the angular position of the vector (θ). Two first-order low-pass filters (LPF) with the delays $1/(1+s\tau_{f2})$ & $1/(1+s\tau_{f1})$, are used in the feedback path of $|v_{pcc}|$ & I_{o_q}, respectively. The magnitude of the reference voltage at the PCC ($|v_{pcc}^*|$) is compared with the actual value ($|v_{pcc}|$) in the outer control-loop and the reference quadrature current magnitude ($I_{o\_q}^*$) is obtained by error amplification using PI controller-1. This reference current magnitude is then compared with the actual current magnitude (I_{o_q}) in the inner control-loop and by error amplification using PI controller-2, the phase angle, δ is obtained. The angle δ is added to the angular reference position (θ) to generate the switching signals using SPWM. Due to the change in δ, V_{dc} and hence v_o changes to regulate the flow of i_{o_q} which consequently stabilizes v_{pcc}. Limiters are used in the control circuit to prevent overshoot and saturation of the controllers. A droop (k_d) of about 1-3% in the V-I characteristic of the CLS is introduced for the fast dynamic response.

IV. Simulation Results

The CLS system and the controllers explained above are simulated with EMTP-RV using a 10μs time-step and the performance results are presented next.

A. Steady-state performance

Figure 12 shows the steady-state waveforms of (a) the phase voltage at the PCC (v_{pcc_ab}), (b) the CLS output phase voltage (v_{o_ab}) (c) the CLS output phase current (i_{o_ab}) (d) the CLS output line current (i_{o_a}) and (e) dc voltages of the three CLS links (v_{dc1_ab}, v_{dc2_ab}, v_{dc3_ab}) per phase. In steady-state, the CLS maintains $|v_{pcc}|$ at 1.0 pu by supplying a rated reactive power (or line current) of 0.4 pu to the power system to compensate the voltage drop due to transmission line impedance (Z_{tl}). The voltage waveforms, v_{pcc_ab} & v_{o_ab} are almost sinusoidal in nature (Figs. 12a & 12b respectively) and contain negligible amount of odd-order harmonics (Figs. 13a & 13b respectively). Note that, the triplen harmonics are absent in both the voltages due to the delta-connection of the CLS. The CLS output phase and line current waveforms (i_{o_ab} & i_{o_a}) are

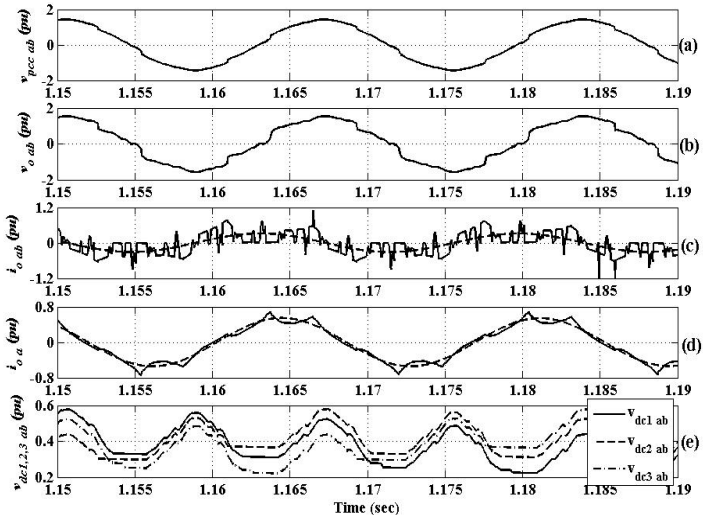

Fig. 12. Steady-state waveforms.

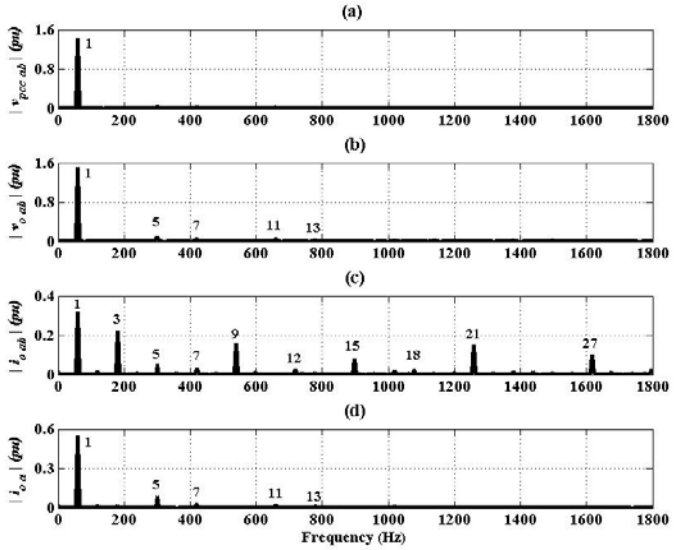

Fig. 13. Harmonic spectrums.

symmetrical and follow the fundamental sinusoidal pattern (Figs. 12c & 12d respectively). The phase current (i_{o_ab}) leads v_{pcc_ab} & v_{o_ab} by approximately 90° and has a peak magnitude of approximately 0.33 pu (i.e. 0.23 pu rms) to stabilize $|v_{pcc}|$ at 1.0 pu. The harmonic spectrum of i_{o_ab} shows dominant triplen harmonics (Fig. 13c) whereas the same are absent in the line current (i_{o_a}) (Fig. 13d) due to the delta-connection of the CLS. Moreover, the line current is almost sinusoidal in nature and contains only a low magnitude of odd-order (except the triplen) harmonics. It is important to note here that the simulation results presented in this paper are without harmonic filters for the CLS system having only 3-links per phase. Therefore, by increasing number of series connected links per phase in the CLS, the harmonics can be further reduced and the use of harmonic filters can be avoided. This can be seen as an overall reduction in the cost of the CLS system. The capacitor used for the voltage support on the dc side of each link has a finite value. Moreover, each link functions as a 1-phase full bridge VSC; therefore, the dc voltage contains ripple at a frequency of 120 Hz (Fig. 12e). The dc voltage ripple depends on, the CLS VAR output, the number of links used per phase and the load. Figure 12e shows considerable amount of dc voltage ripple because CLS is supplying the rated VAR output. Furthermore, as explained, due to the employment of the RGSP, each v_{dc} also contains a low frequency (~40 Hz) ripple superimposed on the second order (120 Hz) ripple. The low frequency ripple of v_{dc} and hence the harmonic content of the CLS output voltage and current can be minimized by increasing number of links per phase in the CLS.

B. Transient-state performance

The CLS is designed to compensate up to 0.4 pu of the transmission line reactive power at the PCC, in the capacitive mode. The systematic calculation of the gains of the PI controllers is out of the scope of this paper. Consequently, the PI controller gains are obtained by trial-and-error as: k_{p1}=0.078, k_{i1}=4.85, k_{p2}=14.6 k_{p1}=415. To investigate the dynamic performance of the CLS system with the controllers (Figs. 4 & 10), the simulation tests are carried out as follows:

1) Step change in voltage reference

In the simulated responses of the step change in the voltage reference ($|v_{pcc}^*|$) (Fig. 14), the R-L load at the receiving end is kept constant with P_L=1.0 pu & Q_L≈0.3 pu. Before the disturbance, the CLS controls $|v_{pcc}|$ at 1.0 pu by supplying the rated VAR (Q_o) of approximately 0.4 pu. The disturbance is introduced at time, t=1.2s by applying a step change in $|v_{pcc}^*|$ of the controller from 1.0 to 0.975 pu. The dynamic response is stable and $|v_{pcc}|$ steps down from 1.0 to 0.975 pu with an approximate over shoot of 5% and a settling time of about five cycles (Fig. 14a). In order to reduce $|v_{pcc}|$ from 1.0 to 0.975 pu, as a response to the step change in $|v_{pcc}^*|$, the CLS reactive output phase current (i_{o_q}) (Fig. 14b) the reactive power output (Q_o) (Fig. 14e) and hence the phase angle (δ) (Fig. 14c) decrease. Consequently, the dc voltages of the link dc capacitors of the CLS also decrease (Fig. 14d).

2) Step change in the load

The simulated responses of the step change in the load are

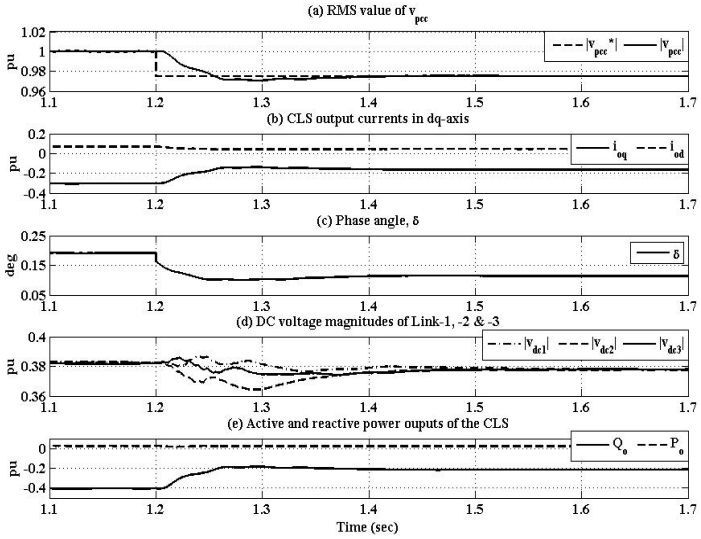

Fig. 14. Response of step change in voltage reference.

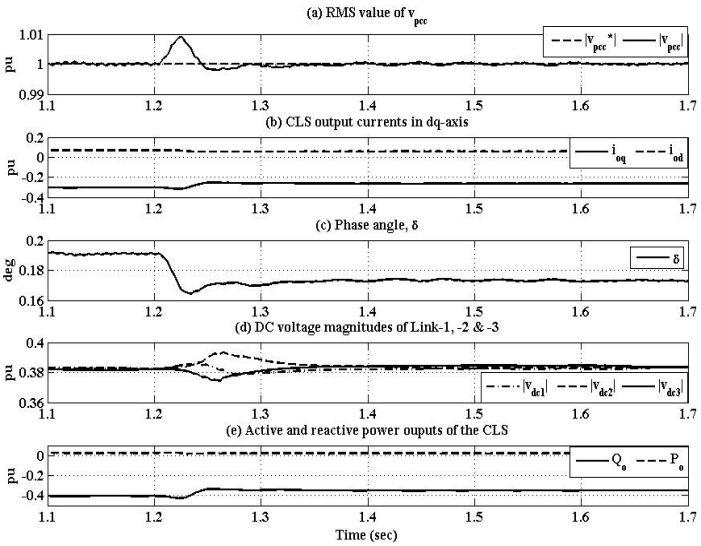

Fig. 15. Response of step change in load.

shown in Fig. 15. In this test, the voltage reference ($|v_{pcc}^*|$) is kept constant at 1.0 pu. Before the disturbance, the R-L load at the receiving end is having P_L=1.0 pu & Q_L≈0.3 pu and the CLS controls $|v_{pcc}|$ at 1.0 pu by supplying the rated VAR (Q_o) of approximately 0.4 pu. The disturbance is introduced at time, t=1.2s by applying a -10% step change in the load (i.e. P_L & Q_L changes to 0.9 pu & 0.27 pu respectively). The above step change causes only a short transient that is dampened quickly in about five cycles and the dynamic response is stable. Therefore, in steady-state $|v_{pcc}|$ stays at 1.0 pu (Fig. 15a). As a response to the above step change, i_{o_q} (Fig. 15b), Q_o (Fig. 15e) and hence δ (Fig. 15c) decrease in order to maintain $|v_{pcc}|$ at 1.0 pu. Consequently, the dc voltages of the link dc capacitors of the CLS also decrease (Fig. 15d). Due to the employment of the RGSP in the CLS, the dc voltages after each disturbance are balanced (Figs. 14d & 15d).

V. Conclusions

A 3-phase CLS having 3-links per phase is presented in this paper. The SPWM technique to drive the switches of the CLS is used such that each switch turns ON/OFF once per cycle of the fundamental frequency to reduce the converter losses by producing a 3-level output voltage waveform per link and to synthesize a multi-level CLS output voltage. Approximate mathematical models of the CLS system are developed using *dq*-transformations. These models are used to design the control strategy whereby the phase angle of the modulating signal is controlled to control the CLS output voltage and hence the voltage at the PCC.

A novel technique called as the RGSP is used to balance the link dc capacitor voltages, where the gating patterns are rotated among the links per phase, in every half cycle of the fundamental frequency. Unfortunately, as a disadvantage, this technique introduces a low frequency ripple in the dc voltages. However this ripple can be minimized or eliminated by increasing number of links per phase.

The performance investigation of the CLS system is done with EMTP-RV in steady- and transient-state conditions. The steady-state analysis shows that by a small variation of the phase angle, a large reactive power (or current) flow can be controlled in the CLS. The steady-state results show that the CLS can produce a good quality output voltage waveform by using a 3-phase delta-connection of the CLS (to eliminate some harmonics from the output line current) and by increasing the number of links per phase. Moreover, the transient tests show a good dynamic performance of the CLS for the voltage regulation. The system voltage recovers within five cycles after a step change in the voltage reference or the load due to the voltage support provided by the CLS system.

VI. Acknowledgment

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