Limitation of Line Fault Currents with the UPFC

L. C. Zanetta Jr., M. Pereira

Abstract - This paper analyses the instantaneous characteristic of series connected VSI-based compensators in fault currents limitations of compensated lines. The magnitude of the series voltage plays a very important role, and the possible use of values higher than those of steady state operation, during short periods, can reduce the undesirable effects of short-circuit currents. The effectiveness of the UPFC was investigated by exploring the series voltage behavior in three and single-phase faults.

Keywords - FACTS, short-circuit, UPFC.

I. Introduction

The FACTS (Flexible AC Transmission Systems) equipment, with series connected VSI based devices, like SSSC (Static Synchronous Series Compensator) and the UPFC (Unified Power Flow Controller), with nearly instantaneous responses, are intended to control the power flow on transmission lines.

Typically, these devices are mainly used for power flow control [1], [2], [3], [4], [5], [8] with an additional task of the shunt VSI being the line voltage support.

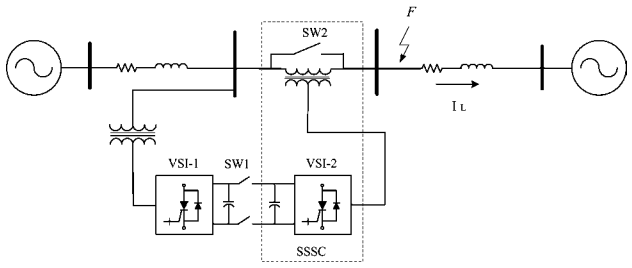

Fig. 1 Series-connected VSI

The connection of the shunt and series converters, VSI-1 and VSI-2, respectively, through the common capacitor, defines the joint operation of the SSSC and the STATCOM, to complete the UPFC arrangement.

Both the SSSC and the UPFC inject a nearly sinusoidal voltage in series with the line. The voltage developed by the UPFC can rotate along 360 degrees relative to the line current.

Power systems with meshed networks have complex power flow problems and the UPFC application is expected to help in power control.

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On the other hand, short-circuit current levels increase with the addition of new lines, generators and transformers. This may surpass the short circuit current ratings of equipment, like for example circuit breakers, a frequent problem in power systems.

The fault current limitation offered by modern controllers, characterized by their fast responses, may become an important assistance in the task to diminish such large currents. Since the fault clearing time is not instantaneous, depending on the operating time imposed by protection and breaker operation delays, adequate control actions can be performed by this equipment.

Although significant flexible features may be introduced in power control by those new devices, they still can be very expensive, and additional benefits like protection improvement should be investigated in order to verify the possibility of their application in the development of more secure and reliable networks.

The knowledge of the system response during fault periods due to the presence of new devices for current limitation is an important subject to be investigated aiming to analyze the viability of such new technology. In order to achieve that objective careful investigations should be performed, identifying system requirements and possible problems due to new applications in the system.

The fault limitation approach presented here explores this new technology and additional functionality offered by the series-connected VSI-based FACTS converters.

II. Fault Current Limitation

The fault current limitation based on impedance control is a quite known subject, as described in the literature. Three-phase faults can be controlled with limiting reactors and phase-to-ground faults need zero sequence impedance management, sometimes with the use of grounding devices. However, little information exists on short-circuit limitation with series voltage injection, in view of their recent introduction on networks.

Since the series voltages are introduced through series coupling transformers, their respective leakage reactances contribute for fault current limitation, and this aspect must be considered in the analysis.

The most important factor that we are analyzing is the possibility of series voltage insertion in an almost instantaneous way, which can also be understood as an emulated reactance or capacitance inserted into the line.

If a capacitive mode of compensation is in operation with voltage leading current, line fault current would be increased,

but if an inductive mode is introduced, with voltage lagging current, the stress of the fault could be substantially limited.

The UPFC fault limitation capability was investigated in [7], [8], [9] and [10], where it was showed that this device could be effective for that purpose.

A concern related to power electronics regards possible damages originated by high currents and their duration, a problem frequently handled with equipment by-pass. The importance of extensive studies of short-circuit currents and withstanding capability of semiconductors is recognized where power electronics is present. On the other hand, the fast control action of series voltages could be significant in the current limitation and so the present analysis is focused in this aspect.

A number of configurations could be envisaged, but we will take into consideration a quite common situation, where the UPFC is located in a substation, connected in series to a transmission line.

The main concept to be applied when inserting series voltages, as we are not modifying the network impedances, is to reduce as much as possible the voltage at the fault point, for three-phase and phase-to-ground faults, which is in fact in agreement with the Thevenin pre-fault voltage concept. As it is expected for short-circuit analysis, in the following only the inductive effect of the non-affected phases, will be considered.

In the very simple configuration of Fig. 2, let's suppose the short circuit occurring at the point F, the connection point of the UPFC to the line. The UPFC action is effective only for the system contribution, at left of the fault, injecting positive sequence voltages in opposition to the left equivalent source, having no effect in the line contribution. In fact, this could be a critical case, since as the fault moves along the line the system contribution reduces as the impedance increases.

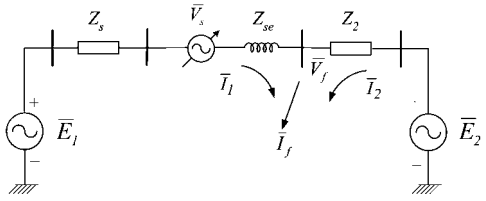

Fig. 2 Series VSI converter application

So, let's consider the fault point in Fig. 2 at bus *F* and the impedance Z_{se} of the series transformer added to the equivalent system impedance Z_s, forming the left side equivalent Z_1. The right side equivalent Z_2 refers to the line where the UPFC is connected in series with the other part of the system.

$$Z_1 = Z_s + Z_{se}$$

The voltage at point *F* due to E_1, E_2, without the presence of V_s, is called V_{uf} (uncompensated fault voltage). The series voltage contribution can be calculated applying the superposition theorem with the following network:

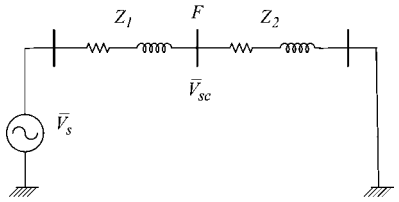

Fig. 3 Series voltage contribution to the fault current.

Calling M the three phase voltage divider matrix:

$$[M] = [Z_2][Z_1 + Z_2]^{-1} \quad (1)$$

The series compensating voltage contribution at the fault point *F* is called V_{sc} and can be obtained by:

$$[V_{sc}] = [M][V_s] \quad (2)$$

And finally, the compensated fault voltage (V_f) being

$$[V_f] = [V_{uf}] + [V_{sc}] \quad (3)$$

To minimize V_f, the compensation term V_{sc} has to be in opposition to V_{uf}, with the series voltage V_s being inserted at its maximum magnitude during the fault period.

Using equation (3) we can analyze the generic case of a three-phase fault.

For the case of a phase-to-ground fault, which is more likely to occur, other aspects such as the effect of the healthy phases should also be considered, which requires that a more careful analysis be performed, taking into account the contributions of positive, negative and zero sequence currents. This can be done with phase or sequence components. In fact, matrix *M* contains important information on the coupling of healthy phases to the faulted one, and so the better strategy of voltages to be developed by the VSI can be adopted. Considering transposed lines matrix *M* can be written as:

$$[M] = \begin{bmatrix} \alpha & \beta & \beta \\ \beta & \alpha & \beta \\ \beta & \beta & \alpha \end{bmatrix} \quad (4)$$

Factors α, β are dependent on the equivalent impedances Z_1 and Z_2 and on the zero and positive sequence values which define the coupling effect between phases. A more detailed analysis of these factors is still under way, but some previous results reveals that in some cases the effect of healthy phases should be considered through factor β.

Although the calculation of total fault current can be of interest [9], we will focus our analysis in the current contribution of one side of the system, taken here the contribution of Z_1 to the fault. For three-phase sort-circuit currents the voltage developed by the UPFC obviously must be in opposition to E_1.

In case of phase to ground fault, according to (3) and taking into account a three phase magnetic circuit, different strategies would be adopted for the voltage V_s. Our analysis will be restricted to verify the three phase application of positive or zero sequence voltages for conventional converters or just a single-phase voltage insertion with a special converter.

Complex cases, needing more sophisticated control actions are being left for future investigations.

The analysis can also be performed with symmetrical components, and to minimize the system fault contribution, which could basically affect the substation circuit breakers, the sequence diagrams are connected in series.

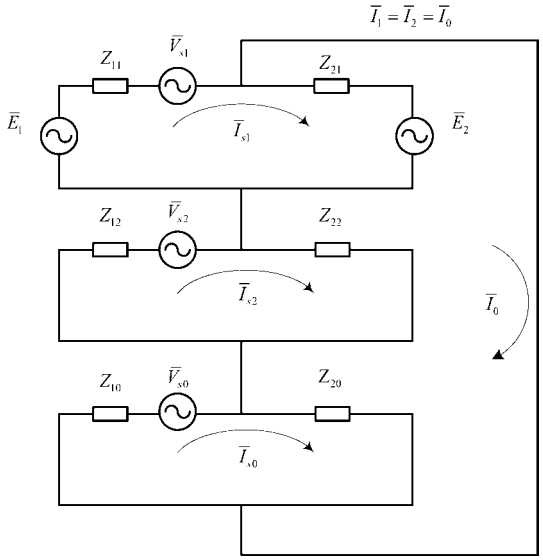

Fig.4 Equivalent sequence diagrams

where:

$\bar{I}_1, \bar{I}_2, \bar{I}_0$: symmetrical components of the fault current.

$\bar{I}_{s1}, \bar{I}_{s2}, \bar{I}_{s0}$: symmetrical components of system current contribution.

Calling:

$$[I] = \begin{bmatrix} \bar{I}_{s1} \\ \bar{I}_{s2} \\ \bar{I}_{s0} \\ \bar{I}_0 \end{bmatrix} \cdot [E] = \begin{bmatrix} \bar{E}_1 - \bar{E}_2 \\ 0 \\ 0 \\ \bar{E}_2 \end{bmatrix} [V_s] = \begin{bmatrix} \bar{V}_{s1} \\ \bar{V}_{s1} \\ \bar{V}_{s1} \\ 0 \end{bmatrix}$$

$\bar{V}_{s1}$, $\bar{V}_{s2}$, $\bar{V}_{s0}$: symmetrical components of the series voltage injected by the UPFC.

The loop equations for the diagram shown in Fig 4 can be written in its compact form:

$$[E] + [V_s] = [Z][I] \tag{5}$$

Calling

$$[Y]=[Z]^{-1}$$

We can write:

$$[I] = [Y][E] + [Y][V_s] \tag{6}$$

and:

$$[I] = [I_u] + [I_{sc}] \tag{7}$$

where:

$$[I_{sc}] = [Y][V_s] \tag{8}$$

$$[I_u] = [Y][E] \tag{9}$$

The term $[I_u]$ in (7) refers to the components of fault current contribution without series voltage and $[I_{sc}]$ is the series voltage contribution to the fault at point *F*. In order to minimize the system contribution to the total fault these currents must be in opposition.

Lets now obtain the left side contribution to the fault current in faulted phase *a*.

$$\bar{I}_{sa} = \bar{I}_{ua} + (\bar{I}_{s1} + \bar{I}_{s2} + \bar{I}_{s0}) \tag{10}$$

This current is obtained through the addition of the first three rows of (8), given:

$$\eta_j = \sum_{i=1}^{3} Y_{ij} \tag{11}$$

where η_j, $1 \le j \le 3$, corresponds to the sum of the first three elements of each column from *[Y]* .

The fault current at phase *a* can be rewritten:

$$\bar{I}_{sa} = \bar{I}_{ua} + \eta_1 \bar{V}_{s1} + \eta_2 \bar{V}_{s2} + \eta_0 \bar{V}_{s0}$$

The current $\bar{I}_{ua}$ may be obtained from any short circuit program. The best strategy for applying either the positive or zero sequence voltage, for each specific system, can be obtained from the analysis of η_j, even when inserting a one-phase voltage.

III. Simulation Results

This section presents the transient behavior of variables during short-circuits applied to the system depicted in Fig. 1. The simulation results were obtained in ATP program by the application of the series voltage compensation with sufficient time delay from the fault inception, only with the purpose to highlight their effect. The instant at which the series voltage is inserted, certainly should be as closest as possible following the fault occurrence, which would increase the effectiveness of the protection system to high currents, avoiding undesirable consequences or equipment damage. The current limitation in this case would also reduce the stress imposed on the semiconductor switches.

With adequate treatment of the fault current, optimal strategy and control action could be developed at the beginning of the fault, a subject not focused in this paper that should be taken into account in a future work. For unbalanced faults, the possibility to develop different voltages in all three phases would also be desirable.

The faults were simulated in the ATP program using a balanced system, in order to verify the possible ability of the UPFC and its internal variables in handling short-circuit currents.

The system used in the analysis presents the following parameters in pu:

System side:

$Z_{10} = .092\angle 77.5^{o}$; $Z_{11} = 0.13\angle 81.3^{o}$

Line side:

$Z_{20} = 0.16\angle 82.9^{o}$; $Z_{21} = 0.044\angle 63.4^{o}$

Originally the system shows symmetry in its positive sequence parameters, but the inclusion of the impedance of the series transformer on the system side unbalances the positive sequence.

The applied converter is a simple neutral-point clamped three-level VSI converter, and no special device was developed for the simulations. For phase-to-ground faults the negative and zero sequence components were incorporated in the model.

Shunt and series converters have a simple PI (Proportional-Integral) controllers and the PLL (Phase-Locked Loop) also has not any particular features. Its characteristics were adopted as being similar to the model given in [6]. The UPFC compensation characteristic simulated in the ATP program was used to control the currents from faults occurring in the compensated line, at the line terminal.

The following results are mostly related to the system left side contribution, with the measuring switch connected between the series coupling transformer and point *F*.

According to the previous analysis of section II, if we consider an operative condition prior to the fault of the system as depicted in Fig. 1 with E_1 with 0° and E_2 with –10°, the voltage at point *F* would have a phase of –5°, for a symmetrical system. During the fault period, the angle of the series voltage should be around 175° in order to reduce the total fault current. To minimize the left equivalent contribution, an angle of 180° in opposition to the 0° of the left equivalent voltage would be necessary, reducing the substation circuit breaker currents. In fact, these two values are quite similar and would not present significant differences in both cases. Those angular values correspond to a strong system with high short-circuit current values and the impact of correct angle application would be more significant in weak systems.

A. Three-Phase Faults

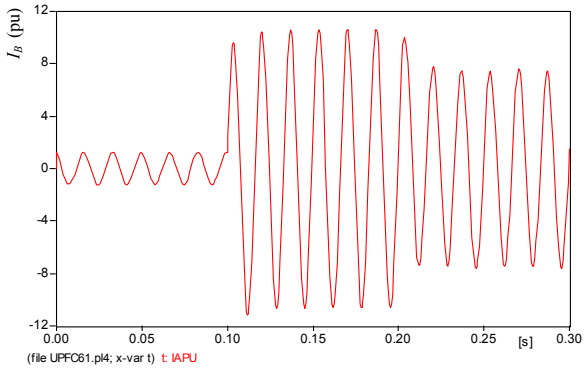

Fig. 5 Reduction of three-phase fault current contribution of system side with UPFC. Voltage transformer relation 1:1.

The UPFC response towards the three-phase short-circuit current is shown in Fig. 5, with a voltage transformer relation primary (converter) to secondary (line) of 1:1.

The three-phase fault currents shown in this figure were reduced from 10.7 pu to 7.4 pu, in approximately 30%. In fact those current values for three-phase faults were obtained with a slightly lower value of positive sequence impedance from system side, which does not change the overall analysis being performed.

This limitation has a strong dependence on the maximum series voltage developed by the converter and in the following cases the maximum value adopted was 0.3 pu.

Of course, higher values of series voltages would reduce even more the fault current, but with an impact on the equipment cost. The next case, presented in Fig. 6, explores the possibility of short-circuit current control increasing the voltage transformer relation in 1: 2 (primary to secondary).

This change can interfere in the leakage reactance reflected to the secondary, so the values were rearranged to yield the same fault current previously obtained.

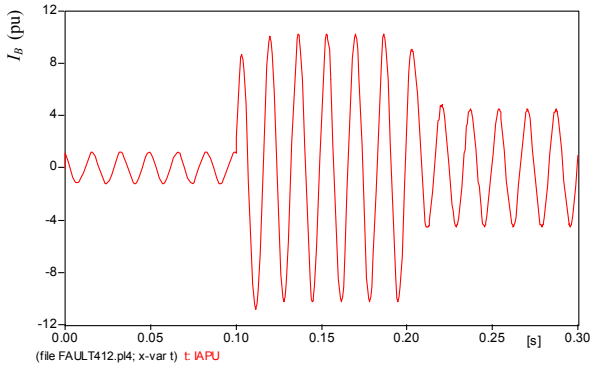

Fig. 6 Reduction of three-phase fault current contribution of system side with UPFC. Voltage transformer relation 1:2.

The three-phase fault currents were reduced from 10.7 pu to 4.8 pu, in approximately 55%. The results show that the transformer voltage relation would have a significant effect on the current limitation, amplifying the voltage developed by the converter. On the other hand the currents in the converter side would be higher causing a negative impact on static switches design.

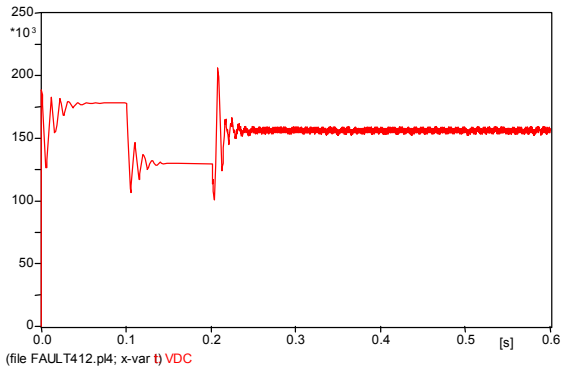

Fig. 7 Voltage at the coupling capacitor during the fault period.

Fig. 7 presents the voltage in the coupling capacitor, showing its variations during the fault and after the series voltage insertion. Although some variations can occur, a relatively stable behavior can be observed in this case.

Some cases presented a more oscillatory behavior, but adequate control actions can be implemented to overcome this problem, a point that shall be explored in future work

B. PHASE-TO-GROUND FAULT

The following results correspond to phase-to-ground faults applied in the AC system, taking into account its positive and zero sequence impedances.

Fig. 8 presents a zero sequence voltage insertion during the fault time period, with amplitude of 0.3 pu. The applied voltage was displaced 180 degrees from the system equivalent voltage, in order to be in opposition to that.

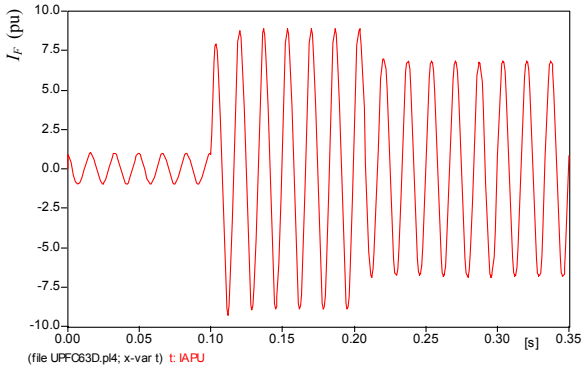

Fig. 8 Reduction of phase-to-ground fault current contribution of system side with UPFC. Zero sequence voltage application.

The fault current contribution from the system side is reduced from 9.0 pu to about 6.8 pu when the series voltage with zero sequence is applied. This case considered the voltage transformer relation of 1:1. For this specific system condition no significant difference was observed when positive sequence was applied.

Another point to be focused for unbalanced faults, like phase-to-ground faults, is the possibility of voltages insertion in selected phases, which would need a special arrangement for voltages developed by the converter. In this specific case of phase-to-ground fault the voltage insertion would be obviously in the faulted phase, resulting in $V_{s0} = V_{s1} = V_{s2}$. For this particular system condition the voltage insertion only on faulted phase *a* and the application of zero sequence series voltage led to very similar results for currents in the faulted phase and so the corresponding figure will not be presented. The reason for this behavior can be found on factors η_j, which are almost equal, although there were zero sequence differences in equivalents Z_1 and Z_2 from both sides.

$$\eta = \eta_1 \simeq \eta_2 \simeq \eta_0$$

$$I_{sa} = I_{sau} + \eta(V_{s1} + V_{s2} + V_{s0})$$

or:

$$I_{sa} = I_{sau} + \eta V_a$$

In fact, other system conditions should be investigated in order to check the significance of these factors for such analysis.

The effect of voltage insertion only on faulted phase *a* is presented in Fig. 9 for higher values of the series voltage, at 0.5pu, 0.7pu and 0.9 pu, respectively.

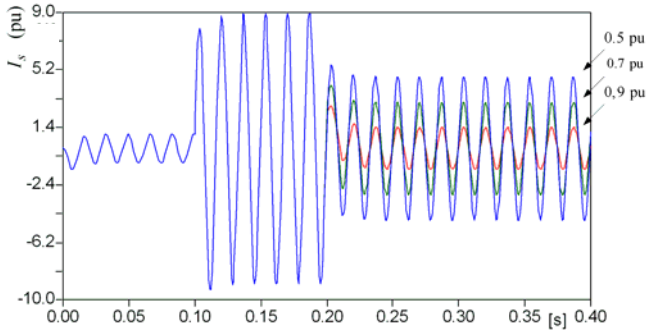

Fig. 9 Current reduction with series voltages of 0.5 pu, 0.7 pu and 0.9pu

The series voltage increase has a substantial impact on the current reduction, lowering its magnitude to almost the values of steady state operation, which could be handled by the electronic switches.

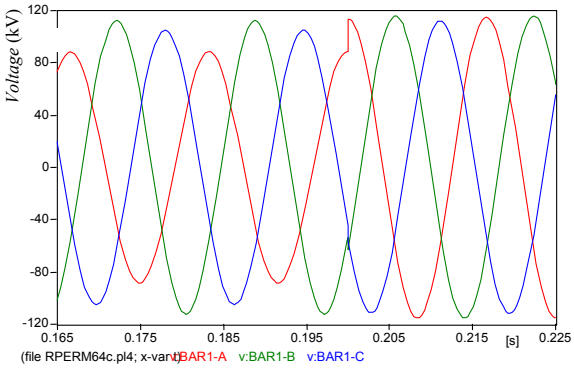

Fig. 10 Substation voltage levels with series voltages of 0.9pu

Such high series voltages inserted on phase *a* at 0.2s do not cause overvoltages in the substation, as shown in Fig. 10.

IV. CONCLUSIONS

Fundamental aspects of AC series voltages insertion to the power system during fault conditions were presented in this paper. It presented basic aspects to get effective short-circuit limitation through series voltage insertion in the network, taking into account the effect of healthy phases in unbalanced faults. Although the analysis focused mainly three-phase and phase-to-ground faults, it could easily be extended to faults of other types.

The magnitude of the series voltage plays a very important role and the eventual use of higher values than that of steady state operation, during short periods, can reduce the undesirable effects of short-circuit currents.

The current limitation strategy also needs to take into account the magnetic circuit of the series coupling transformer so as to avoid saturation and admit the best voltage relation on primary and secondary windings. This topic and also

applicable control strategies are left to further research, as they are related to specific design of such equipment.

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