Real-Time Simulation of Modular Multilevel Converters for Network Integration Studies

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***Abstract*—Modular multilevel converters (MMC) present a major challenge for electromagnetic transient simulator due to their high number of semiconductor devices and node count yielding a very large and cumbersome admittance matrix that needs to be refactored at nearly each time step. Following a brief presentation of this new generation of voltage source converters (VSCs) and its control, this paper describes an efficient decrease and conquer modeling of the MMC topology that is well-suited for parallel processing, allowing real-time performances for hardware in the loop (HIL) simulations. An MMC-based VSC-HVDC 50-km transmission link is used to demonstrate the proposed modeling and illustrate its usefulness for studying network events such as rapid power transmission reversal and major grid voltage drops.**

***Keywords*: Decrease and conquer algorithm, electromagnetic transient (EMT), hardware in the loop (HIL), HVDC transmission, modular multilevel converter (MMC), parallel computing, real-time simulation, voltage source converter (VSC).**

I. Introduction

The latest voltage source converter (VSC) technology provides undeniable advantages over conventional line-commutated converters (LCC) at the cost of slightly higher losses. These new VSCs, usually referred to as modular multilevel converters (MMC), use a very high number of levels, two orders of magnitude more than earlier VSC technology with lower commutation frequencies to achieve an impressive spectral purity, which greatly reduces or eliminates the need for filters on the network side of the converter, and reduces losses to LCC comparable levels [1]. Furthermore, at the electrical and mechanical levels, this topology easily lends itself to a modular implementation, which facilitates development, deployment and maintenance, while reliability is effortlessly enhanced by increasing the number of modules installed.

Major manufacturers have embraced this new technology, as can be observed from their product portfolio and related projects are beginning to sprout [2]-[6].

Simulation is an essential tool for the design, validation and fine-tuning of power systems. However, power electronics have always been problematic to incorporate in power network simulations because of their topology-changing nature and their switching frequencies that tend to be much higher than AC network frequency. Earlier VSC technologies were troublesome because of their high switching frequencies and high harmonic content but now, with MMCs, the difficulties lie with the large number of switching elements contained in the whole VSC. For example, the Trans Bay Cable Project requires 216 modules per half-phase, each containing two IGBT/diode elements, for a grand total of 2592 switching elements in one converter. In light of this information, it is easy to understands that complete and highly accurate switching device modeling, such as SPICE modeling, is completely out of reach with current computational technology and that some form of simplification is required to accomplish network integration, stability or hardware-in-the-loop (HIL) studies.

Some authors have proposed the use of switching functions to represent the switching devices [7]-[8] and others have proposed Thevenin equivalent for the converter arms [9]-[10]. The first approach is interesting under normal operating conditions because it is computationally simple and fast and harmonics are correctly represented but modeling of the diodes, of the losses and internal faults is far from simple with this technique. The second approach consists in bundling all the elements of one arm into one voltage source equivalent but it still requires solving the equations for all the underlying elements with usual switch device models. This "decrease and conquer" technique reduces each mathematical system to a more manageable size. While still computationally intensive, this approach retains all the characteristics of the switching device model used and easily allows the modification of the topology during the simulation for representation of internal faults and other abnormalities.

The current paper adopts the second approach to reduce each arm of the converter to a single Norton equivalent inserted in the power network. Once nodal voltage equations are solved, the voltage and current for each switching element are determined analytically. Natural switching of the diodes is faithfully represented with a precision switching algorithm.

The rest of the paper is divided as follows. The next section briefly presents the MMC topology and the controller employed in this work; the third section describes the modeling and decoupling technique and discusses the real-time performances obtained. A realistic VSC-HVDC system is used as an application example in Section IV and concluding remarks are given in Section V.

II. MMC Topology and Control

Before going into the detail about the MMC modeling, a brief overview of the MMC structure and its basic control loops is given.

A. Topology

As seen in Fig. 1, the simplified MMC topology consists of three phase units, each composed of two arms, stacks of *N* power modules (PM) with serial choke reactor. The internal details of a power module are presented in Fig. 2. An active

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module has its capacitor in circuit (switch 1 on and switch 2 off) thus presenting a certain voltage V_c to the circuit, while an inactive one (switch 1 off and switch 2 on) shorts node P and M. While different manufacturers and/or authors have slightly different terminology and PM internals, the general idea is the same: multiple identical units stacked in each arm, individually controllable, synthesizing with high fidelity a certain reference voltage.

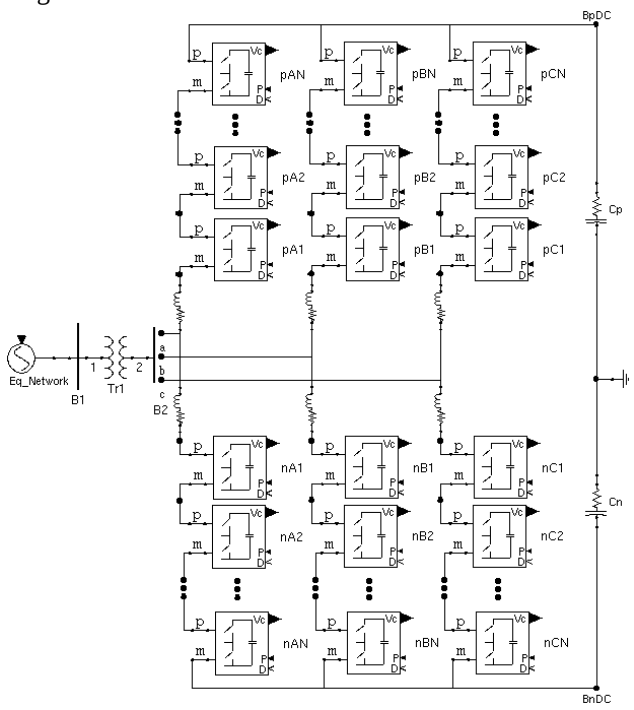

Fig. 1. MMC topology.

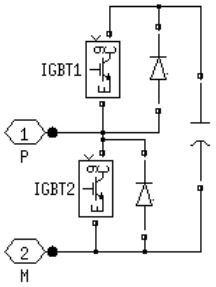

Fig. 2. Power module internal details.

B. Main Control

An MMC, like a VSC, has the ability to control both active power (or DC bus voltage level) and reactive power (or AC voltage level). This ability is quite attractive and very complex control schemes can be developed to exploit it to its fullest extent but, since the focus of this paper is not the possible control strategies of MMCs, simple P-Q and V_{dc}-Q controllers are rapidly presented.

The P-Q controller, used on the rectifier side of an HVDC link, is illustrated in Fig. 3. The first part of the controller is the P-Q PI regulation loop with direct feed-forward of I_d-I_q using measured DC bus voltage (Fig. 4). Once reference values for I_d and I_q are determined, PI regulation of direct and quadrature currents yields V_d-V_q used to generate the voltage reference.

On the inverter side of an HVDC, a V_{dc}-Q controller can be used (Fig. 5). In this case, the active power setpoint is the output of PI regulation of the DC bus voltage V_{dc}. Otherwise it is identical to the P-Q controller.

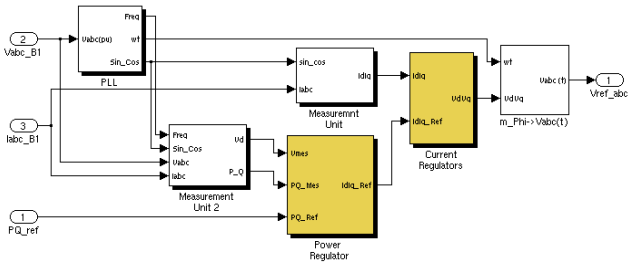

Fig. 3. Basic MMC controller.

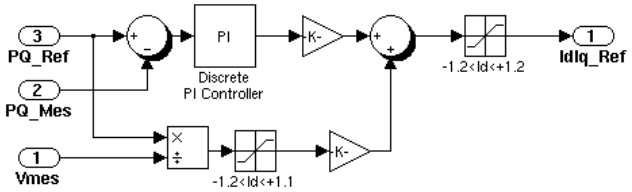

Fig. 4. Basic PQ controller with feed-forward.

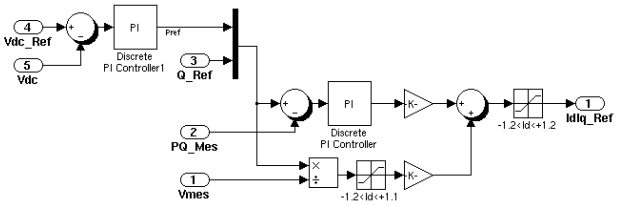

Fig. 5. Basic V_{dc}-Q controller with feed-forward.

C. Power Module Control System

Once reference voltages are determined, the power module control (PMC) system is responsible for the pulse generation sent to the power modules. In order to synthesize the correct waveform using the available PM, the PMC must select the most appropriate combination of capacitors to be activated (i.e. put into the circuit). Several strategies are possible [10]-[12].

The present paper relies on the nearest-level method for PM selection. This scheme has the benefit of being simple yet efficient and it inherently provides loose balancing of capacitor voltages.

The selection is primarily based on the arm current: for a positive current, the weakest capacitors are brought into service to build the necessary arm voltage and to charge them up. In the case of a negative arm current, the strongest capacitors are selected since this will bring down their voltage. This selection method is quite straightforward but some sort of mechanism must be employed to prioritize already active modules over inactive ones to reduce PM switching frequency. Without this priority mechanism, switching frequency and losses would be very high as the optimal selection is different at each time step. On the other hand, the spectral purity of the synthesized voltages would greatly suffer from an overly strict priority system. All in all, the priority mechanism is a tradeoff between harmonic distortion and switching losses. However, as the number of PMs per arm goes up, the overall harmonic distortion goes down, since the granularity of the voltage synthesizer is much higher, and the switching frequency's impact on it is reduced. As a rule of thumb, adequate results are obtained with average switching frequencies around 2-4 times the desired voltage fundamental frequency with 30 and more PMs per arm.

III. Modeling and Real-Time Performances

Direct simulation of the MMC structure with conventional EMT models yields incredibly large equation systems, resulting in impractical execution times as demonstrated by [9]. In the same fashion as [9]-[10], arms are represented with an equivalent, here as a Norton equivalent instead of a Thevenin. In the modeling presented, the arm subsystem is then solved using a simple analytical solution derived from circuit laws instead of a full-fledged equation system solved by matrix computations. Furthermore, those calculations easily lend themselves to parallel computation, as shown later in subsection B.

A. Arm equivalent

Before constructing the arm equivalent, the module equivalent must first be determined. As mentioned earlier, each module contains two switching devices and a capacitor. Each switching device is represented by a R_{on}/R_{off} resistor and the capacitor by its EMTP equivalent (current source in parallel with an equivalent resistor) as seen in Fig. 6 (a). Each module is then reduced to a single Norton equivalent (Fig. 6 (b)) where equivalent admittance and current injection for module *n* are derived as follows:

$$\begin{aligned} Y_{eq1_n} &= (R_{sw1_n} + R_{c_n})^{-1} \\ Y_{eq2_n} &= (R_{sw2_n})^{-1} \\ Y_{eq_n} &= Y_{eq1_n} + Y_{eq2_n} = (R_{eq_n})^{-1} \end{aligned} \tag{1}$$

and

$$I_{eq_n} = R_{c_n} I_{c_n} Y_{eq_n} . \tag{2}$$

The arm equivalent is then simply the Norton equivalent of several modules linked together. The total admittance contribution is then

$$(Y_{eqTot})^{-1} = R_{eqTot} = \sum_{n=1}^{N_{PM}} R_{eq_n} \tag{3}$$

and the total equivalent current injection is given by

$$I_{eqTot} = Y_{eqTot} \sum_{n=1}^{N_{PM}} R_{eq_n} I_{eq_n} . \tag{4}$$

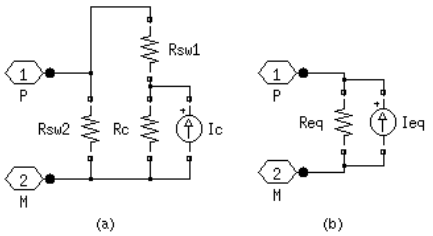

Fig. 6. Power module modeling (a) and equivalent (b).

Determining the exact conditions of each individual module is then simple since the current flowing between the AC and DC nodes is easily calculated and all the modules' current injections are known. This task, by its nature, is well-suited for recursive divide and conquer algorithms.

This method has the characteristic of retaining all the operating details of the switch devices (i.e. IGBT/diode states, currents, voltages and parameters) since they are necessary for determining the arm equivalent. Under certain circumstances, this level of detail may be unnecessary but for HIL simulation of controllers, the ability to represent abnormalities and parametric differences between arms and/or PMs is a major advantage.

Mathematically speaking, using this representation is quite advantageous since all the internal nodes are removed from the nodal equation system, hence reducing the admittance matrix size and the computational cost of its factorization or inversion, depending on actual solver algorithm. Furthermore, computing the arm equivalent is a simple, albeit tedious, task that only requires the voltage at both extremities and prior knowledge of the operating conditions of the arm PMs , making it a perfect candidate for parallel computation. Taking advantage of this fact makes it possible to seamlessly partition the mathematical burden of large MMC-VSCs.

B. Mathematical decoupling

In the field of power system simulation, several decoupling methods exist to partition large network into a group of smaller ones in order to reach real-time performances. These methods typically rely on physical delays, such as the ones introduced by transmission lines or the presence of high-inertia elements that tolerate a time delay, usually large inductive or capacitive reactors depending on the nature of the signal to be delayed. This last approach is not always simple to apply since non-linearities on either side of the decoupling point can destabilize the whole simulation and, more often than not, this method introduces power imbalances.

With the current VSC modeling, there is an opportunity to partition the computational burden by mathematical parallelization of the system. As mentioned in the previous section, the VSC is reduced to six arm equivalents that contribute to the admittance matrix and the current injection for the voltage calculations. By tasking a processing core for each arm equivalent, a theoretical six-fold reduction in execution time is possible. Needless to mention that once again, communication time impedes the reduction but, nonetheless, appreciable performance gains are observed.

As illustrated in Fig. 7, six processing cores are required for the simulation of one converter and its related AC and DC networks. The main processor is responsible for the voltage calculations as well as one arm equivalent. Once the admittance and current contribution of its arm equivalent are determined according to the firing pulses, the main processor must wait for the Y_{eqTot} and I_{eqTot} contributions of the coprocessors. This inactive period is short since all processors are synchronized at the start of the time step and they all have an almost identical task to execute. After all arm equivalents are updated in the main processor, necessary steps are taken to compute node voltages, which are then transmitted to all coprocessors to calculate PM conditions. Finally, the natural switching of the diodes is considered.

Since everything is done within one time step, no artificial delays or power imbalances are introduced. In other words, this technique and intra-step communications allow for a seamless division of the computational load. It could be applied to other cases as well.

C. Performances

This MMC modeling was implemented in the Hypersim real-time simulator [13] with satisfying results. The model can be run with or without the mathematical decoupling when real-time performances are not required and not enough processing cores are available. With the mathematical decoupling enabled, the coprocessor processes are seen as a regular Hypersim simulation task. Hence, data acquisition, IOs, simulation snapshot and all other regular simulation actions are available.

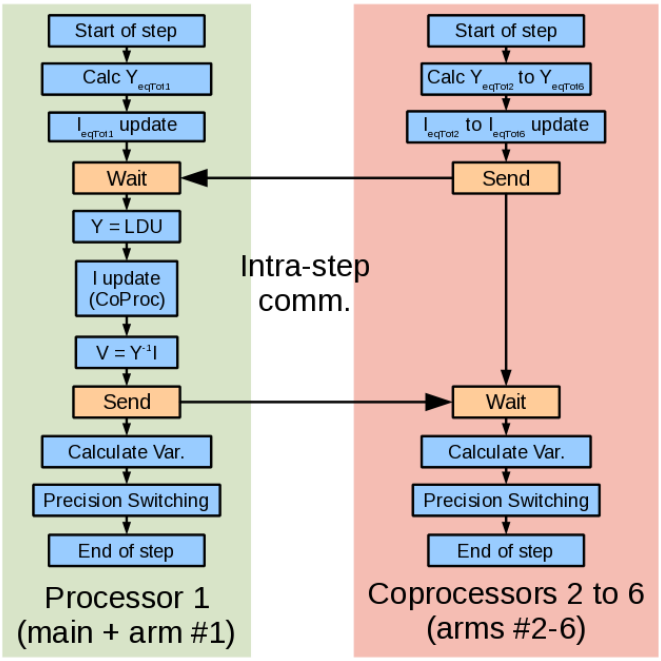

Fig. 7. Converter parallel simulation flowchart for one simulation time step.

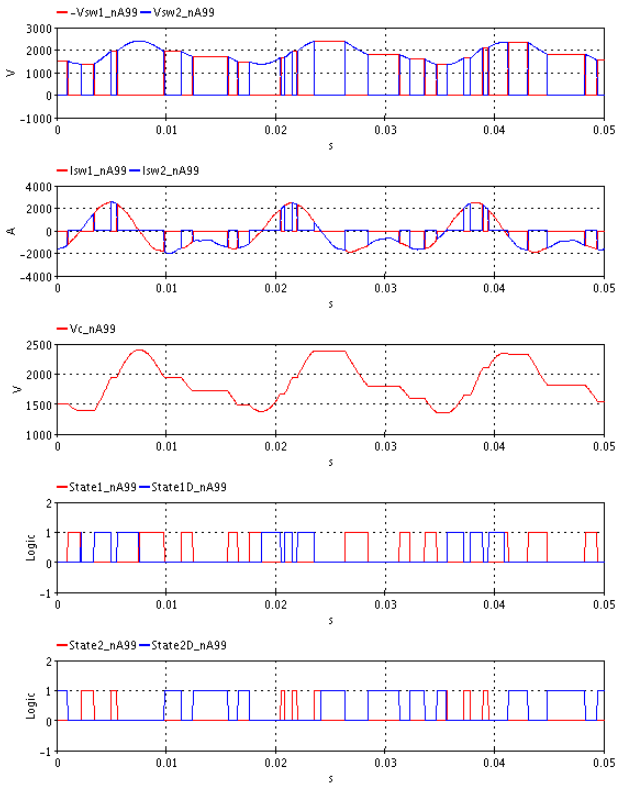

Fig. 8. Switch voltages and currents, capacitor's voltage followed by IGBT and diode states for power module 99 of the lower arm of phase A.

A single MMC connected to equivalent AC and DC networks was used to quantify performances. Without mathematical decoupling, MMCs with 30 PMs per arm can be simulated in real-time with multiple IOs on an Sgi Altix 4700 with Intel's Itanium 2 processors. With decoupling, a little over 110 PMs per arm are possible to simulate in real-time using the same time step and still with multiple IOs. Figs. 8 and 9 were obtained during real-time simulation of the HVDC system presented in the next section (see Fig. 10).

If real-time performances are not required, the offline mode of Hypersim can be used to efficiently simulate large MMCs. For example, a 216 PM per arm MMC has an average execution time per step around 20% slower than real-time.

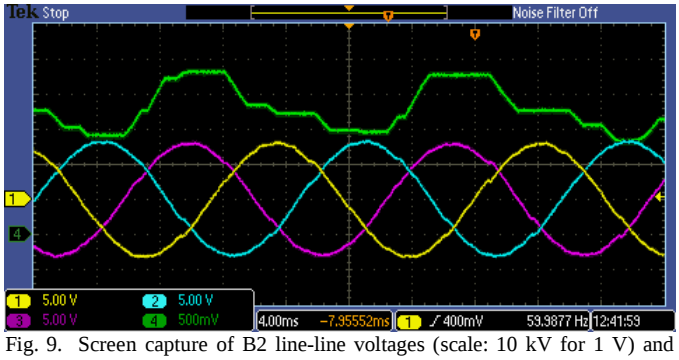

Fig. 9. Screen capture of B2 line-line voltages (scale: 10 kV for 1 V) and capacitor voltage of a power module (scale: 1kV for 1 V).

IV. Application Example

The usage of the proposed modeling will be illustrated through real-time simulation of a complete VSC-HVDC link (see Fig. 10). Two 60 Hz equivalent networks, one operating at 120 kV and the other at 230 kV, exchange energy through an ±100 kV MMC-based HVDC transmission system. Unlike the LCC technology, VSCs do not require AC filters or impose boundaries on the short-circuit level of the related network. In this example, both equivalent networks present a very low short-circuit level (450 MVA) compared to the converter's nominal power rating of 225 MVA.

The DC transmission system is composed of capacitive filters and a 50-km cable. This represents an underground or submarine cable that would be used for connecting on/offshore wind power plants or for crossing natural obstacles where overhead lines are difficult and/or too costly to install.

Each MMC, rated at 225 MVA, sports 108 power modules per arm followed by a choke reactor. Each module contains a single cell with a 2 kV nominal voltage on a 6 mF capacitor. In this example, the whole HVDC system contains 5184 individual semiconductors since the total switching device count in a single converter reaches 1296, or 2592 individual semiconductors.

The whole system is simulated in real-time on an Sgi Altix 4700 equipped with Intel's Itanium 2 processors. Each VSC and its related AC network requires six cores. As explained earlier, one core solves the nodal equations plus one MMC arm while the other five arms are computed on the other cores.

In the following subsections, the HVDC system is subjected to a drastic power setpoint change and a single line-to-ground fault on B1 to demonstrate the real-time simulation possibilities that are now accessible.

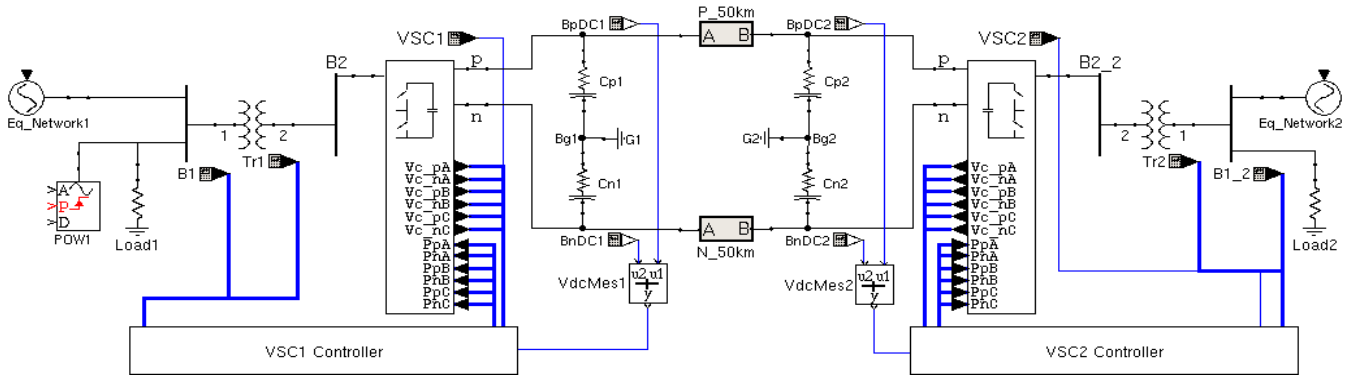

Fig. 10. 225-MVA ±100 kV VSC-HVDC 50-km link system.

A. Power order change

As shown on Fig. 11, VSC1 initially sends +200 MW on the HVDC link while providing 90 MVar to equivalent network 1, maintaining bus voltage near its nominal value. At the other end of the link, VSC2 regulates DC voltage at 200 kV while giving 10 MVar to equivalent network 2. Three cycles after the start of the acquisition, the power reference value of VSC1 is ramped from +200 MW down to -50 MW in 200 ms (-1.25 GW/s). During the power flow reversal, the DC bus voltage presents a serious drop, around 60 kV but, as illustrated in Fig. 12, the impact on both AC network is very limited. Furthermore, the nearest level selection method employed allows a nearly equal sharing of the voltage drop among all the capacitors of each arm due to its inherent voltage balancing.

TABLE I
SIMULATED VSC-HVDC LINK PARAMETERS

AC systems	AC 1	AC 2
V_{bus1} (L-L kV)	120	230
Short-circuit level (MVA)	450	
Load (MW)	50	
Transformer (Y_g-Δ) (L-L kV)	120/55	230/55
$S_{nominal}$ (MVA)	225	
$X_{leakage}$ (pu)	0.12	
Transformer's X/R ratio	30	
DC system	VSC 1 & 2	
PM per arm	108	
L_{arm} (H)	0.015	
R_{arm} (Ω)	0.050	
C (mF)	6	
$V_{c\ nominal}$ (kV)	2	
R_{on}/R_{off} (Ω)	1e-3 / 1e6	
DC filter C (µF)	5	
DC filter R (Ω)	1	
Cable length (km)	50	
Cable R (Ω/km)	0.0139	
Cable L (mH/km)	0.159	
Cable C (nF/km)	231	

This kind of simulation is very useful for control strategy development and validation using mathematical model of the controller due to the fast execution times. It is even more interesting when replica or actual controllers are connected to the real-time simulator for HIL testing since the real behavior of the controller, due to all its real implementation details, can be observed and quantified for fine tuning the controller's setting and parameters.

B. Single line-to-ground fault at B1

The initial operating point is the same as previously described. Three cycles after the start of the data recording, a single line-to-ground fault is applied at bus bar B1 on phase A. Once the fault is cleared, after a delay of 100 ms, both controllers are able to bring the system back under control and resume the 200-MW power transfer. Bus B1 and B2 voltages and other related waveforms are illustrated in Fig. 13.

This example could be used as the basis for more complex network integration studies by replacing the equivalent networks with a more detailed representation of both power systems such has the one used in [14]. Even with such a large network, HIL simulations could still be possible and would provide invaluable insights into possible interactions between the VSCs and other equipment such as synchronous and static compensators, wind power plants and LCC-HVDCs interconnections for example.

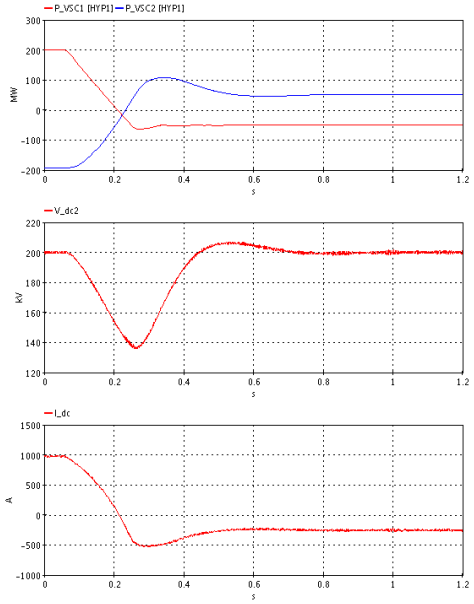

Fig. 11. MMC absorbed power, inverter-side DC voltage and DC current in the 50 km link during a partial power reversal (VSC1 goes from 200 MW to -50 MW in 0.2 s (1.25 GW/s)).

Furthermore, the proposed modeling is beneficial for both real-time and offline simulations. If real-time performances are not required, MMCs with any number of power modules per arm could be simulated in much timely manners than without the parallel computing of module conditions. Hence, offline EMT or stability studies of very-high-voltage MMCs (i.e. 400+ PMs per arm) connected to large tightly-meshed power networks, which are difficult to partition for parallel computing, are possible with the method presented here.

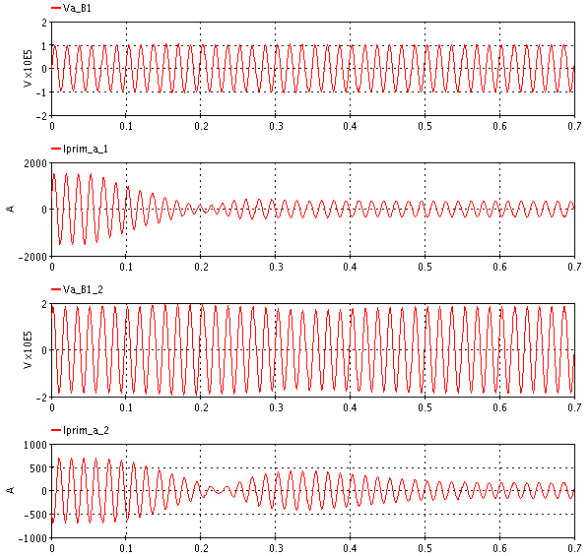

Fig. 12. Voltage of bus B1 and transformer primary currents (phase A only) for both equivalent networks.

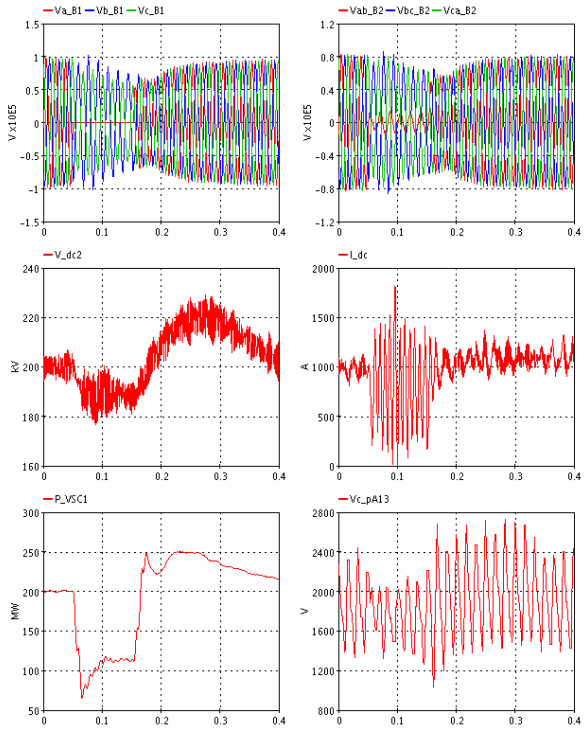

Fig. 13. System waveforms during a single line-to-ground fault on phase A (B1 L-g and B2 L-L voltages, VSC2-side DC bus voltage, DC link current, VSC1 absorbed active power and PM pA13 capacitor voltage).

V. Conclusions

As with any other major projects, power utilities have to perform extensive simulation studies before installing multilevel voltage-source converters into their network to evaluate their impacts. In order to do so, simulation tools, such as the one presented in this paper, will be required to conduct stability and network integration studies as well as HIL studies to fine-tune the controllers and identify and evaluate interactions with other network devices.After a brief presentation of MMC technology and its controller, the current paper presented a parallel modeling of the MMC topology. The proposed method allows drastic reductions in the execution time, making real-time simulation a reality, without losing the details of the switching elements or the ability to represent abnormal operations and internal faults. This makes possible the rapid development and validation of control strategies as well as providing a swift and powerful tool for all sort of electromagnetic transient and even stability studies of very large power networks with MMCs. Finally, this modeling approach was demonstrated in real-time with a 225-MVA ±100 kV VSC HVDC 50-km link with 108 power modules per arm.

Efforts will be made in future work to further expand our real-time simulation capabilities of MMC and other topologies and to use this simulation tool in other application contexts such as more detailed HVDC interconnection simulations and offshore wind power plants integration studies.

VI. References

[1] B. Gemmell, J. Dorn, D. Retzmann, D. Soerangr, "Prospects of Multilevel VSC Technologies for Power Transmission," Conf. Rec. IEEE TDCE, pp. 1-16, 2008.

[2] ABB Power T&D Solutions > HVDC http://www.abb.com/hvdc.

[3] Siemens HVDC PLUS (VSC Technology): References, http://www.energy.siemens.com/us/en/power-transmission/hvdc/hvdc-plus/references.htm.

[4] ABB HVDC Reference Projects in Europe > DolWin1 http://www.abb.com/industries/ap/db0003db004333/8b74a5fe4cc03e44c125777c003f3203.aspx.

[5] Alstom, "Alstom Grid Selected to Provide HVDC Converter Assets for Tres Amigas SuperStation," Press release, Oct. 21, 2010, http://www.alstom.com/us/news-and-events/press-releases/tresamigasHVDC/.

[6] Siemens AG, "Ready for the future: Siemens erects power converter stations for HVDC link between France and Spain as part of the Trans-European Network," Press release, Jan. 12 , 2011, http://www.siemens.com/press/pool/de/pressemitteilungen/2011/power_transmission/EPT201101032e.pdf.

[7] J.-N. Paquin, C. Dufour, L.-A. Grégoire, J. Bélanger, "Real-Time Simulation of a 180-cell 720 switch Modular Multilevel Converter for HVDC Transmission Studies," Cigré Canada Conf. on Power Systems, Vancouver, Canada, Oct. 17-19, 2010.

[8] L.-A. Grégoire, J. Bélanger, C. Dufour, "Solvers for Real-Time Simulation of Bipolar Thyristor-Based HVDC and 180-cell HVDC Modular Multilevel Converter for System Interconnection and Distributed Energy Integration," will be presented at Cigré Int. Symp. Recife, Pernambuco, Brazil, April 3-8, 2011.

[9] U.N. Gnanarathna, A.M. Gole, R.P. Jayasinghe, "Efficient Modeling of Modular Multilevel HVDC Converters (MMC) on Electromagnetic Transient Simulation Programs," IEEE Trans. Power Delivery, vol. 26, pp. 298-306, Jan. 2011.

[10] Q. Tu, Z. Xu, "Impact of Sampling Frequency on Harmonic Distortion for Modular Multilevel Converter," IEEE Trans. Power Delivery, vol. 26, pp. 298-306, Jan. 2011.

[11] M. Hagiwara, H. Akagi, "Control and Experiment of Pulsewidth-Modulated Modular Multilevel Converters," IEEE Trans. Power Electronics, vol. 24, pp. 1737-1746, July 2009.

[12] J. Rodriguez, L. Moran, P. Correa, C. Silva, "A Vector Control Technique for Medium-Voltage Multilevel Inverters," IEEE Trans. Industrial Electronics, vol.49, pp. 882-888, Aug. 2002.

[13] D. Van Que, J.C. Soumagne, G. Sybille, G. Turmel, P. Giroux, G. Cloutier, S. Poulin, "Hypersim--an integrated real-time simulator for power networks and control systems," Proc. Int. Conf. Digital Power System Simulators, Vasteras, Sweden, May 1999.

[14] R. Gagnon, G. Turmel, C. Larose, J. Brochu, G. Sybille, M. Fecteau, "Large-Scale Real-Time Simulation of Wind Power Plants into Hydro-Quebec Power System," 9th Int. Workshop Large-Scale Integration Wind Power into Power Systems & Transmission Networks for Offshore Wind Power Plants, Quebec, Canada, Oct. 18-19, 2010.