Validation of a 60-Level Modular Multilevel Converter Model - Overview of Offline and Real-Time HIL Testing and Results

Luc-Andre Gregoire, Wei Li, Jean Belanger, Laurence Snider

***Abstract*-- In this paper, full real-time digital simulation of a static modular multilevel converter (MMC) HVDC link interconnecting two AC networks is discussed. The converter has 60 cells per arm; each cell has two power switches with anti-parallel diodes and one capacitor. The simulated model can be used to study the natural rectifying mode, which is very important in the energizing process of the converter, whether a ramping voltage or a charging resistance is used. The model also incorporates a simple controller to show the system behavior in different operating conditions. The converter model and the controller are simulated on two independent real-time simulators and connected though their respective IO and physical signal cables to perform Hardware-in-the-Loop testing. All capacitor voltages are supplied to the controller using digital to analog converters. Firing signals from the controller are sent using digital signals with opto-couplers, as would be the case with a real setup. By doing so, a Hardware-in-the-Loop (HIL) simulation is obtained. The main challenges of this setup are the very high number of IOs, which reaches over 730, considering both controller and converter, and the processing power required to simulate the 360 cells within a small time-step of 50 µs or less, as required for electromagnetic transient analysis. The simulation is achieved with a time-step of 20 µs using 10 INTEL 3.2-Ghz processor cores. Different faults are applied to determine their effects on the controller and the converter. In order to produce results that are as realistic as possible, a saturable transformer is used; the impact is particularly noticeable during faults and unbalanced load. The real-time digital simulator used is based on MATLAB, SIMULINK, SimPowerSystems and eMEGAsim.**

Keywords: Multilevel voltage source converter, real-time simulation, hardware in the loop

I. Introduction

The global power system infrastructure is rapidly changing; from concentrated generation centers and Extra High Voltage (EHV) transmission grids towards increasingly distributed generation/distribution systems. This transformation mandates expanded use of power electronic devices: e.g. HVDC, FACTS and interfacing devices for DC and variable-frequency power sources (photovoltaic, wind generation). Power electronic converters have evolved rapidly, both in terms of available electronic switching devices and converter topologies. The evolution from thyristor-based converters to voltage source converters (VSCs) to modular multilevel converters (MMCs) [1-7] has placed increasingly onerous demands on simulation technology, in particular real-time digital simulators. The challenge related to the simulation of VSCs, for example, is the very small time-step required to deal with relatively high carrier frequencies, and models have been developed that achieve accurate results using time-steps in the range of 20 to 50 microseconds [2], typical of what may be achieved using standard INTEL/AMD multi-core processors. MMCs add to this challenge because of the large number of I/Os required monitoring the voltages of a large number of cells. The main objective of this development is to meet this challenge. [3-4]

In this study, a real-time digital simulation of an MMC-based back-to-back bipole HVDC interconnecting two AC networks is presented. Such ac-dc-ac converter systems can be used, for example, for low-voltage converters used in the integration of distributed generation systems, such as wind farms.

In the system presented in this paper, the sending-end and receiving-end converters, as well as the sending-end controller, are modeled together on the same multi-core real-time digital simulator. The receiving-end controller is simulated in a separate simulator and interconnected through IOs and cables, enabling HIL testing of an MMC. The transformer models include their respective core saturation characteristics, providing for a realistic evaluation of the performance of the converters in the face of ferromagnetic nonlinearities.

The specific objectives are to demonstrate accurate simulation of the MMC converter (note that the reliability of the controller is not the subject of the study). And to demonstrate the capability to simulate large MMC models with large numbers of I/O channels for HIL applications, using a time-step value in the range between 20 and 50 microseconds.

Verification studies present results of several applications of this model, including natural rectifying mode (without a controller) enabling evaluation of the energizing process of the converter, using a ramping voltage or a charging resistance. The performance of the converters in the face of AC system faults is also presented.

II. Modular Multilevel Converter Topology

The converter topology is presented in Figure 1. The system comprises an HVDC converter system, equipped with two 60-

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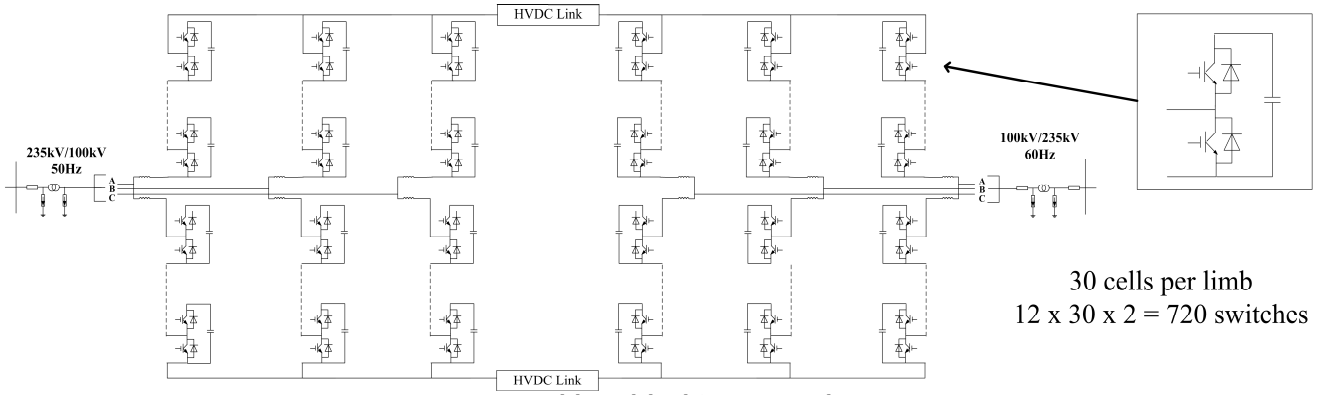

Figure 1 Modular Multilevel Converter Topology

level Modular Multilevel Converters (MMC). Each converter has 60 cells per arm, with each cell having two power switches with anti-parallel diodes and one capacitor. This topology requires some 720 I/Os linking the converters and controllers; the capacitor voltage of each cell must be fed from converter to controller, and firing signals must be fed (through opto-couplers) from the controller to the switching devices of the converter.

A. Real-time model:

The setup used for the study is presented in Figure 2. Real-time simulation with Hardware-in-the-Loop (HIL) was achieved in full numerical mode using two real-time computers connected by analog and I/O lines. Notwithstanding the onerous requirements, real-time simulation was achieved with a time-step of 20 microseconds on standard dual six-core PC platforms using only 9 INTEL 3.3-Ghz processor cores. The simulation software is based on MATLAB, SIMULINK, SimPowerSystems [8] and RT-LAB [9]

In HIL [10-11] mode, two independent real-time simulators are used to simulate the plant (Target 1) and the controller (Target 2) and are interfaced with 360 analog/digital IO signals. The controller of the right-side HVDC converter is simulated on the Target 2 simulator while the controller of the left-side converter is simulated on the Target 1 simulator, together with the plant model. Figure 2 also shows how the model is separated for parallel simulation on nine (9) processor cores. All processor cores are interfaced by high-speed on-chip shared memory. Seven processors are used for the converters while one processor is used for the controller and one processor is used for the AC network model.

The same setup is used for fully numerical simulation mode except that the controller of the right-side converter is also simulated on a separate processor core of the Target 1 computer. In this case, the communication between the controller and the plant model is made through shared memory instead of IO converters.

B. Comparing Results with Reference Case using a One Microsecond Time-Step

The results obtained with OPAL-RT real-time models are compared with those obtained from a reference model simulated off-line (non-real-time) using a 1 microsecond time-step. The reference model, called the SPS model, uses the same configuration and parameters as the OPAL-RT real-time models, in addition to using the universal converter bridge model from the SimPowerSystems (SPS) library. Note, that while the standard universal bridge model is very accurate, it cannot be used in real-time simulation since its state-space matrices must be continuously recomputed during the simulation, leading to very lengthy and non-constant processing times. Furthermore, the SPS universal bridge model does not simulate the effects of firing events occurring within the model simulation step since SPS uses a very accurate variable-step solver, iterating at each switching event – clearly not suitable for a real-time solution. Consequently, the OPAL-RT real-time model uses the SPS standard model library for transformers, inductors, resistors and capacitor, and the OPAL-RT MMC cell model with OPAL-RT's ARTEMiS solver, which is optimised for real-time simulation with a time-step in the range of 20 to 50 microseconds.

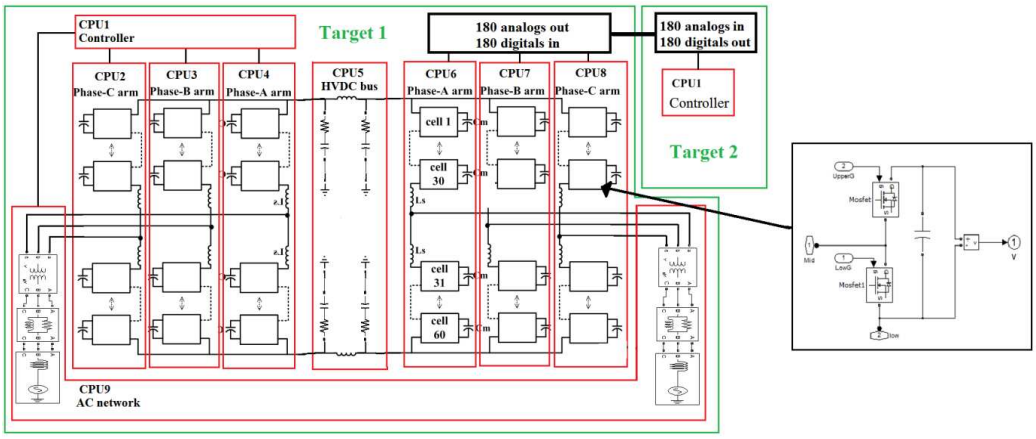

Figure 2 Real-Time Simulator configuration & model distribution for HIL test

C. *The Controllers*

The controllers used for the static converter can regulate the voltage of the capacitor cell, but the amplitude and the angle of the PWM reference voltages must be set manually. OPAL-RT's RT-Events control block library is also used for accurate generation of firing pulses occurring within the model's time-step.

While this is a very simple controller, it is adequate for testing the plant model under a number of balanced and unbalanced steady-state and fault conditions. (It must be noted that the objective of this study is to evaluate the feasibility and performance of the simulator and not to develop a controller. The method used for the controller was inspired by [5-6])

III. SIMULATION RESULTS

A. *Natural rectification mode – Fully Numerical Mode – 20 microseconds*

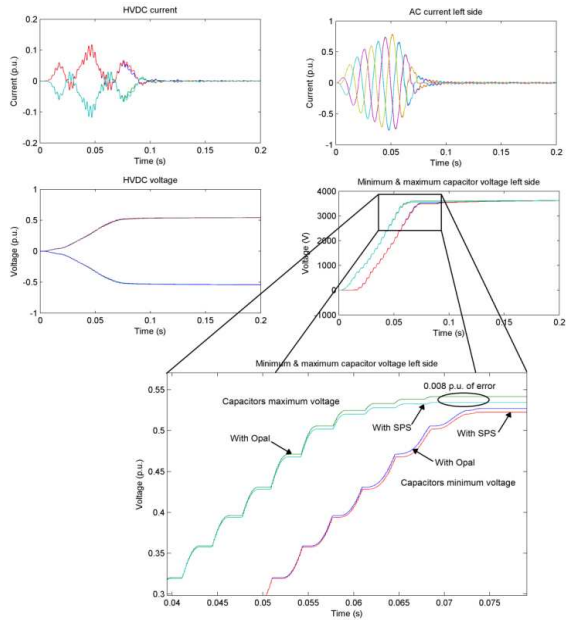

Figure 3 Natural rectifying mode - SPS and Opal-RT model results superimposed.

Figure 3 presents results obtained with the proposed real-time model using a time-step of 20 microseconds, superimposed with the results obtained with SPS at 1 microsecond, where the system operates in natural rectification mode during the charging phase. As shown in Figure 3, the waveforms achieved in both cases are very close to each other. The maximum difference is less than 0.015 p.u., making it acceptable for real-time HIL testing,

Figure 3 verifies the behaviour of the system during the charging of the capacitor for all 180 cells. The same results are given for the SPS model and for the Opal-RT model. It is easy to see that results are very close. Note that only the minimum and the maximum voltage values of all cells are displayed in the lower right graphic. This indicates that all the capacitor voltage is between that minimum and maximum.

Figure 4 illustrates the results obtained with the proposed model using a time-step of 20 microseconds, superimposed with the results obtained with SPS with a time-step of 1 microsecond, when the system operates in the controlled mode during the steady-state phase. The margin of error between the real-time 20 microsecond model and the 1 microsecond SPS model is less than 0.025 p.u..

B. *Fault Condition – Fully Numerical Mode – 20 microseconds*

Different faults were applied to the model to test its accuracy during transient conditions. Figure 5 presents the results for a fault applied between phase A and the ground at the location between the AC power supply and the power transformer. The HVDC bus voltages and currents are shown. Results obtained with the real-time model running at 20 microseconds compare very well with results from the model running at 1 microsecond, with the margin of error ranging between 0.02 p.u. and 0.01 p.u.

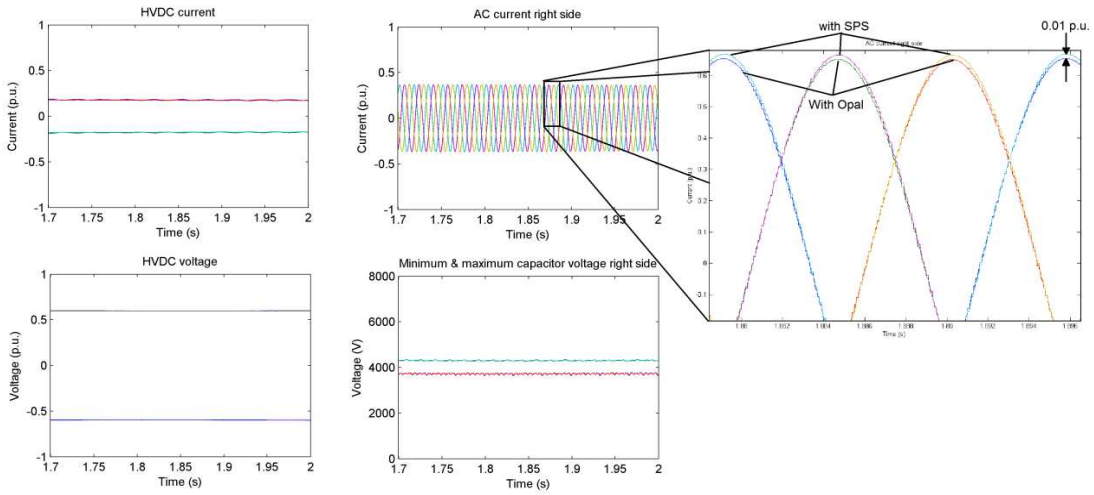

Figure 4 Steady state for HVDC bus at 0.6 p.u – SPS and Opal-RT model results superimposed.

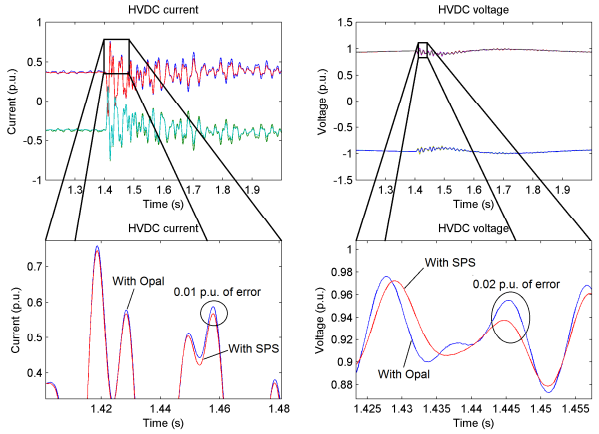

Figure 5 HVDC current and voltage and their error, test FT-2. SPS and Opal-RT model results superimposed

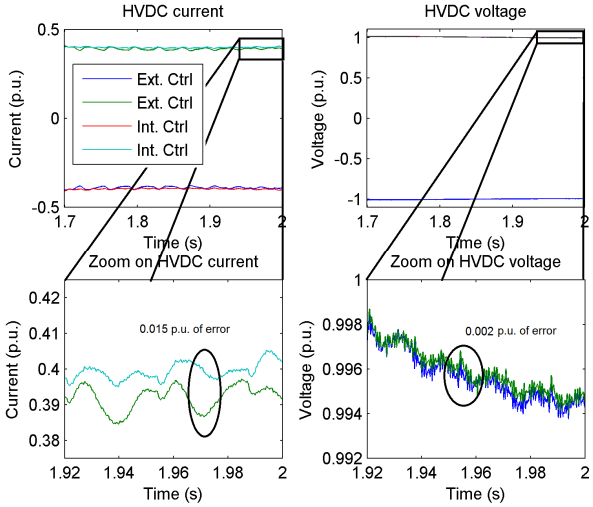

Figure 6 HVDC current and voltage and their error, using external controller.

1) Tests in HIL Mode

The same tests were repeated in HIL mode using two real-time digital simulators: one for the plant and one for the controller. Both simulators (Target 1 and Target 2) are interconnected through their respective I/O systems. A total of 360 analog and digital signals with time stamping are used in each real-time computer, which requires a very high performance I/O system, only available with high-end simulators. Here, 6 OPAL-RT OP5142 FPGA-based IO cards are used. Each OP5142 card has configurable IO for INPUT or OUTPUT, analog or digital. One OP5142 can manage up to 256 channels; note that analog IO requires 2 channels. The PCIe bus is used for communication between the OP5142 and the target CPU.

The controller is synchronised with the AC voltage using a phase-lock-loop consistent with real systems.

The I/O communication delays obtained with the real-controller impact the power flow, while the ideal controller would not include these delays. This explains the lower current on the HVDC bus. However, the voltage of the HVDC bus is still regulated by the internal controller, and will follow the reference of 1 p.u.

The above simulation illustrates the usefulness of HIL testing to analyse phenomena that are often not seen with ideal controllers. A future study will analyse the behaviour of the systems under fault conditions.

Simulation Performance

In order to minimize calculation time to allow real-time simulation, the model is distributed across 11 CPU cores. Table I illustrates the calculation times achieved on each CPU core during real time simulation. T_s is the time-step used during simulation, T_{cal} is the time required for calculation of each subsystem, and $T_{s\ min}$ is the minimum time-step that can be achieved. In this test, $T_{s\ min}$ is 11 microseconds, which means the discrete simulation time-step of this model can be reduced to as low as 11 microseconds. When physical I/Os are added, the simulator will need more time to manage the large number of IOs. Nevertheless, the minimum achievable time-step of the model is still below 20 microseconds.

Table I Real-time simulation's timing performance

CPU frequency3.3 GHz				
cpu	subsystem	T_s (microseconds)	T_{cal} (microseconds)	$T_{s\ min}$ (microseconds)
1	Ac grid	20	2	11
2	Arm-A left	20	3	
3	Arm-B left	20	3	
4	Arm-C left	20	3	
5	Arm-A right	20	3	
6	Arm-B right	20	3	
7	Arm-C right	20	3	
8	Dc link	20	1	
9	PWM gen left	20	5.4	
10	PWM gen right	20	5.4	
11	controller	20*5	3.8	

Table II illustrates the timing performance for two CPU frequencies, if additional subsystems are merged together. This demonstrates the advantage of using multiple CPUs to reduce $T_{s\ min}$.

Table II Timing performance on 6 CPUs

		CPU frq=3.33G		CPU frq=2.4G	
CPU	subsystem	subsystem Tcal (us)	model T_s min (us)	subsystem Tcal (us)	model T_s min (us)
1	Ctrl, ac dc system	6	13	9	19
2	Arms A, B, left side	7		10	
3	Arms A, B, right side	7		10	
4	Arms C left & right side	7		10	
5	PWM generator left	9		12	
6	PWM generator right	9		12	

C. Performance of FPGA-Based HIL I/O System

The HIL tests presented above were conducted using only 180 I/O channels. However, in practice the number of I/O channels can easily reach 2000. Consequently, we evaluated the time required to transfer a large amount of I/O data to and from the main processor memory. The eMEGAsim real-time simulator can include several I/O subsystems, with each I/O subsystem including one FPGA board controlling up to 128 analog I/O converters or 256 discrete I/O channels. The following graph illustrates the minimum time-step that can be achieved when a number of FPGA I/O sub-systems are connected to the real-time computer using a PCI Express switch.

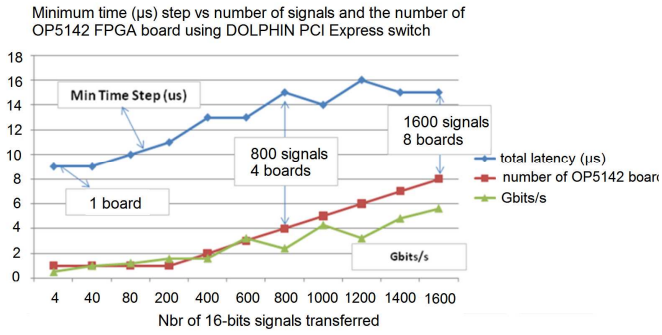

Figure 7 Minimum time-step vs number of signals and OP5142 boards

The above tests do not include any model computation but include all communication overhead and I/O management.

As can be observed, the total performance increases as the number of FPGA boards installed increases, enabling the transfer of very large amounts of data via a high number of I/O channels. This high performance is made possible by the PCI Express communication fabric now installed on all modern PCs. PCI Express uses a high-speed switch capable of transferring data directly to and from processor memory at speeds exceeding 10 gigabits per second. In fact, the new generation of PCI Express switches can reach speeds in excess of 40 gigabits per second. The speed of the PCI Express link used for each OP5142 card is 9 microseconds and can transfer data from only one board at a time. Consequently, the real-time simulation of complex MMC models with a large number of I/Os can only be performed with modern and high-performance I/O systems. The simulations presented in this paper demonstrate that building custom computers is no longer necessary, and may, in many situations, limit overall system performance. This means that a PCI Express switch can handle several OP5142 I/O boards simultaneously, as demonstrated by the Figure 7. In comparison, the old 32-bit PCI bus has a maximum speed of about 1 gigabit per second.

The main results of the studies are the following:

1. The minimum time-step achievable is approximately 9 microseconds using one OP5142 board, without considering MMC model calculation, which is about 3 to 9 microseconds, depending on the number of 3.3-GHz processors used.
2. Total latency remains constant at approximately 13 to 16 microseconds, when the number of signals increases from 400 to 1600 using 2 to 8 boards.
3. Total incremental bandwidth increases from about 1 gigabit per second to 4 gigabits per second when the number of boards increases from 1 to 5. The maximum transfer rate increases to 5.5 gigabits per second with 8 boards.

IV. CONCLUSIONS

1) The proposed MMC converter can be simulated on the presented real-time simulator with a time-step of 20µs or less, even when the number of I/Os exceeds 360 channels.

2) The proposed MMC model, developed by Opal-RT and running at 20 microseconds is sufficiently accurate for control development, design and tests in HIL applications.

3) As expected, test results in HIL mode are slightly different than results obtained in fully numerical mode. This indicates that ideal controllers used for fully numerical simulation should include the simulation of communication delays that will be present with actual controllers.

4) The simulator can be used to simulate the complete system, including the controller in off-line mode, at a speed faster than real time and with an acceleration factor of more than 200 times. This is compared to simulations performed on only one processor at a time-step of 1microsecond.

5) In practice, off-line simulation of such systems with one processor at 1 microsecond is not practical, since the simulation time can be tediously long. For this reason, power electronic manufacturers are still using or contemplating using analog simulators to design and test their controllers. The proposed real-time digital simulator is therefore a very viable alternative.

6) More accurate results could be obtained using a smaller time-step, but this would increase the size

and cost of the real-time simulator or require the use of FPGA processors.

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