EMTP-ATP Modeling of a Resistive Superconducting Fault Current Limiter

Elizaveta Egorova, Himanshu Bahirat, Dr. Bruce A. Mork, Dr. Warren F. Perger, Dr. Matthew Holcomb

Abstract-- **Before application of a superconducting fault current limiter (SFCL) in a power system, it can be useful to confirm performance of the SFCL through simulation studies. This paper presents the development and implementation of a resistive SFCL model in the Alternative Transient Program (ATP) where simulations are performed in time domain.**

The modeled SFCL has four superconducting elements in parallel per phase and can thus operate for three consecutive reclosing operations before locking out. In the ATP model, the resistive behavior of the superconducting elements is controlled by the circuit current only.

This model is applied to a small distribution system of 15 kV to study the fault current limitation and the transients associated with the switching between various elements. The effectiveness is demonstrated, with a reduction in fault current of about 50% on average.

Keywords: **Superconducting fault current limiter (SFCL), Alternative Transient Program (ATP), nonlinear resistance, distribution network, transient recovery voltage (TRV), fault current reduction.**

I. Introduction

DEVELOPMENT of the energy infrastructure requires changes to be made involving interconnection of power systems and adding renewable energy resources. These factors lead to higher fault current levels in the altered system [1]. On the other hand, older but still operational equipment gradually becomes underrated, e.g., some transformers, switchgear, cables, or other underground equipment, can be very expensive to replace. To reduce increased fault current levels, three general solutions exist [2], [3]:

- existing bus can be broken and served by two or more smaller transformers,
- use of a single, large, high-impedance transformer, resulting in degraded voltage regulation for all the customers on the bus,
- use inductive current-limiting reactors to reduce fault current level seen by older portions of the system.

These options assume the tradeoff between fault control, bus capacity, and system stiffness [2]. The first two options require considerable investments. Reference [3] offers an expanded list of conventional solutions for reduction of fault currents, giving advantages and disadvantages for using the fault current limiting reactors. These devices will suppress fault currents by generating the limiting impedance. Insertion of the limiting impedance happens faster than a conventional circuit breaker will clear the fault. However, current limiting reactors have a voltage drop under normal conditions. Also, the interaction with other system components can cause transient overvoltages or other problems in some cases [3].

Superconducting fault current limiters (SFCLs), unlike reactors or high-impedance transformers, will limit fault currents without adding impedance to the circuit during normal operation. From [4], utilities will achieve financial benefits with installing SFCLs versus investments for multiple upgrades of circuit breakers, fuses, and busworks. Other benefits from installing SFCLs are safety, reliability, and power quality. The same reference, [4], gives comparison between fault currents without and with SFCL: fault currents through transformers can reach up to 10-20 times the steady state design current. SFCL can reduce these fault currents down to levels not exceeding 3-5 times the steady state current. Thus, damage to expensive grid-connected equipment is prevented by SFCLs.

A good overview of the state-of-the-art of fault current limiting devices is given in [5]. This reference also identifies the most suitable types of fault current limiters (FCLs) for specific types of locations in smart grids.

Reference [6] shows an ATP model for the resistive SFCL consisting of one superconducting element and studies the effects of such parameters as length of superconductor, critical current, and cross section of superconductor on the peak values of limited fault currents. Reference [7] uses the model from [6] to apply to a small distribution system and studies voltage sag and transient recovery voltage (TRV).

In this paper, the resistive type SFCL is modeled for a distribution network of 15 kV in Alternative Transient Program (ATP).

The modeling of the SFCL with a number of elements in

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parallel (four in this work) for each phase considers the effects due to transition between elements during successive fault-reclose sequences.

II. Materials for Resistive SFCLs

The resistive SFCL is simpler and more compact in design than other types [8]. They are also more cost-effective than inductive limiters. Reference [9] mentions the following types of HTS superconducting materials used for resistive SFCLs: BSCCO coils, MgB_2 wires, YBCO bulks, thin films and YBCO coated conductors.

A cheaper alternative to the superconducting materials mentioned above was recently developed [10], [11]. These superconducting elements feature superconductor/metal matrix composites (SMMC™) that consist of Type II superconducting particles embedded in a Type I proximity effect superconducting material [11]. A Type II superconductor is represented with granular superconducting ceramic particles, and a Type I superconductor is a ductile metal matrix.

Grid-Logic, Inc. uses MgB_2 powder embedded in a variety of metals. Preference is given to gallium (Ga) matrix where Ga forms about 30% of the total volume. Such a composition and percentage overcome shortcomings of both HTS and MgB_2 materials [11]. The manufacturing of such superconductive element per phase is much cheaper compared to other technologies [11].

Table 1 summarizes materials for resistive SFCLs described in this section, where T_c is the critical temperature.

TABLE I
Materials Used For Resistive SFCLs

Material		Superconductor type/generation	T_C, K	Way of use
BSCCO	$BI_2Sr_2Ca_2Cu_3O_{10}$ (referred to as BSCCO) [17], also referred to as Bi-2223	Type II / 1G	110 [17]	coils [9]
	$BI_2Sr_2Ca_1Cu_2O_8$ (referred to as Bi-2212) [17]	Type II / 1G	110 [17]	
YBCO	$YBa_2Cu_3O_7$ [17]	Type II / 2G	93 [17]	bulks, thin films, coated conductors [9]
MgB_2	MgB_2 [10]	Type II / 2G	40 [10]	wires [9], [10]
SMMC™	MgB_2/Ga [11]	Type II superconducting particles embedded in a Type I proximity effect superconducting material	40 [11]	coils [11]

III. Overall SFCL Concept

From [11], the SFCL system consists of two main components: turret system and cryogenics. The number of superconducting elements (later referred to as elements) in parallel per phase is dependent on the design, where only one element per phase is on-line at a time (see Figs. 1 and 2).

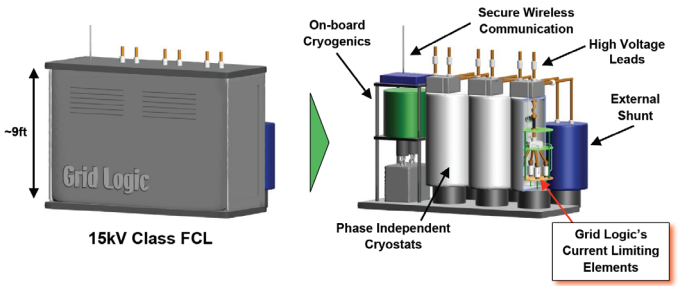

Fig. 1. Fault Current Limiter Concept, with permission from [11].

The turret system consists of the following components: four elements, HTS leads in series with the turret, thermal transducer (elements are switched into the line via a thermal transducer), switching control module (to determine an active element). The cryogenics system cools the elements to a temperature below the critical utilizing liquid neon (Ne). The current limiting shunt is located outside of cryogen. The HTS leads thermally isolate the elements from the high current copper leads.

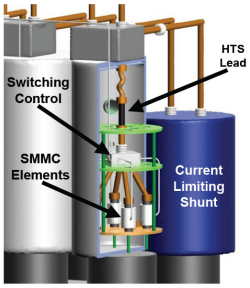

Fig. 2. One phase of the SFCL device with 4 elements per phase, with permission from [12].

During normal operation, all the current flows through one of the elements whose resistance is about zero. When the fault current exceeds the critical current (I_c), the element rapidly acquires its metallic state and eventually its resistance is much higher than resistance/impedance of the shunt. This redirects the majority of the fault current to flow through the shunting branch, making the shunt dissipating the fault energy. Rapid insertion of this resistance/impedance reduces the magnitude of the fault current and thus prevents downstream circuit breakers from tripping. After the fault is cleared, current is again below its critical value and the resistance of the element returns to about zero value.

From [12], automatic reset happens as follows: when current magnitude falls below I_c, the in-line element begins to cool down under the normal load current. The cooling process activates the turret switch and a parallel element is brought on-line. The off-line element is cooled under no-load conditions.

In case of a persisting fault, the central switch control system will change the element remaining in the metallic state to one of the elements still remaining in a superconducting state at a time determined by the temperature of the element and the utility. The elements intrinsically respond to faults within first ¼ cycle.

IV. Modeling in ATP

The superconducting materials respond to changes in critical temperature, critical current and critical magnetic field. There are several ways to model elements of a resistive SFCL:

- ***R (t)* with transition time of about 1 ms,**
- ***R (I, T)*, *R (I)* based on the V-I characteristic,**
- ***ρ (J, T)*, *ρ (J)* based on the E-J characteristic,**

where:

R is resistance,
t is time,
I is current,
T is temperature,
ρ is resistivity,
J is current density, and
E is electric field intensity.

However, it is typical to use a characteristic that is a function of current only and do not directly model a thermal characteristic [6], [13], [14].

For this work, ATP modeling, performed in time-domain, will show behavior of the elements during transition from the superconducting state to the resistive state of each element and from one element to the other.

For resistive type SFCLs, the inductance of a winding in normal condition is very small and usually neglected in modeling [15]. The inherently small inductance of the superconducting elements was not included in the model. The changes from the superconducting state to the normal metallic state are controlled as a function of the circuit current only.

The ATP software allows users to control elements with the general technical description language called MODELS [16]. The nonlinear resistances representing the superconducting elements are controlled by a MODELS block containing a code where the input signal is a circuit current and the output signal is a time-varying resistance.

The first goal was to model the complicated resistance development, where the R-I curve of each element during quench conditions is based on its V-I characteristic as shown in Fig. 3. In this figure and later in the text, n is resistive transition index.

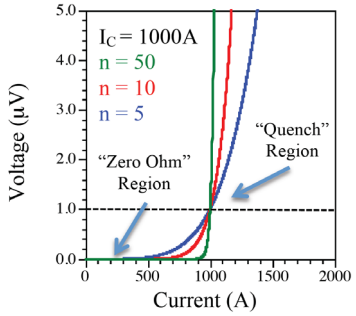

Fig. 3. V-I characteristic of a 1 cm long superconducting component, with permission from [12].

The critical current (I_c) flowing through the superconducting component creates an electric field of 1 μV/cm in the material (this is typical for all HTS materials [17]). As the current exceeds I_c, the electric field within the material (i.e., the resistance) continues to increase. This is described by (1):

$$V = V_c \left(\frac{I}{I_c}\right)^n \tag{1}$$

where:

V_c = (1 μV/cm)·component length, here V_c = 0.06 V.

The higher the value of n, the faster the voltage increases with the current for values greater than I_c.

The resistance development of each element is modeled as three time intervals:

1. R_1 is a nonlinear steep rise after reaching the critical current value I_c (depends on the transition index n), described as a derivative of (1) with respect to circuit current I, leading to (2):

$$R_1 = \frac{dV}{dI} = \frac{nV_c I^{n-1}}{I_c^n} \tag{2}$$

2. R_2 is a slow linear exponential decay after reaching maximum value of no more than 30 Ohms, in the code described with (3):

$$R_2 = R_{\max} e^{-t_c/\tau} \tag{3}$$

where:

R_{max} is maximum value of resistance reached at the moment t_c, no more than 30 Ohms,
t_c is start of interval 2, and
τ is time constant of the exponential decay.

3. R_3 is a linear decrease down to the superconducting state with some slope, i.e., the equation of the straight line with the negative slope, in the code described with (4):

$$R_3 = R_{crit} - \frac{R_{crit}}{slope}(t_c - t_{crit}) \tag{4}$$

where:

R_{crit} is critical value of resistance at which the full power cooling is applied, and
t_{crit} is start of interval 3.

In real situations, the cooling can take up to several minutes, which is too long to perform simulations for many experiments with the time step of 0.1 μs. Thus, the value of the slope chosen for the simulations was 9 s for each element, which corresponded to about 9.1 s for each element to both acquire the resistive state and recover to the superconducting state. However, the system is parameterized and can be tailored to meet the actual specifications of the device provided by the manufacturer. The last interval corresponds to the application of the full power heat removal. AC losses of the SFCL were not studied. Three time intervals of the resistance development are indicated in Fig. 4 for element 4. Fig. 5 shows closely the resistance development of element 1 for interval 1 and partly for interval 2.

The second goal was to model switching between four elements which was implemented with the combinations of if-else statements. Fig. 4 demonstrates resistive behavior of four elements for a permanent fault. 0.5 s after the first element was brought off-line, switching was performed onto the second element. The time intervals between engaging each element

correspond to the reclosing intervals in distribution systems. Typically, three consecutive reclosing operations are programmed with increased time interval: 0.5 s after the first trip, 2 s after the second trip, and 5 s after the third trip [18]. These time intervals can be seen in Fig. 4.

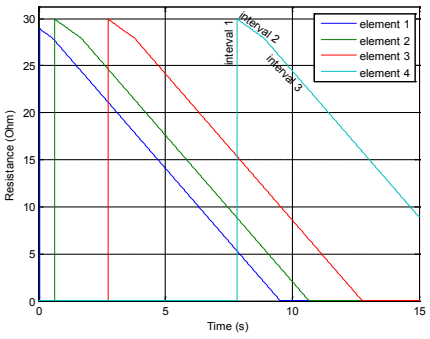

Fig. 4. Nonlinear resistive behavior of phase-A elements for a permanent fault, n = 10.

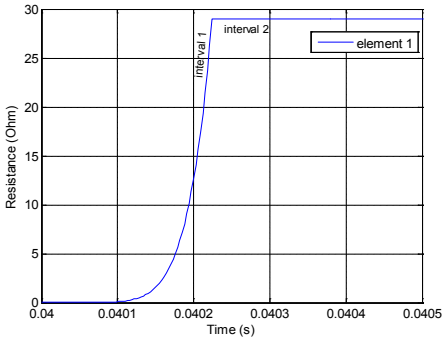

Fig. 5. Time evolution of nonlinear resistance for the first element, n = 10.

If, after the third reclosing, the fault current still persists, then the SFCL will run out of the healthy elements and the recloser will lock out.

The total interrupting time of the recloser (relay plus circuit breaker interrupting time) for "fast trips" was chosen as 6 cycles or 0.1 s. This is consistent with common practice as discussed in [19].

The ATP model of the SFCL device and the simple 15 kV distribution system for three-phase-to-ground fault are shown in Figure 6. The system shown has the source impedance providing X/R ratio of 2 (typical for distribution systems) and a load of power factor 0.9 lagging. In order to avoid numerical oscillations, the load inductor and resistance had to be separated from the 3-phase system and the source impedance was paralleled with a high-value damping resistance.

The capacitances shown in Fig. 6 are implemented to study transients in the system. They are lumped in three elements per phase and estimated based on [20]: 150 pF per four switches in each phase in the SFCL; the SFCL without switches was approximated to have an effective capacitance, corresponding to that of an outdoor current-limiting reactor – 250 pF per phase. The resistances associated with these capacitances are used for damping of numerical oscillations. The estimation of transients was associated with the operation of the switches in the SFCL device.

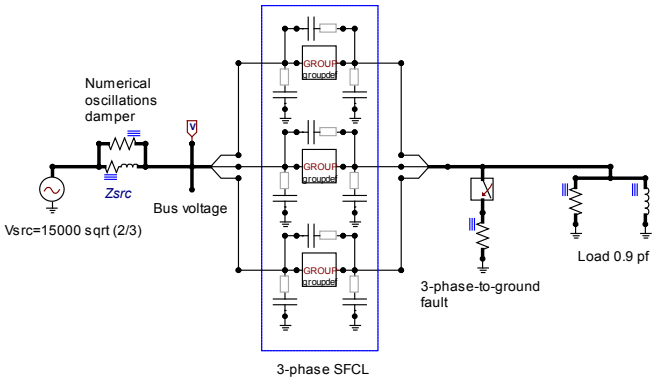

Fig. 6. Distribution system with the 3-phase SFCL.

Each box in Fig. 6 contains four resistive elements in parallel representing the superconducting elements and one resistive element representing the shunt of 0.5 Ohms, as per Grid-Logic, Inc. requirements. Such a configuration can operate for three consecutive reclosing operations before locking out. The simplified diagram for controlling the four parallel elements of each phase is shown in Fig. 7.

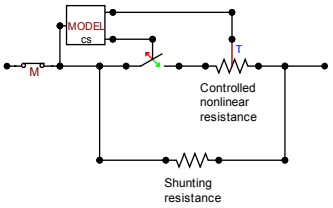

Fig. 7. Simplified control of nonlinear resistance. Four elements are connected in parallel in the implemented model.

In the simulation model, the recloser functions actually are carried out by the switches within the SFCL (see Fig. 7). Integrating the circuit breaker and current limiting functions within one device means that the switches need to possess adequate interrupting and TRV capability. Simulations were limited to successive fast trips to demonstrate the current limiting capabilities and multi-shot reclosing of up to 3 times.

The modeled SFCL can perform any sequence of switching in/out operations starting from any element for any single or repeated fault with the time intervals between engaging each the following element as discussed above.

V. Case Studies

Any kind of fault can be simulated with the three-phase SFCL model developed. However, due to the space limitation, results are given here for the three-phase faults only.

The simulations were carried out with the time step of 1 μs and 3 μs for long-time simulations and 0.1 μs for short-time simulations to allow for prospective high frequencies of TRV during switching to be captured on the plots.

The faults were initiated at 0.04 s. The rated system load current is 700 A, and the critical current is 800 A.

Introducing the SFCL into the system, as shown in Fig. 6, reduced the first peak of the three-phase fault current by about 50% on average, and to be more precise: phase-A reduction by 53.8%, phase-B reduction by 42%, and phase-C reduction by

57.6%. The phase-C fault current first peak is the highest, thus plots will be shown for phase C. Fig. 8 demonstrates the prospective fault current and reduced fault current for phase C.

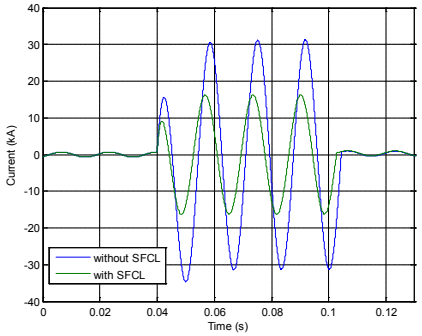

Fig. 8. Phase-C prospective and reduced fault currents.

Fig. 9 shows the TRV that would appear across the circuit breaker (not shown in Fig. 6) if no SFCL was applied.

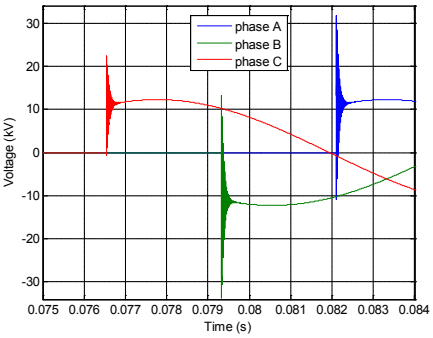

Fig. 9. Voltage across the circuit breaker without SFCL in the system.

The SFCL model presented here did not introduce TRV in the system, and the explanation with the reference to the corresponding figures follows later in the text.

A. Temporary Fault

Fig. 10 shows the currents through two elements for a temporary fault which is self-cleared at 0.18 s, i.e., before the next of four elements will be brought on-line, thus this element will stay in its superconducting state. That means that the rated current will flow through the second element, which is shown in Fig. 10. The first peak from Fig. 10 is enlarged in Fig. 11.

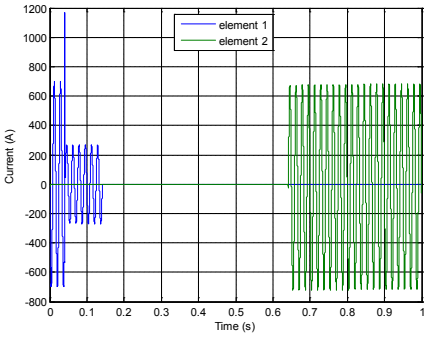

Fig. 10. Phase-C currents through two elements, $n = 10$.

After the final resistive state was achieved, the value of the current through the element is 277 A, the rest of the fault current flows through the shunting resistance of 0.5 Ohms (about 16 kA). Each element is exposed to the fault current for 6 cycles as discussed above.

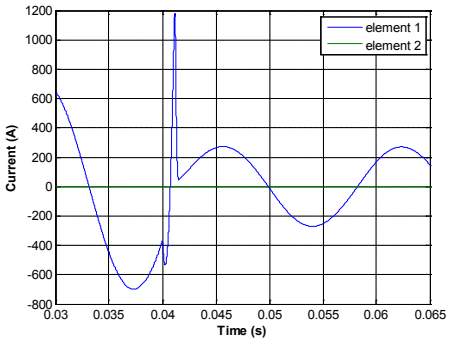

Fig. 11. Enlarged first peak of the current from Fig. 10, $n = 10$.

Fig. 12 shows the bus voltage for the same temporary fault. Due to the fact that the bus voltage does not have discontinuities at the recovery moment and the recovery is achieved without opening the switch (fault is self-cleared), there is no TRV upon the system recovery compared to Fig. 9. The bus voltage dropped by 33.5%. Fig. 13 and 14 show enlarged portions of Fig. 12 for initiation of the fault and recovery of the system, respectively. Fig. 13 shows that as the fault starts, voltages of all the phases dropped to zero, and Fig. 14 shows clean bus voltage recovery.

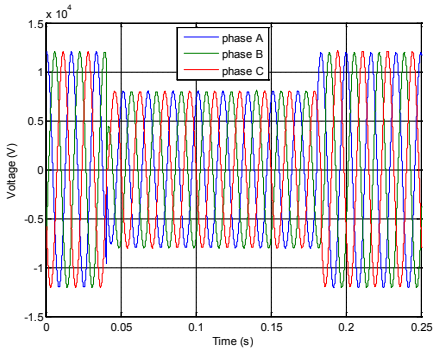

Fig. 12. Bus voltages during normal operation and three-phase fault.

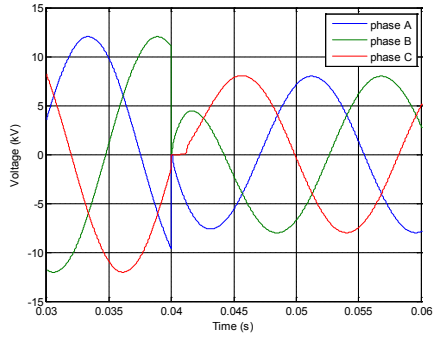

Fig. 13. Enlarged portion of Fig. 12 for the fault initiation.

B. Permanent Fault

For a permanent fault in Fig. 15, four elements of phase C are shown engaged with the time intervals as discussed above. Fig. 16 demonstrates enlarged portion from Fig. 15 for currents for the first two elements. The corresponding plots of the bus voltage and voltages across each switch which opens related element did not show TRV for any kind of fault due to

the fact that the shunting resistance always provides an alternate path for the flow of current (see Fig. 7).

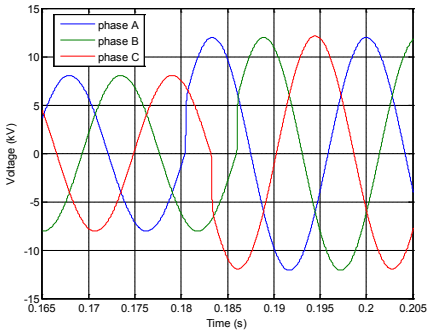

Fig. 14. Enlarged portion of Fig. 12 for the system recovery.

Fig. 17 shows voltage across the switch of the second element. Zero voltage corresponds to the period when the switch is closed and second element is on-line. Before and after, the switch is open and the voltage shown is the voltage reduced due to the fault.

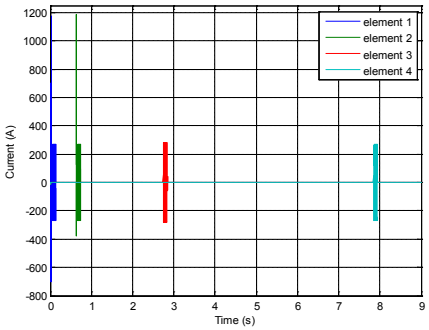

Fig. 15. Phase-C currents through all four elements for a permanent fault, $n = 10$.

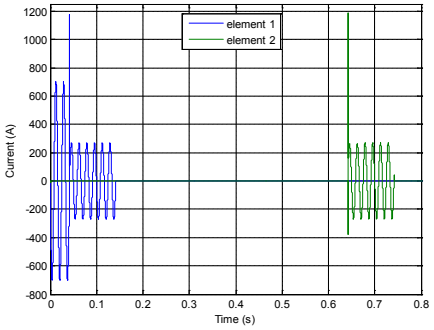

Fig. 16. Enlarged portion of Fig. 15 for currents through the first two elements.

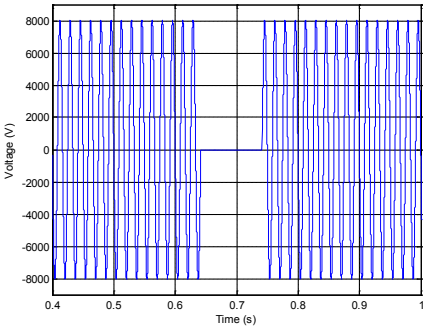

Fig. 17. Voltage across the switch of the second element.

C. Transition Index

We are interested in short time transition from zero resistance to the normal metallic state because it speeds up the limiting resistance development. The transition index n is responsible for this speed. Fig. 18 shows comparison of currents through the same superconducting element (first one to encounter the fault) for $n = 5$, 10, 50. The largest peak corresponds to $n = 5$. Due to the slow development of the resistance, the peak has time to reach a high magnitude. The lowest peak corresponds to $n = 50$, where the limiting resistance develops much faster. Fig. 19 gives a more detailed picture of these peaks for different n: the peak through the first element was 802 A ($n = 50$), 1164 A ($n = 10$), 2755 A ($n = 5$).

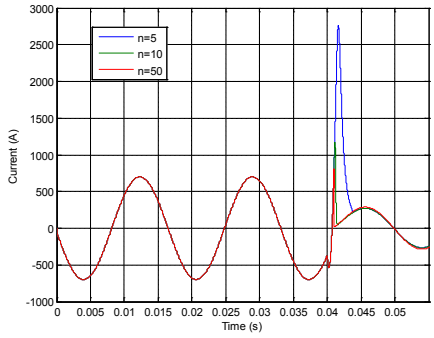

Fig. 18. Phase-C first peak fault current limitation through the first element for $n = 5$, 10, 50.

The transition index does not affect the voltage and current levels, except for the first peak of the current passing through the superconducting element at the very beginning of the fault, and thus affecting the first peak magnitude of the fault current in the system. Development of the limiting resistance depending on the transition index is demonstrated in Fig. 20. The fastest is for $n = 50$, the slowest is for $n = 5$.

The final value of the resistance of 30 Ohms is reached in the case of $n = 5$ and $n = 10$. For $n = 50$ the final value of the resistance is 28 Ohms, however for $n = 50$ this level is achieved faster, affecting the first peak magnitude from Fig. 19. As can be seen in Fig. 19, the time difference of almost 0.5 ms affects the first peak of the current passing through the superconducting element dramatically.

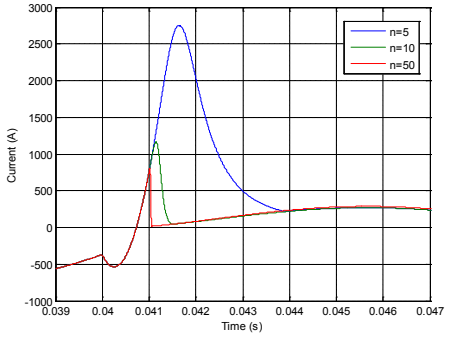

Fig. 19. Enlarged portion of the first peaks from Fig. 18.

However, very high values of n leading to fast transition to normal state can cause dangerous overvoltages. Reference [21]

suggests transition time interval of 2-4 ms.

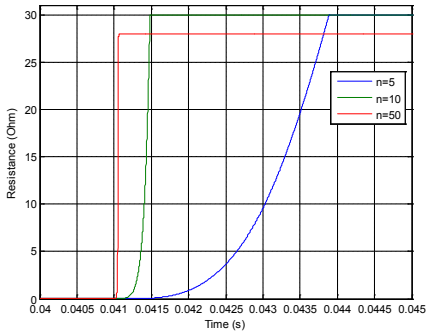

Fig. 20. Development of nonlinear resistance for n = 5, 10, 50.

VI. Conclusions

This paper presents modeling of a resistive SFCL with four parallel superconducting elements and a shunt resistance of 0.5 Ohms. The simulation results showed:

- on average between three phases, the first peak of the three-phase fault current was reduced by 50% compared to the prospective fault current, and to be more precise: phase-A reduction by 53.8%, phase-B reduction by 42%, and phase-C reduction by 57.6%.
- operation of the switches inside the SFCL does not introduce TRV.
- during the three-phase fault, the voltage sag on the bus was 33.5% compared to 100% without the SFCL, which completely eliminates the power outage for the system studied.
- the simulation results proved that the higher transition index, the lower the first peak of the current passing through the superconducting element is, thus affecting the first peak of the system fault current. For the same three-phase fault, the peak through the first element was 802 A (n = 50), 1164 A (n = 10), 2755 A (n = 5).

VII. Future Work

The recommendations for future work include:

- In an actual implementation, an upstream recloser would perform the tripping and reclosing, the SFCL would be placed downstream, and the switches within the SFCL which sequence through the four elements would only operate when deenergized, i.e., after the recloser trips but before it recloses. The switches within the SFCL could then be rated similar to those within a sectionalizer. With such a combination of the recloser and SFCL, TRV across the recloser contacts can be studied.
- Additional can be done for cases of delayed trips (3rd and 4th trips), reconciling the thermal performance of the SFCL with the electrical circuit equivalent.

VIII. References

[1] G. Kaur, M. Y. Vaziri, "Effects of distributed generation (DG) interconnections on protection of distribution feeders," in *Proc. 2006 IEEE Power and Energy Society General Meeting*, pp. 1-8.

[2] An in-house tutorial of American Superconductor Corporation, Brockenborough, 1996. [Online]. Available: http://www.wtec.org/loyola/scpa/04_03.htm

[3] L. Kovalsky, Xing Yuan, K. Tekletsadik, A. Keri, J. Bock, and F. Breuer, "Applications of superconducting fault current limiters in electric power transmission systems," *IEEE Trans. Appl. Supercond.*, vol. 15, no. 2, pp. 2130-2133, Jun. 2005.

[4] Superconductivity News Update, Bob Lawrence & Associates, Inc., Alexandria, VA, Oct. 2007. [Online]. Available: http://www.superconductivitynewsupdate.com/newsletters/FaultCurrentLimitersOct2007web.htm

[5] Y. Zhang and R. A. Dougal, "State of the art of fault current limiters and their applications in smart grid," in *Proc. 2012 IEEE Power and Energy Society General Meeting,* pp. 1-6.

[6] Ye Lin and K.-P. Juengst, "Modeling and simulation of high temperature resistive superconducting fault current limiters," *IEEE Trans. Appl. Supercond.*, vol. 14, no. 2, pp. 839-842, Jun. 2004.

[7] Ye Lin, M. Majoros, T. Coombs, and A. M. Campbell, "System studies of the superconducting fault current limiter in electrical distribution grid," *IEEE Trans. Appl. Supercond.,* vol. 17, no. 2, pp. 2339-2342, Jun. 2007.

[8] W. Hassenzahl and M. Young, "Superconducting fault current limiters," Technology Watch 2009, Dec. 2009. [Online]. Available: http://www.smartgridnews.com/artman/uploads/1/000000000001017793.pdf

[9] Z. Hong, J. Sheng, J. Zhang, B. Lin, L. Ying, Y. Li, and Z. Jin, "The development and performance test of a 10 kV resistive type superconducting fault current limiter," *IEEE Trans. Appl. Supercond.*, vol. 22, no. 3, pp. 560-504, Jun. 2012.

[10] M. J. Holcomb, "Supercurrents in magnesium diboride/metal composite wire," *Physica C – Superconductivity and its Applications*, vol. 423, issues 3–4, pp. 103-118, Jul. 2005.

[11] Appendices to Grid Logic's Request for Support for Electric Utility Energy Efficiency Equipment Manufacturing Operations, March 2010.

[12] M. Holcomb, G. Caravias, "FCL technology overview," Grid-Logic, Inc., Metamora, MI, Mar. 2010.

[13] Z. Pei and J. He, "Effects of Superconducting Fault Current Limiter on Power Distribution Systems," in *Proc.* 2009 *APPEEC Asia-Pacific Power and Energy Engineering Conf.*, pp. 1-5.

[14] V. S. Mehairjan, M. Popov, A. Geschiere, and W.L. Kling, "Transient analysis of a 150 kV fault current limiting high temperature superconducting cable," in *Proc. 2011 IPST Power Systems Transients Conf.*, pp. 1-6.

[15] B. C. Sung, D. K. Park, J.-W. Park, and T. K. Ko, "Study on a Series Resistive SFCL to Improve Power System Transient Stability: Modeling, Simulation, and Experimental Verification," *IEEE Trans. Industrial Electronics*, vol. 56, no. 7, pp. 2412-2419, Jul. 2009.

[16] L. Dube, "Users Guide to MODELS in ATP," Apr. 1996.

[17] W. Hassenzahl and M. Young, "Superconducting power equipment," Technology Watch 2011, Dec. 2011. [Online]. Available: http://www.iass-potsdam.de/sites/default/files/files/epri_sc_technology_watch_2011.pdf

[18] J. D. Glover, M. S. Sarma, and T. J. Overbye, *Power System Analysis and Design*, 4th ed., Thomson Learning, 2008, p. 512.

[19] P. R. Heavey, "A tutorial for distribution protective relay applications," *58th Annual Conference for Protective Relay Engineers*, pp. 169-188, Apr. 2005.

[20] IEEE Guide for the Application of Transient Recovery Voltage for AC High-Voltage Circuit Breakers, IEEE Std C37.011-2011, Nov. 2011.

[21] R. Sharifi, H. Heydari, "Analytical hierarchy process based optimization of resistive superconducting fault current limiters," in *Proc. 2010 Power Quality Conf.*, pp.1-7.