Interaction of Capacitor Bank Inrush Current Limiting Reactor and Medium Voltage Vacuum Circuit Breakers

Gopal Gajjar, A. M. Kulkarni, and S. A. Soman

***Abstract*—This paper presents an investigation of a flashover incident in 33 kV GIS switchgear used for back-to-back capacitor bank switching duty. The contribution of this paper is to highlight a rare case of real-life non sustained disruptive discharge (NSDD) and its effects. In one failure incident, the capacitor cells in one of the capacitor bank got damaged. Subsequently a flashover occurred in the GIS panel for the vacuum breaker used for switching the other bank. The possibility of occurrence of NSDD in a laboratory environment is now widely recognized. However, NSDD is generally considered benign, and very little is known about its harmful effects, if any, in real operating conditions. We show that the failure event discussed here is caused due to voltage escalations due to NSDD and subsequent restrikes in the vacuum circuit breaker. The role of the capacitor bank inrush current limiting reactor in causing the failure is analysed. EMTP-ATP simulations and analytic study are presented to support the conclusion.**

***Keywords*—NSDD, restrike, vacuum circuit breakers, back-to-back, capacitor bank.**

I. Introduction

THIS paper presents a study of failure of a medium voltage Vacuum Circuit Breaker (VCB) employed for back-to-back shunt capacitor bank switching duty. The failure incident occurred in an unusual situation: The failed circuit breaker was in open position for 24 hours before failure.

The following sections present the system configuration, details of incidents, and a discussions regarding Non Sustained Disruptive Discharge (NSDD). The role played in the failure by characteristics of VCB, NSDD, the cable connecting between VCB and capacitor bank and the current limiting reactor is discussed in detail. Analytical arguments and simulation results are presented in support of the conclusion.

A. System Details

The system pertains to a 33 kV urban distribution system. The station is a major receiving point getting supply at 220 kV. It is stepped down at 33 kV by a 100 MVA transformer. The 33 kV switchgear is SF_6 with vacuum circuit breakers. Several underground feeders distributes power further, there are over ten such outgoing feeders with average length of about 5 km. The 33 kV bus has two switched capacitor banks of 8 MVAR and 12.5 MVAR connected through VCBs. A 30 kV rated voltage surge arrester is connected to 33 kV main transformer. Both the capacitor banks are in ungrounded double star connection. To limit the capacitor bank switching inrush current, both capacitor banks are provided with current limiting series reactors which limit the inrush current frequency to about 500 Hz. Fig. 1 shows the relevant circuit.

Authors are with the Department of Electrical Engineering, Indian Institute of Technology Bombay, Mumbai, India e-mail: gopalgajjar@ieee.org

Paper submitted to the International Conference on Power Systems Transients (IPST2013) in Vancouver, Canada July 18-20, 2013.

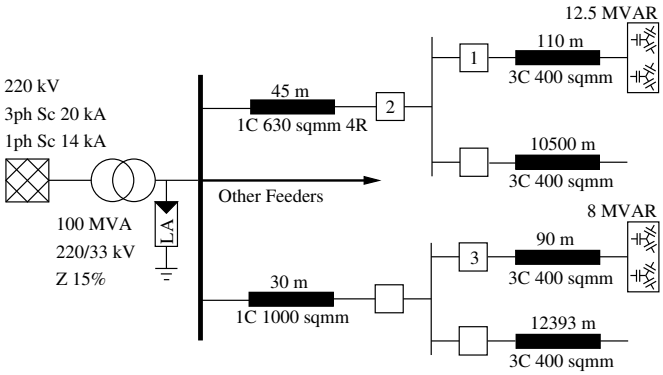


Fig. 1: Single Line Diagram of the System.

B. Event Details

The system was in service for three years without any history of faults. On the day of the event, VCB-1 connected to the 12.5 MVAR capacitor bank was in open position for the previous 24 hours. The 8 MVAR capacitor bank experienced a fault in the capacitor cells and it was successfully isolated from the system through operation of VCB-3. After a few

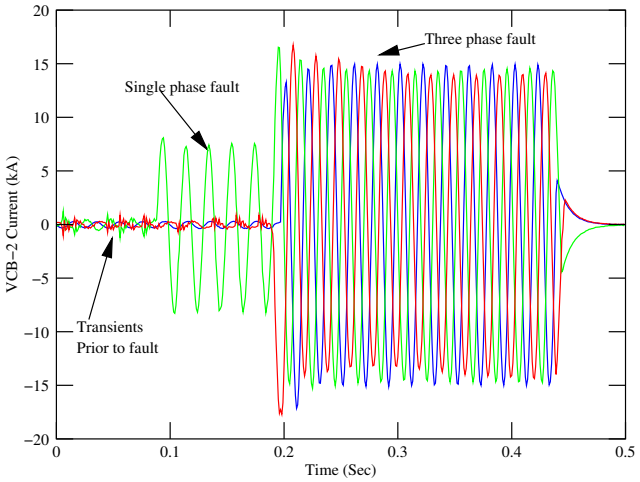


Fig. 2: DR of fault current through VCB-2.

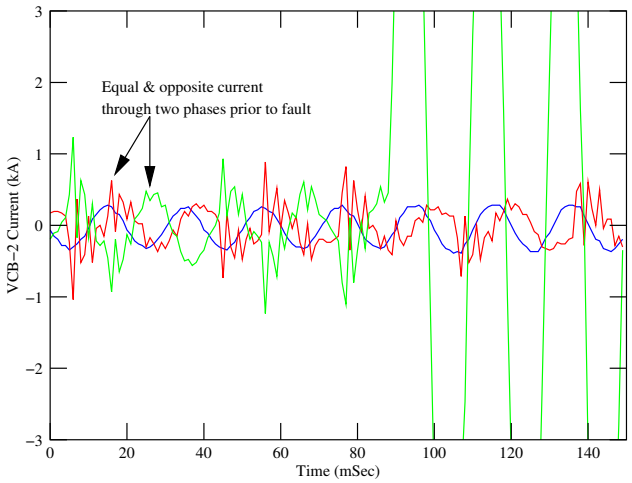


Fig. 3: Zoomed view of transients prior to fault.

seconds a three phase fault was detected and was cleared by operation of VCB-2. A visual inspection revealed a flashover in the panel of VCB-1.

The disturbance record (DR) of current through VCB-2 is shown in Fig. 2. Here it can be seen that it was a evolving fault with some initial disturbance progressing to single phase to ground fault and ultimately resulting in a three phase fault. The zoomed view in Fig. 3 shows the incipient fault where the peak value of fault current is below 1 kA and the current in two phases is equal in magnitude and opposite in phase. The waveforms look like damped sinusoids and have a frequency just below 500 Hz as observed with the 1 kHz sampling frequency of DR.

C. Analysis

The system was modeled and simulated in EMTP-ATP and it was found that the situation captured by the DR can be simulated only if the current takes a path through two poles of VCB-1 to the 12.5 MVAR capacitor bank, without involving any shunt path. If the current is intermittent, then it is possible to have damped sinusoidal waveform with recurrent nature. The calculated natural frequency of oscillation of inrush currents 12.5 MVAR bank is 460 Hz (calculated in the next section.) which matches closely with that observed in the DR.

Such inrush current is possible if there are multiple restrikes in the poles of VCB-1. The inrush currents in two phases of 12.5 MVAR capacitor bank can also cause similar currents in the parallel 8 MVAR capacitor bank due to outrush effect. The capacitors cells are not rated for carrying such high amplitude high frequency currents for long and they failed. Moreover, multiple restrikes cause voltage escalation near VCB-1 and it result into the fault progressing to single phase to ground fault and then to three phase fault. The equivalent circuit involved in this case is shown in Fig. 4.

Factory inspection of the failed circuit breaker revealed complete failure of the vacuum interrupter of the two poles. Arcing marks were observed between the two open contacts of the interrupter. The melting of metallic shields revealed that interrupter was subjected to heavy current arcing for long time. This observation confirmed that the path of the current prior

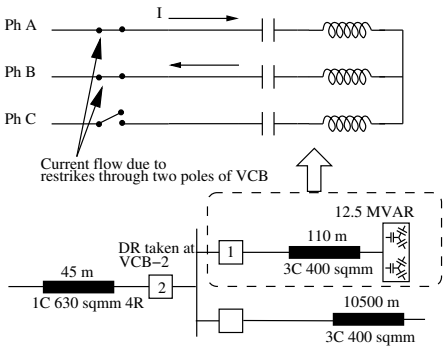


Fig. 4: Equivalent Circuit causing distorted current in DR prior to the single phase fault current.

to the single phase to ground fault was through the two poles of open vacuum interrupters.

Having established the probable cause of the flashover and the other incident as the multiple restrikes through the two poles of VCB-1, the next sections investigates further the possibility of such restrikes. The possible causes under investigation are discussed through analysis and simulation, see Fig. 5. It is pertinent to remember that VCB-1 was in open position, and we aim to establish that restrikes are still possible in this state. We show that the VCB condition and the circuit configuration, especially the current limiting reactor, play important role in this.

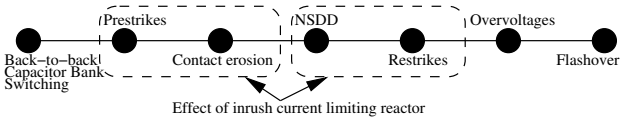


Fig. 5: Possible stages leading to failure.

II. Capacitor Bank Switching Duty

The issues associated with back-to-back capacitor bank switching are well documented in [1], [2]. The high frequency inrush currents associated with back-to-back switching can stress circuit breakers. When switching off a capacitor bank there is a possibility of restrike. The circuit breakers have a defined rated back-to-back capacitor bank inrush making current and capacitor bank switching class C2 for ensuring very low probability of restrike during capacitive current breaking.

VCB-1 is rated for back-to-back operation and can withstand up to a peak current of 20 kA and frequency of 4250 Hz, giving tolerable rate of rise of inrush current (di/dt) as 85 A/μs. To ensure meeting the operation limitations in actual service, the 8 MVAR and 12.5 MVAR capacitor banks are equipped with a series current limiting reactor at neutral side of the bank as shown in Fig. 4. The reactor is rated at 1 %. Thus, at rated current through the capacitor bank the voltage drop across the reactors is 1 % of the rated voltage. In ungrounded capacitor bank the highest inrush current occurs when at switching instant peak line to line voltage appear between two phases. The worst case peak current and inrush frequency is given by,

$$I_p = \sqrt{2} V_{LL} \sqrt{\frac{C_{eq}}{L_{eq}}} \qquad f = \frac{1}{2\pi \sqrt{L_{eq} C_{eq}}} \qquad (1)$$

Where,

$$L_{eq} = 2\left(L_1 + L_2\right) \qquad C_{eq} = \frac{1}{2}\frac{C_1 C_2}{C_1 + C_2}$$

It involves the equivalent circuit consisting of both the capacitor bank. C_1 and L_1 are the per phase capacitance and the current limiting reactance of 8 MVAR capacitor bank, C_2 and L_2, the corresponding values for 12.5 MVAR capacitor bank. This calculates to peak current of 958 A and frequency of 460 Hz, resulting in di/dt of 0.44 A/μs, well within VCB capability.

A. *Effect of Cables and Inrush Current Limiting Reactors*

Apart from the parallel capacitor bank, the parallel cables connected to the same bus also experience similar transients while switching on the capacitor bank. They also contribute to high frequency inrush currents. The frequency of inrush current contributed by cables depends on their length, while the magnitude of current depends on the number of cables connected in parallel [3].

The effect of cable inrush current is significantly reduced by application of the inrush current limiting reactor. However, this reactor is ineffective in controlling the magnitude and frequency of inrush current caused due to the cable connected between the VCB and capacitor bank. The cable length in this case is 110 m. The calculated cable surge impedance is about 32 Ω and propagation velocity is about 1.4x10^8 m/s. There is always some discrepancy between closing of circuit breaker poles. When the first pole of the circuit breaker closes, it results in a travelling wave over this cable which partially gets reflected at the first discontinuity of the capacitor and the reactor. The refracted wave then splits in to two parts that travel over the other two phases of the cables. Full reflection occur at the two open poles of the VCB and the waves travel back. This results in the first current zero at the VCB contact at about 1.6 μs. The frequency of this current resulting from the wave propagation in the cable between breaker and capacitor bank is about 300 kHz, and the worst case initial peak current is 800 A. This makes the initial di/dt as 1500 A/μs. After first reflections there are several other reflections from various discontinuities in the source side too and the frequency of the current through the breaker contacts may actually be higher than mentioned above. The frequency of oscillations depends on the length of the cable. For shorter length the frequency is high. But with shorter cable length the duration of high frequency oscillations is lower as shorter cable gets charged faster and attains steady state faster.

As we mentioned earlier, this high frequency inrush current cannot be reduced by having series reactors. Rather the presence of reactor extends the period for which this high frequency currents are sustained. This is because without the reactor the cable section quickly attains the voltage of supply side and the multiple reflections damps down fast. However, in presence of the reactors the cable sections beyond the reactors take time to charge thus prolong the period for which multiple reflections occurs.

These effects are shown in Figs. 6, 7. It can be noticed that longer cable and with reactor causes the high frequency inrush current sustained for longer periods. The multiple reflections causing variable frequencies can be observed in the zoomed view Fig. 6b and the beats seen in all waveforms at 100 μs intervals. The total duration of this high frequency oscillations is of the order of few hundred microseconds. It may be noted that the simulations to obtain the inrush current ignored the small inductance in the GIS panels as they are negligible compared to the current limiting reactor. All the cable sections shown in Fig. 1 were modeled.

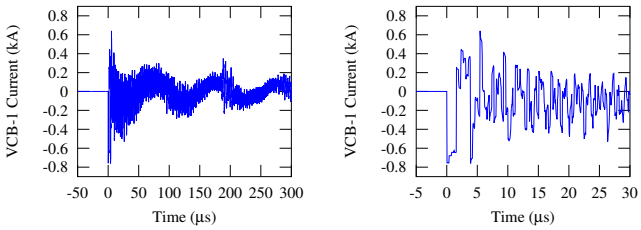


Fig. 6: The Cable Inrush Current: Cable length 110 m.

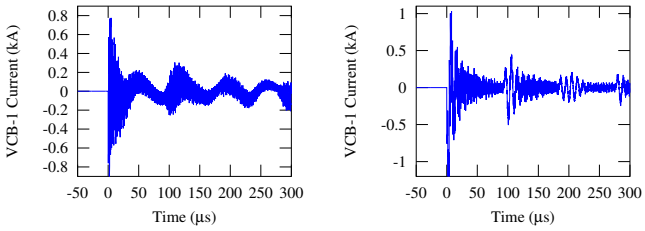


Fig. 7: The Cable Inrush Current: Cable length 55 m and Without Reactor.

B. *Prestrikes*

All circuit breakers experience prestrikes and for uncontrolled three phase operation it is highly probable that the pole having highest voltage across its contacts while closing will result in prestrike. So this high frequency current flows across the breaker while still the contacts are separated. The class C2 test duty for making capacitive current does not deal with such high frequency and high di/dt inrush current. The circuit breaker performance for daily operation for three years at this inrush current level is unknown. The effect of prestrikes on vacuum circuit breakers is discussed in [1], [4]. It is stated that high frequency current during prestrikes may result into micro-melting and welding of contacts. Breaking of these welding when contacts are opened at low current result in damage of contact surface and reduction in dielectric strength. VCB-1 has rated current of 1250 A and rated short circuit current is 25 kA, while the 12.5 MVAR capacitor bank present the load current of only 219 A. Hence, it may be said that the prolonged large magnitude high frequency current during prestrike due to presence of the series reactor lead to faster vacuum circuit breaker contact erosion and reduced dielectric strength. This could lead to more harmful consequences caused by NSDD.

III. Non Sustained Disruptive Discharge

NSDD is a phenomenon observed in vacuum circuit breakers. NSDD is defined as a disruptive discharge with current

interruptions that does not result in the resumption of power frequency current or, in the case of capacitive current interruption, does not result in current at the natural frequency of the circuit [1].

Usually NSDD is considered as harmless phenomenon, and it is frequently observed in the type test of vacuum breakers. It is known to be observed in the field operation too, but rarely reported, as it does not cause any damage to equipment and does not give any indications in the conventional measurement instruments. However, it is also reported in literature that, if the duration of current through NSDD is long enough to excite oscillations involving main capacitive element of the capacitor bank, it would result in restrike [5]–[7]. In this case, it is not counted as NSDD, as defined by [1], but an incident of restrike, although such restrikes are in fact caused by initial NSDD. Generally the oscillations following NSDD are associated with the parasitic capacitance and inductance local to, or of, the circuit breaker itself. NSDDs may also involve the stray capacitance to ground of nearby equipment.

A. Late NSDD

The circuit breaker standards [1], [2] prescribe maintaining the full voltage across the circuit breaker for 300 ms after opening of a capacitor bank. The capacitor bank retains charge during this period and hence the breaker contacts are stressed by as high as 2.5 pu voltage across the first pole to clear in case of ungrounded capacitor bank.

NSDD in the charged ungrounded capacitor bank can lead to voltage escalations across the healthy breaker contacts [8]. In worst case after first NSDD the voltage across healthy phase may go to 3.5 pu. This is due to the presence of the trapped charge in the capacitor bank, and the voltage doubling effect due to the traveling wave in the cable connecting the breaker and capacitor bank.

Observations are available of NSDD occurring in laboratory testings much after the 300 ms time period if the voltage stress is maintained [4], [5]. Such NSDD are called late NSDD. While very little actual data is available, it is not impossible for a breaker kept in open condition but stressed with full voltage for long period to experience NSDD. In case of very late NSDD the capacitor bank is in discharged state and hence the breaker is stressed with 1.0 pu voltage. Hence, even if NSDD occurs the worst case voltage escalation across the healthy phases would be 2.0 pu.

B. Effect of Series Reactor during NSDD

Ref. [8] discusses the effect of cables between VCB and capacitor bank through traveling waves, while [5]–[7] take lumped circuit view to take into consideration the effect of connection circuit. None, however, consider the case where current limiting reactor is present.

The major emphasis in discussion regarding NSDD is [6] that vacuum gaps have a very good capability of interrupting high frequency current and the current caused by NSDD is composed of several components at different frequencies. If this current is interrupted at a current zero caused by high frequency component prior to excitation of main capacitor

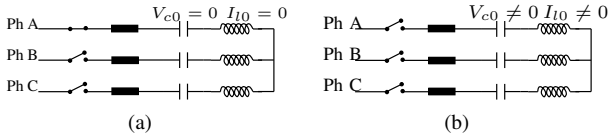


Fig. 8: Equivalent circuit during and after NSDD.

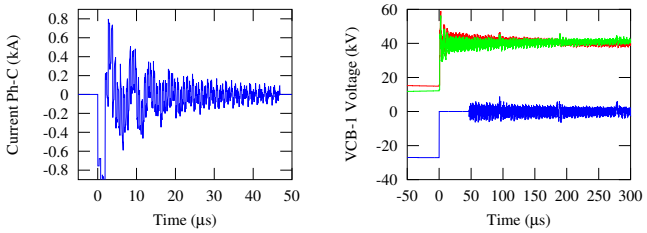
circuit, the voltages at healthy phases do not rise to dangerous level. Hence, the NSDD terminate with high frequency interruption and no further damage is caused. On the other hand, if this current persists for longer time, the voltage buildup across healthy phases is large enough to cause restrikes. The natural frequency of oscillation of main circuit i.e. involving the capacitor bank and the source side inductance is of the order of few kHz or lower. It would require a NSDD duration of about 1 ms to raise the voltage to 2 pu at 460 Hz. Usually such long duration NSDD is not possible. So from this point of view presence of the reactor helps in preventing any failures post NSDD.

But, detailed analysis of the situation reveal a different situation. Consider the circuit shown in Fig. 8a, the capacitor bank is in uncharged condition prior to a late NSDD. During NSDD the capacitor bank and the reactor gets charged. If NSDD is terminated fast the voltage rise in capacitor bank is not much, but the current developed in the reactor is significant. This is due to the fact that frequency of this current is governed by the cable capacitance and the reactor inductance. This frequency is in range of few tens of kilohertz, hence the reactor current would achieve its peak even if NSDD duration is about 20 to 50 μs.

The current through the circuit breaker contact gap is high frequency, but current through the reactor and the capacitor bank is much lower. So NSDD can get terminated at any of the high frequency current zero, while still a significant current is flowing through the reactor. After NSDD is terminated the cable, capacitor bank and reactor circuit is isolated from all power sources. But the voltage and current oscillations in this isolated circuit continues due to capacitor trapped charge and the reactor trapped current, see Fig. 8b. The frequency of this oscillation is again governed mostly by the cable capacitance and reactor inductance. This oscillation continues for a long time as there is very little damping in this circuit. The voltage attained by the cable ends connected to circuit breakers depends on the magnitude of reactor current at the instant the NSDD got terminated. In worst case the voltage could be 2 pu. So after few milliseconds after the NSDD is terminated the circuit breaker contacts get stressed by 3 pu. This could induce another breakdown in the vacuum contact gaps and may ultimately lead to restrikes.

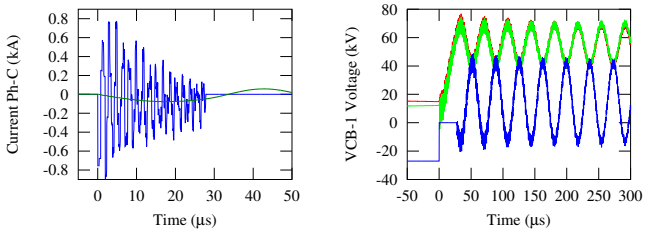
IV. Simulation Results

To show the validity of previous discussion, a simulation was performed on the circuit shown in Fig. 1. The VCB was modeled as slightly modified version of that presented in [9] to get controlled initiation of NSDD. The termination of NSDD is governed by the modeled properties of VCB i.e. the chopping current and high frequency current interruption capability. The cables were modeled at their high frequency



(a) (b)

Fig. 9: The NSDD current and post NSDD Voltage across VCB-1, without reactor.



(a) (b)

Fig. 10: The NSDD current and post NSDD Voltage across VCB-1, with reactor.

impedance Bergeron model [10], [11] considering the higher losses at frequency of 20 kHz. The dielectric losses in the cable insulation were also considered to obtain a realistic damping of high frequency oscillations.

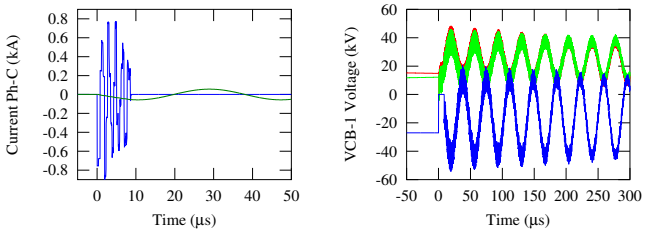
Fig. 9a shows the NSDD current in case without the current limiting reactor and Fig. 9b shows the voltage across the VCB-1 after the NSDD is terminated. Here it is seen that NSDD lasts for about 47 μs and the voltage across the healthy phases of VCB-1 is about 2 pu for short time and then damps to a very low value. Hence, it can be deduced that without the reactor, NSDD in a fully discharged capacitor bank poses no problem of restrikes.

The simulation where the reactor is considered is shown in Fig. 10. In Fig. 10a the NSDD current through VCB contacts is compared to the current through the reactor. The reactor current is very slow to rise and small magnitude compared to the NSDD current. Moreover, it can be observed that when NSDD is terminated at 28 μs the reactor current is nonzero. This trapped current causes the oscillations in isolated cable, capacitor bank and reactor circuit. As a result of these oscillations, the voltage across VCB-1 can seen to rise above 2.5 pu and it is sustained for a longer time than in case without reactor, Fig 10b. The frequency of these oscillations is around 27 kHz, governed by the value of reactor and the capacitance of the cable between VCB and the capacitor bank.

A. *Effect of VCB Contact Deterioration*

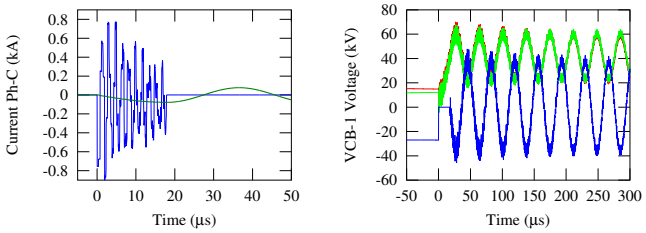
When the VCB contacts get deteriorated the chopping current and the high frequency current interruption capability reduces. Hence, the NSDD persists for longer time in deteriorated contacts. To see this effect two simulations were performed with different VCB contact conditions.

Fig. 11 show the NSDD current and post NSDD voltage with a healthy VCB having chopping current (I_{ch}) of 5 A



(a) (b)

Fig. 11: The NSDD current and post NSDD Voltage across VCB-1, $I_{ch} = 5\ A$, $di/dt = 400\ A/\mu s$.



(a) (b)

Fig. 12: The NSDD current and post NSDD Voltage across VCB-1, $I_{ch} = 2\ A$, $di/dt = 250\ A/\mu s$.

and high frequency current interrupting capability of (di/dt) of 400 A/μs. In this case the NSDD current lasts for about 10 μs and the resulting post NSDD voltage across VCB is much less i.e. about 1.5 pu. While with deteriorated VCB, Fig. 12, with I_{ch} as 2 A and di/dt as 250 A/μs the NSDD currents persist for about 20 μs and the post NSDD voltage across VCB is above 2 pu. The simulation shown in Fig. 9 and Fig. 10 pertain to VCB chopping current I_{ch} of 1 A and di/dt of 100 A/μs.

B. *Restrikes due to NSDD*

The post NSDD voltage oscillations in the isolated circuit persists for a long time as there is very little damping at the frequency of oscillations. Hence, after some time when the source side voltage reverses the voltage across the VCB can reach to a larger value. Fig. 13a show a longer view of voltage across VCB, till 10 ms, after termination of NSDD for the case with deteriorated VCB with I_{ch} of 2 A and di/dt of 250 A/μs. It can be observed that voltage in one of the phase goes beyond 90 kV i.e. much higher than 3 pu. Hence, there is high probability of restrikes in this case. For comparison, the post NSDD voltage in case of healthy VCB is shown in Fig. 13b, in this case the worst case voltage stress across VCB is around 2 pu.

So, it shows that combination of deteriorated VCB contacts along with a inrush current limiting reactor can cause extension of NSDD current and may ultimately lead to restrikes in VCB. The restrike is possible even in case of delayed NSDD when the capacitor bank is in discharged state. Next we discuss one possible solution to this mode of failure of VCB.

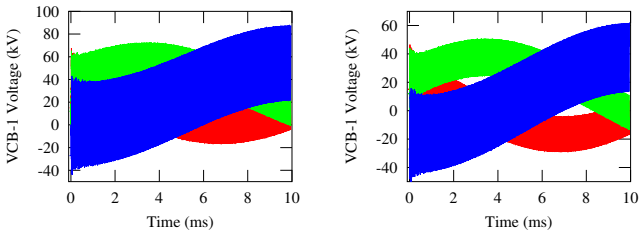


Fig. 13: The post NSDD Voltage for half power frequency cycle - Short and Long NSDD time.

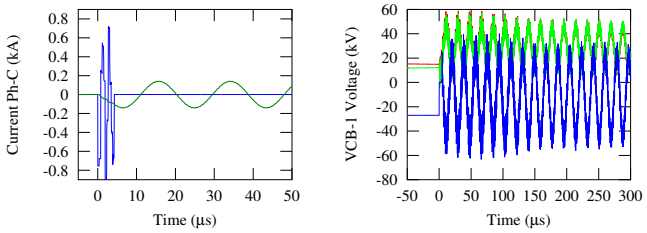


Fig. 14: The NSDD current and post NSDD Voltage with the reactor value reduced to one fourth.

V. Preventive Measures

A. Reduced value of inrush limiting reactor

The previous sections showed that the inrush current limiting reactor plays two roles in the failure of VCB. The first part is, the reactor connected at the capacitor bank terminal in ineffective in reducing di/dt of inrush current caused by source side parallel cables and the cable between VCB and the capacitor bank. On the other hand it extends the duration and maintain high magnitude high frequency inrush current during pre-arcing at every closing operation of VCB. This may deteriorate the contacts of VCB in long duration, increasing the NSDD duration. The second effect is that the post NSDD voltage stress across VCB is increased by due to the reactor. As seen earlier, this may cause restrikes in the VCB ultimately causing failure of VCB.

The inrush current limiting reactor in the present case limits the frequency of inrush to about 460 Hz, and peak inrush current to about 1 kA. While the VCB is rated to handle 4250 Hz and 20 kA peak inrush. It is possible to reduce the reactor value while still operating within the VCB capabilities. If the value of the reactors for both capacitor bank is reduced by one fourth value the frequency and peak value of inrush current due capacitor bank switching would double 1. With this reduced reactor value the frequency of inrush due to cable is not reduced, however, it gets damped early and hence reduces the contact deterioration. It also has significant effect in reducing the post NSDD voltage across the breaker as shown in Fig. 14. In this case the deteriorated VCB condition was considered for simulation.

B. Reactor position before cable

Change in configuration of the circuit to place the inrush current limiting reactor between circuit breaker and the cable would effectively counter the problem of inrush current due to the cables as well as the capacitor banks. However it is not always possible to get such configuration due to limitation of practical substation layouts. Even a small inductance of about 30 μH can limit this inrush currents due to cables. Such inductance occurs naturally in the air insulated outdoor substations with distances about 50 m [1]. In medium voltage GIS panels the reactors need to provided physically. Absence of such stray inductance is one of the reason this failure is observed in GIS breaker.

C. Controlled Switching

The change in inrush current limiting reactor value or its position may not be practical in all cases. In such cases the most effective solution is to apply the controlled switching of the capacitor bank. The controlled switching can eliminate the deterioration of contacts due to prestrikes. Generally in case of ungrounded capacitor banks, first two phases are closed simultaneously when their instantaneous voltages are equal. The third phase is closed after 5 ms of closing of the first two phases. This eliminates the capacitor bank inrush currents as well as the prestrikes. In most cases the controlled switching in this manner would solve most problems due to contact deterioration.

Even with controlled switching there can be a small discrepancy of few 100 μs between closing of first two phases. Hence, the phase closing first would still face the high frequency inrush current due to cables as the voltage in the phase is half of the peak value. To eliminate even this inrush current a change in the closing sequence is proposed. Instead of closing first two phases simultaneously, one of the phase should be closed when the voltage to ground in that phase is zero. This would eliminate the inrush current due to cables. The next phase is then closed after a delay of 1.66 ms when the voltage of the incoming phase is equal to the already connected phase, the final phase is closed as in previous case i.e. after delay of 5 ms. In simulation it is observed that while closing the first phase within 200 μs of the voltage zero the peak inrush current due to cables is limited to 50 A.

Applying controlled switching in medium voltage breakers also faces some impediments, as such breakers are usually operated in mechanically ganged manner. The controlled switching requires individual control of each pole of breaker. Hence any one of the above mitigation methods may be applied taking into consideration the cost and practicability of each method.

VI. Conclusion

This paper presented analysis of a rare case of VCB failure due to NSDD. The detailed analysis, verified through simulations, leads to counter intuitive result of adverse effect of large inrush current limiting reactor. The role of the parallel underground cables on source side and the cable connecting the VCB to the capacitor bank is also studied. The effect of cables and reactors is in two ways. It is shown that interaction of the high frequency inrush currents due to cables and the large reactor can cause VCB contact deterioration in long run.

In second way the large reactor causes higher voltage and extends the duration of post NSDD voltage across the VCB contacts and lead to VCB failure due to restrikes. Finally some of the practical ways are suggested for prevention of contact deterioration of VCB and avoid the failures.

ACKNOWLEDGMENT

The authors would like to thank Aaron Kalyuzhny of The Israel Electric Corporation Ltd., Haifa, Israel and Laszlo Prikler of Budapest University of Technology and Economics for the discussions and help in simulation.

REFERENCES

[1] *C37.012-2005 IEEE Application Guide for Capacitance Current Switching for AC High-Voltage Circuit Breakers*, IEEE Std., 2005.

[2] *IEC 62271-100 High-voltage switchgear and controlgear - Part 100: Alternating current circuit-breakers*, IEC Std., 2008.

[3] A. Kalyuzhny, "Switching capacitor bank back-to-back to underground cables," *To be published*. [Online]. Available: grouper.ieee.org/groups/td/cap/AaronKalyuzhnySwitchingCapacitorsUndergroundCables_Paper.pdf

[4] R. Smeets, R. Wiggers, H. Bannink, S. Kuivenhoven, S. Chakraborty, and G. Sandolache, "The impact of switching capacitor banks with very high inrush current on switchgear," *Cigre*, 2012.

[5] R. Smeets and A. Lathouwers, "Non-sustained disruptive discharges: test experiences, standardization status and network consequences," *IEEE Transactions on Dielectrics and Electrical Insulation*, vol. 9, no. 2, pp. 194–200, Apr. 2002.

[6] R. Smeets, A. Lathouwers, and L. Falkingham, "Assessment of non-sustained disruptive discharges,(NSDD) in switchgear, test experience and standardization status," *Cigre*, 2004.

[7] R. Smeets, A. Lathouwers, L. Falkingham, and G. Montillet, "A summary of non-sustained disruptive discharges (NSDD) in vacuum switchgear," in *Power Engineering Society General Meeting, 2005. IEEE.* IEEE, june 2005, pp. 2260–2266.

[8] H. Schellekens, "Capacitor bank switching with vacuum circuit breakers," in *Electricity Distribution, 2008. CICED 2008. China International Conference on*. IEEE, Dec. 2008, pp. 1–7.

[9] B. Kondala Rao and G. Gajjar, "Development and application of vacuum circuit breaker model in electromagnetic transient simulation," in *Power India Conference, 2006 IEEE*, Nov. 2006, pp. 1–7.

[10] J. A. Martinez-Velasco, *Power system transients: parameter determination*. Boca Raton, FL: CRC Press, 2010.

[11] B. Gustavsen, J. Martinez, and D. Durbak, "Parameter determination for modeling system transients-part ii: Insulated cables," *Power Delivery, IEEE Transactions on*, vol. 20, no. 3, pp. 2045 – 2050, July 2005.