Efficient Techniques for Real Time Simulation of MMC Systems

T. Maguire, B. Warkentin, Y. Chen, J. Hasler

***Abstract*-- There is movement toward creating HVDC grids containing many HVDC terminals and employing Modular Multi-level Convertors (MMC). Each of the many convertors will typically include 6 valves. Each individual valve in a convertor can contain hundreds of Voltage Source Convertor (VSC) bridges of either the full or half bridge variety. Consequently, efficient simulation algorithms are required in order to be able to simulate these schemes in real-time using time-steps of 2 or 3 microseconds. This paper discusses simulation techniques that provide the required efficiency.**

A surrogate network topology is described that represents the real valve behavior but requires significantly less computational power for simulation. First, a processor-based model is described. Subsequently, implementation details are provided for computing the model using the parallel hardware architecture of a Field Programmable Gate Array (FPGA). A single FPGA is used to model three separate valve models each containing 512 submodules (SMs). In order to demonstrate the accuracy of the proposed real-time methods, comparisons are provided between the results produced by the FPGA-based model, a simplified processor-based model calculated on the real-time simulator and the simplified model implemented in PSCAD.

***Keywords*: Modular multi-level converter, half-bridge, full-bridge, submodule, FPGA**

I. Introduction

Real-time Hardware-In-the-Loop (HIL) testing of the control systems that control the individual SMs in MMC valves has been conducted by the manufacturers for many years.

In some cases, the number of SMs in the MMC valve was relatively small at 40 or 50 SMs per valve. In such cases, the processor based valve models received separate firing control input for each SM. In other cases, where the number of SMs per valve was in the hundreds, sophisticated models [1] have been developed that work on average capacitor voltage. Neither approach has provided support for real-time modeling of internal MMC valve faults.

The work described in this paper was driven by the need to provide a real-time simulation model that could represent 512 SMs per valve with individual SM control input and with representation of internal MMC valve faults. The decision was made to create an algorithm that would be able to take advantage of the massive parallel processing resources that are available on FPGA chips.

Basically, an MMC valve consists of a reactor and a chain of series-connected half- or full-bridge SMs. A surrogate network for an MMC valve is described that has a modified topology compared to the real valve but produces the same computational result in all significant aspects. The surrogate network consists of three (3) series sections: the reactor section, the blocked SM section, and the deblocked SM section. The particular SMs to be included in the blocked and deblocked sections is determined in each time-step prior to the calculation of new Dommel [2] history terms and is based on external firing pulse input at that instant in time.

The paper is organized as follows: Section II discusses the surrogate network for both the half- and full-bridge MMC valves. Section III describes a valve model for calculation in real-time on a processor with individual SM firing control input. Section IV describes the implementation of the same valve model for calculation on an FPGA along with methods of representing various internal valve faults. A simplified processor-based valve model is discussed in Section V which receives control input consisting of only a block/deblock signal and the number of deblocked SMs that oppose/promote current. The simulation results are provided in Section VI. Finally, the conclusion is given in Section VII.

II. Surrogate Network for the MMC Valve

An MMC valve includes a reactor and a chain of series-connected half- or full-bridge SMs. Figure 1 illustrates an MMC valve containing a few half-bridge SMs, but in reality a valve may contain hundreds of SMs.

A surrogate network for an MMC valve containing half-bridge SMs is shown in Figure 2. The surrogate network has a modified topology compared to the real valve but produces the same computational result in all significant aspects. The surrogate network consists of three (3) series sections: the reactor section, the blocked SM section (“Blocked SM”), and the deblocked SM section (“In +ve SM”). The particular SMs to be included in the blocked and deblocked sections are

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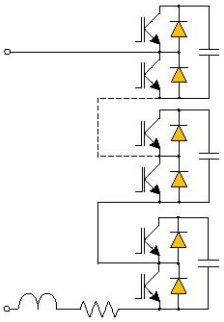

Figure 1. Half-bridge MMC valve.

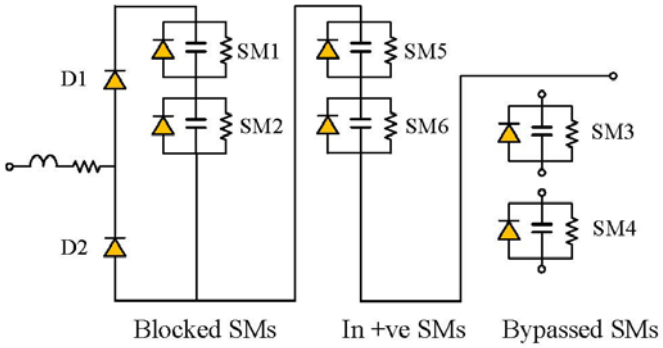

Figure 2. Half-bridge surrogate network topology

determined in each time-step prior to the calculation of new Dommel history terms and their selection is based on the external firing control input at that instant in time. The SMs that are not included in the blocked or deblocked sections during a time-step, referred to as “Bypassed SMs”, are allowed to discharge in isolation according to the RC time constant of the particular SM.

There are two main characteristics of the individual SMs that support the equivalent surrogate network. The first characteristic is that individual SM capacitors cannot charge to negative voltages because of the diodes connected across them. Consequently, the fundamental building block for the surrogate network consists of the parallel connection of a capacitor, a discharge resistance and an upward-directed diode as shown in Figure 2. This parallel connection is referred to in this paper as a "SM capacitor branch". In the FPGA-based version of the model, the SM capacitor branch can also include an additional switchable resistance to enable a controlled fast discharge. In the electromagnetic transient simulation, each SM capacitor branch is represented by a Thevenin branch consisting of a resistance and a series history voltage source *Vhc*. This branch is the Thevenin equivalent of the usual conductance and parallel current source used in the typical Dommel branch [2] representation.

Fortunately, it is not actually necessary to explicitly model the diode as a switched element in the simulation. The diode only prevents the capacitor voltage (*Vc*) in the "SM capacitor branch" from going negative. Without explicitly representing the diode, negative *Vc* can be avoided in the algorithm by resetting negative values of *Vhc* and *Vc* to zero whenever negative voltage occurs. It is important to do resetting of both *Vc* and *Vhc* in order to avoid the possibility of numerical oscillations.

Consequently, whenever multiple SMs are connected in series in a section as in Figure 2, the multiple SMs can be reduced to one equivalent Dommel branch containing a summed resistance and a summed series history voltage term.

The second characteristic of the SM that supports the equivalent surrogate network is that the diodes in each blocked SM always switch synchronously with the diodes in all other blocked SMs according only to the direction of the overall MMC valve current. Consequently, if the MMC valve current is charging the capacitor in one blocked SM then the capacitors in all blocked SMs are being charged. Overall MMC valve current never discharges the capacitors of blocked SMs.

Accordingly, diodes D1 and D2 in the surrogate network in Figure 2 are sufficient to assure that the overall MMC valve current causes the correct charging to occur in all SM capacitors in the blocked SMs. It is not necessary for every blocked SM to have a separate pair of diodes. Of course, individual SM capacitors can discharge during a simulation according to local SM effects such as discharge through the parallel R, activation of a fast-discharge branch or application of a short circuit fault on the SM capacitor.

Figure 3 illustrates the surrogate network for a valve containing (N=6) full-bridge SMs. Actual MMC valve current goes through 1 IGBT/diode switch per SM in a half-bridge valve and 2 IGBT/diode switches per SM in a full-bridge valve. In the surrogate network, the valve current goes through 1 diode for the half-bridge and 2 diodes for the full-bridge. Therefore, the representation of diodes D1, D2, D3 and D4 in the surrogate networks each must include the forward voltage drop of N IGBT/diode switches. Consequently, the diodes D1, D2, D3 and D4 are each represented according to the details illustrated in Figure 4.

Figure 2 also shows a section of series connected SM capacitor branches (“In +ve SM”) that are deblocked and inserted with a +ve reference direction. These SM are charged by +ve MMC valve current (downward) and discharged by –ve current. The individual upwardly-directed SM diodes in the deblocked section serve a significant purpose. When current flows upward through a particular deblocked SM, the current will pass through the capacitor until the +ve charge on the capacitor is depleted. If in extreme operating conditions, the +ve charge on the capacitor is completely depleted, then the upward current will transfer to the upwardly-directed diode and the capacitor will not charge to a -ve voltage. It is important to have a separate upwardly-directed diode in parallel with each deblocked SM capacitor in the surrogate network because the charge on the individual SM capacitors could be depleted at different times causing diodes to switch ON at different times.

For the half-bridge MMC valve shown in Figure 2, the SM capacitor branches in the deblocked section are all inserted

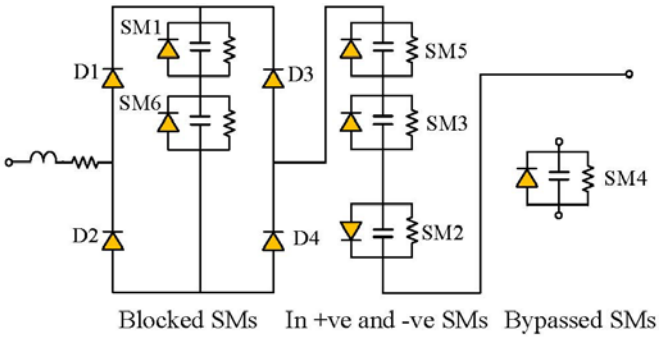

Figure 3. Full-bridge surrogate network topology

with a +ve reference direction so as to be charged positively by +ve MMC valve current. However, in a full-bridge MMC valve model such as shown in Figure 3, it is possible to insert SMs with a -ve reference direction such as submodule SM2 in Figure 3. Typically, at a particular time during normal operation, all of the SMs in the deblocked section will have either the +ve reference direction or the -ve reference direction. However, if firing input dictates, the deblocked SM section for a full-bridge valve can contain a mixture of SM inserted with the +ve reference direction and the -ve reference direction as shown in Figure 3. The present model supports that possibility.

III. Processor-Based MMC Valve Model

The processor-based models for half- and full-bridge MMC valves use the surrogate networks explained above with reference to Figures 2, 3 and 4. Generally, one valve is modeled on one processor and the modeled valve can contain about 40 SMs in the case of a full-bridge valve and about 50 SMs in the case of a half-bridge valve. Of course, this is dependent on the other models that are handled by the particular processor in the small time-step of 2 to 3 µs.

The main difficulty with the processor-based MMC valve models is the amount of I/O required to be communicated between the valve model and the external physical controls. Initially, digital input and analog output cards were considered for handling the I/O. However, with perhaps 40 SMs per valve, there would need to be more than 240 analog output channels per convertor. Also, actual MMC controls often receive their signals through fiber communication and the controls do not actually have pre-existing analog input ports. Therefore, the use of normal simulator I/O cards was abandoned.

The more practical approach of direct communication by fiber-optic cable was chosen. A model was prepared to execute in the small time-step on the processor to handle fibre-optic communication between the processor and the FPGA on a Xilinx ML507 or ML605 development board. IP firmware was prepared for the FPGA board so that it could also communicate over the fiber. The controls manufacturer then prepared additional IP firmware for the FPGA so that the FPGA board could act as a translator between the simulator

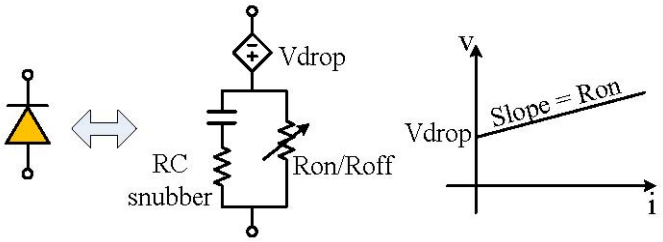

Figure 4. Representation of the diode in the surrogate network topology

processor and the physical controls under test. In this way, capacitor voltages and valve current were passed to the controls and firing pulse information was passed back to the convertor model.

The diodes D1, D2, D3 and D4 used in the surrogate network are represented using switched resistances, as shown in Figure 4. Also, SM capacitor branches are routinely included and removed from the blocked and deblocked SM sections based on firing input. Such switching would normally force decomposition of the conductance matrix of the small time-step network as is normally required by the Dommel algorithm. However there is inadequate time to do such decomposition. Therefore, it was decided to isolate the valve branch from the small time-step network by using a Bergeron transmission line model as shown in Figure 5 having a travel-time of ½ small time-step or about 1.5 µs. The equations used for the ½ time-step T-line model are exactly the equations used in the normal electromagnetic transients model of a Bergeron transmission line and the same small time-step size is used at both ends of the line. However, the solution points at each end of the line are shifted by ½ time-step with respect to each other in order to accommodate the ½ time-step travel time. The short travel-time keeps the shunt capacitance of the interface T-line very small. For instance, if 1 milli-Henry of inductance is shifted out of the MMC reactor into the interface T-line, then the shunt capacitance is an insignificant 2.25 nano-Farads for a travel-time of 1.5 µs. The configuration of the interface T-line as shown in Figure 5 permits the MMC valve model to be connected between any two nodes in the small time-step network. This provides the needed flexibility in connecting the MMC valve model into the small time-step network.

In the case of the half-bridge MMC valve model, each half-bridge SM is controlled by a separate pair of bits. Thus, 16 half-bridge SMs can be controlled by the bits in one 32-bit integer word. The 2nd Least Significant Bit (LSB) is a deblock bit. If this 2nd bit is 0, then neither IGBT in the half-bridge SM is fired. The LSB is only used when the deblock bit is 1. In that case, an LSB of 0 causes the bottom IGBT to be fired and an LSB of 1 causes the top IGBT to be fired. Therefore, an LSB of 1 causes the deblocked SM to be inserted +ve as discussed above. An LSB of 0 causes the deblocked SM to be bypassed. A similar approach is used for the full-bridge SMs.

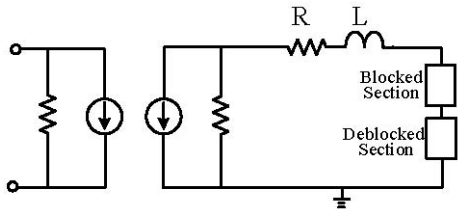

Figure 5. The T-Line Interface in the surrogate network topology

IV. FPGA-BASED MMC VALVE MODEL

The goal of modeling 512 SMs per valve in the small time-step using a processor is not practical, particularly if the goal includes representation of internal MMC valve faults. Therefore, a different approach was selected.

It is widely known that if a mathematical computation can be separated into a large number of isolated parallel computations then an FPGA chip may be a good choice for executing the computations quickly. Consequently, an MMC support unit containing a Xilinx ML-605 FPGA board was prepared as shown in Figure 6. The MMC Support Unit communicates with the small time-step network processor over a fiber connection.

The FPGA-based MMC valve model uses the surrogate networks and ½ time-step interface T-line discussed above. In the FPGA-based MMC valve model, the network end of the interface T-line shown in Figure 5 is computed on the small time-step network processor while the MMC end of the interface T-line is solved on the FPGA. T-line injections are exchanged between ends over the fiber. The interface between the small time-step network and the MMC valve model is highly stable because it is merely a normal T-line model.

The fiber between the processor and the FPGA also carries control signals from the processor to the FPGA for the purpose of applying various faults in the MMC valve model. Signals are also sent from the FPGA to the processor including minimum, maximum and average SM capacitor voltage. These signals can confirm that the MMC controls under test are balancing SM capacitor voltages acceptably well.

It was found that three separate valve models, each containing 512 SMs, could fit into a single FPGA. When the actual valve to be modeled contains less than the full 512 SMs, then the superfluous SMs are permanently bypassed by fictitious firing control input so that they do not have any effect on the simulation. However, the computation is always done for all 512 SMs. This allows the same firmware to be used in the FPGA regardless of the number of SMs in a particular MMC valve. Constants dependent upon the specific SM parameters are downloaded to the FPGA at the start of the simulation.

Certain stages of the MMC valve computation are not suitable for parallel computation. The overall surrogate network on the FPGA contains only 3 nodes when the "Blocked SM" chain and "In +ve SM" chain in Figure 2 are considered as two consolidated branches and the surrogate network is placed as a branch into Figure 5. The calculation involved in finding the voltage on the MMC valve branch and the voltages on the two internal nodes presents no significant opportunities for parallel computation. Also, the computation of currents down through the 2 chain branches is essentially serial in nature. However, these computations are fairly light.

Figure 6. FPGA-based MMC Support Unit

Once these two chain currents are known, the parallel computation for the SMs can begin. For organizational purposes, the 512 SMs are divided into 8 permanent groups of 64 SMs before the simulation begins. The variables for the 64 SMs in a group are passed through pipelined computational resources on the FPGA that are dedicated to that group. The 1st SM in the group takes about 200 nanoseconds to pass through the computations. However, because of the pipelining of the computations for the group, the computations for each additional SM in the group only require an additional 10 nanoseconds per SM. Therefore, the parallel computations for all 512 SMs can be completed in about 840 nanoseconds.

The first pipelined computations required for a particular SM depend upon whether the old state of the SM is the "blocked" state, "inserted +ve" state or the "bypassed" state, as determined by previous firing control input. The old state determines the particular chain current that is used in calculating the new SM capacitor voltage, *Vc*. Of course, if the old state of the SM is "bypassed" then no current is used in the capacitor voltage calculation. The selected current and the SM old history voltage term *Vhc* are used to find the new SM capacitor voltage, *Vc*. Once the new *Vc* is obtained, a lower limit of 0 is applied to *Vc* to account for the presence of the diode in the SM capacitor branch. The new capacitor voltages are available for sending out to the physical controls as soon as they are produced.

At this point, new firing control input is used to determine whether the new state of the SM in the next step will be "blocked", "inserted +ve" or "bypassed". With reference to Figure 2, the new state of each SM determines whether the particular SM will be placed in the "Blocked SM" chain or in the "In +ve SM" chain or whether the SM will be "Bypassed". The current in the selected chain is used along with the SM capacitor voltage *Vc* to produce a new capacitor branch history voltage term *Vhc* for the SM. A lower limit of 0.0 is applied to *Vhc* in order to account for the diode in the SM capacitor branch.

Within each group of 64 SMs, as each individual SM is

processed in the pipeline, the new SM resistance and new SM history voltage *Vhc* are respectively accumulated into a resistance sum and a history voltage sum for the particular chain to which the SM was assigned according to the new state. Therefore, when computations for the 64 SMs in a group are complete, there are resistance sums and history voltage sums for the "Blocked SM" and for the "In +ve SM" chain in the group. The sums for the 8 groups are combined into a consolidated resistance and history voltage source for the total "Blocked SM" chain and a consolidated resistance and history voltage source for the total "In +ve SM" chain.

The opportunities for parallel calculation are complete at this point in the computations. The consolidated Thevenin branch for the "Blocked SM" chain and the consolidated Thevenin branch for the "In +ve SM" chain are inserted into the network shown in Figure 2. Subsequently, by a process of reduction, the entire MMC surrogate network is converted into a single conductance and parallel current source. From that point the circuit computations continue in the usual way.

The capacitor voltages and MMC branch currents are sent out over fibers from the front of the MMC Support Units to external physical controls using an Aurora communication protocol. In return, the external physical controls send firing control input to each SM in the valve model over a fiber. The 8-bit input word to each SM in the FPGA-based model can include a deactivation signal bit and a fast-discharge signal bit. A particular SM responds to a deactivation signal by going into bypass mode regardless of the firing control bits. This mimics the closing of the SM mechanical bypass switch. Figure 7 shows two MMC Support Units connected to communicate with MMC controls, developed in-house by RTDS Technologies, also implemented on MMC Support Units. These simple MMC controls were created so that operation of the MMC valve model could be confirmed. In connecting the physical controls of particular manufacturers to the MMC Support Units which model the valves, it will usually be necessary to translate communication with the particular physical controls to the Aurora protocol used by the MMC Support Units.

The FPGA-based valve model supports various internal valve faults that can be initiated from the connected simulator processor. The inductance of the MMC reactor can be dynamically reduced to simulate a turn-to-turn fault in the valve reactor. The voltage on capacitors that are pre-selected by the User can be forced to zero to simulate capacitor shorting faults. The capacitance of pre-selected SM capacitors can be reduced during the simulation to simulate a partial loss of capacitance in an SM. A range of contiguous SM in a valve may be forced into bypass regardless of the firing control input in order to simulate a fault between two points in the valve. And of course, the full range of AC bus and DC rail faults can be applied. The faults can be applied simultaneously within a valve in any combination.

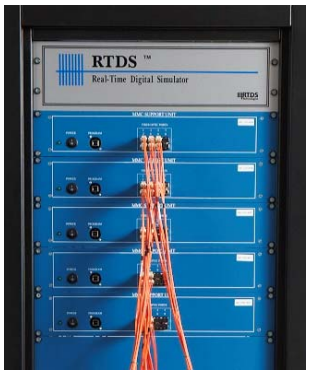

Figure 7. Fiber optic cable connection between MMC valve FPGAs and control FPGAs.

V. Processor-Based MMC Valve Model with Internal Capacitor Voltage Balancing

In some cases it is desirable (e.g. system level operation and performance studies) to conduct simulations in which only the high level functions of the MMC control are represented. These high level control functions may be performed by a physical controller or they may be simulated in the large time-step control blocks of the simulator. In such simulations, no firing control input is created for individual SMs and the full processor-based or FPGA-based valve models cannot be used. For these studies, the control signals produced may be limited to a block/deblock signal and an order for the number of SM that the control would insert into the MMC valve path. Consequently, an MMC valve model has been prepared which represents the contribution of individual SM to the valve output wave but which receives only a block/deblock signal and the number of SM to be inserted with +ve or –ve reference direction.

The model works on the principle that at the beginning of each small time-step the voltage on all capacitors is equal. During the ensuing small time-step all of the SM capacitors are notionally cycled through the inserted state and the bypassed state with state duration selected according to weightings that are determined by comparing the SM order number with the total number of SMs. The result is that at the end of the small time-step all of the capacitors still have equal capacitor voltages. In fact, computations are done for only one "Blocked SM", one "In +ve SM" and one "Bypassed SM". The change in the calculated voltages for the three SMs is multiplied by their number to find the net voltage change on all SMs. The net voltage change is distributed equally to all SMs. Therefore, this simple MMC valve model executes with apparent ideal internal SM capacitor voltage balancing control.

The model is fairly light weight from a computational perspective. Therefore, the six (6) valves of an MMC convertor, with up to 640 SMs per valve, can be simulated on a single card containing two (2) processors. The valve output voltage wave contains steps according to the SM order number. No internal faults are represented in this simple

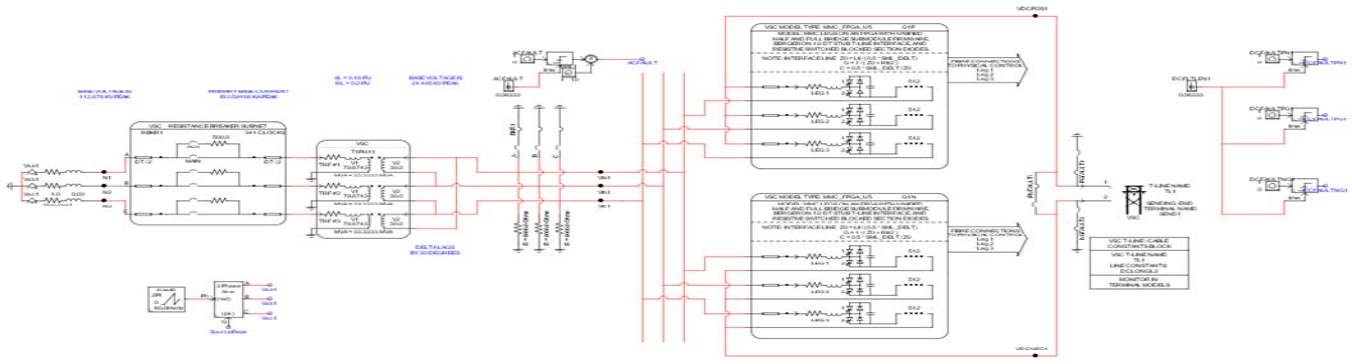

Figure 8. One end of a point-to-point HVDC MMC system

model.

As noted above, the block/deblock signal and SM order number must be created by the high-level control functions of an MMC valve control. The MMC valve model would send the valve current and average capacitor voltage to the control. The high-level control functions can exist in a physical controller in which case I/O signals are exchanged between the control and the valve models using simple I/O cards. When there is no physical high level controller available, the control can be simulated in the large time-step (50 µs) using standard control blocks.

In either case, the model with internal voltage balancing control can be used for modeling one end or both ends of an MMC-based HVDC link. If the model is used for one end only, the other end could be modeled using the full processor-based or FPGA-based models discussed in Sections III and IV above.

VI. Simulation Results

A simple point-to-point MMC-based HVDC link was simulated to demonstrate the proposed FPGA-based modeling techniques. Figure 8 illustrates the power system for one end of a point-to-point MMC-based HVDC link using the FPGA-based model with 512 SMs per valve. A three-phase source feeds a WYE-DELTA three-phase transformer through a three-phase breaker. The transformer supplies the three-phase MMC converter. Various fault switches are illustrated. The main parameters of this system are given in the Appendix.

Figure 9 illustrates plots captured during deblocking of the MMC-based HVDC link. Each plot contains a signal from the simplified real-time processor-based model compared with a corresponding signal from the simplified model implemented in PSCAD. Figure 9(a) illustrates the current in kA in the top A-phase valve at one end of the DC link. Figure 9(b) illustrates the current in the top A-phase valve at the other end. Figure 9(c) illustrates the mid-point DC voltage in per unit. It is clear that simplified real-time processor-based model produces substantially the same result as the PSCAD version.

Figure 10 illustrates plots similar to those illustrated in Figure 9 except that in Figure 10 the results from the detailed

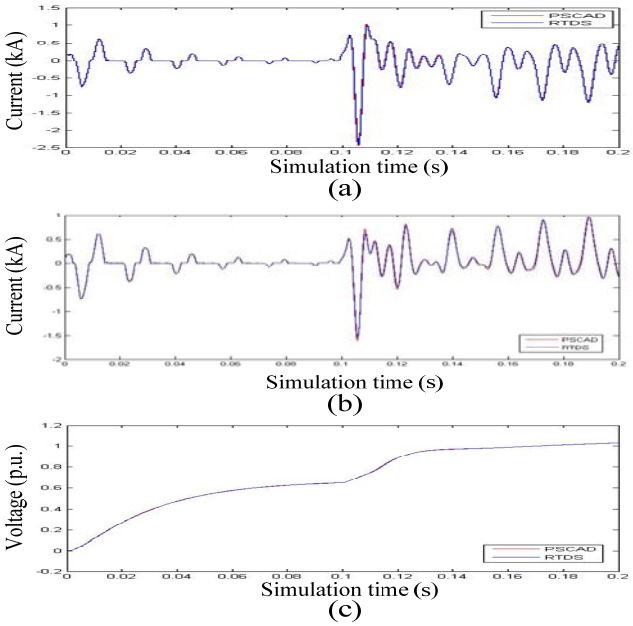

Figure 9. Comparison of simplified real-time and PSCAD valve model results during deblocking: (a) and (b) MMC branch currents of top valve Phase A at both ends in kA; (c) mid-point DC voltage in p.u.

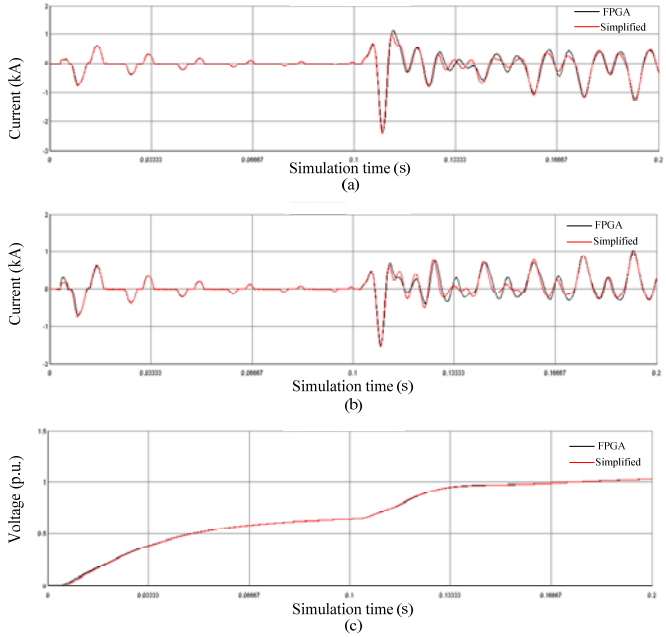

Figure 10. Comparison of FPGA-based real-time and simplified real-time model results during deblocking: (a) and (b) MMC branch currents of top valve Phase A at both ends in kA; (c) mid-point DC voltage in p.u.

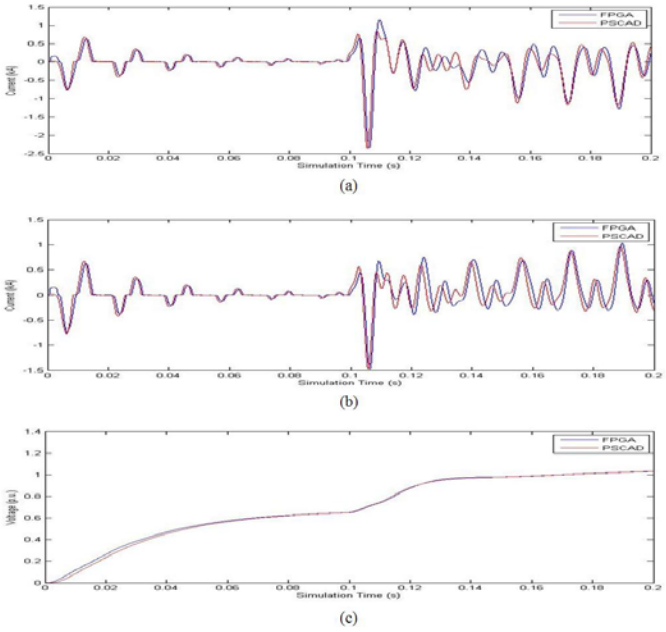

Figure 11: Comparison of FPGA-based real-time to detailed PSCAD model as in Figure 10

FPGA-based real-time model are compared with the simplified processor-based real-time model. The small time-step in the FPGA-based model is 2.63 µs while the time-step for the simplified case is 3.33 µs. It is clear that the detailed FPGA-based real-time model with external FPGA-based controller produces substantially the same result as the simplified real-time processor-based valve model, having regard to differences such as point on wave and the use of the detailed control in the FPGA-based model.

Figure 11 illustrates plots similar to those illustrated in Figure 10 except that in Figure 11 the results from the detailed FPGA-based real-time model are compared with a detailed model in PSCAD developed independently by Mr. Jianzhong Xu, a Ph.D. student visiting the University of Manitoba from North China Power Engineering University, NCEPU. The high level control in this PSCAD model is similar to that in the RTDS detailed case, but the capacitor voltage balancing control is quite different. Regardless, the results are similar.

VII. Conclusions

Surrogate networks for half- and full-bridge MMC valves have been described that have modified topologies compared to the real valves, but produce the same computational results in all significant aspects.

The surrogate networks facilitate the efficient real-time simulation of MMC valves with large numbers of SM on FPGAs. The mapping and pipelining of computations on the FPGAs is explained. Approaches for representing various internal valve faults are also explained.

A simplified MMC valve model is explained that provides internal capacitor voltage balancing control. This model is useful in testing high-level controls such as may be of particular interest when modeling DC grids where the low level voltage balancing control is of less interest.

Simulation results are presented showing good comparisons between those produced by the detailed FPGA-based MMC valve model, the simplified real-time processor-based valve model, and the non-real-time simplified model implemented in PSCAD.

VIII. Appendix

The case point-to-point HVDC MMC power system parameters are as follows:

Ac source: 138kV, R = 1.0 Ohm, L = 0.03mH; transformer ratings: 100MVA, 138kV/30kV, 18 % leakage; MMC reactor inductance: 0.03 mH; MMC reactor resistance: 0.0 Ohms; SM capacitance: 50000mF; nominal net DC voltage: 60kV; SMs per MMC valve: 512.

IX. References

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X. Biographies

Trevor Maguire graduated from the University of Manitoba with B.Sc.EE, M.Sc.EE and Ph.D. degrees in 1975, 1986, and 1992 respectively.

Employment experience includes time with Manitoba Hydro (1975-76), Manitoba HVDC Research Centre (1986-1994), and RTDS Technologies, Inc. (1994-present). He has an interest in real time simulation model development and also real-time simulation digital hardware development.

Bruce Warkentin received a B.Sc. in Electrical Engineering from the University of Manitoba in 1996. After graduating he joined RTDS Technologies Inc. working on integrating new hardware technologies into the RTDS simulator. Now he oversees hardware development with a personal focus on real time applications for microprocessor and FPGA based systems.

Yuan Chen received Ph.D. degree from the University of Alberta, Canada, in 2012. He is currently a simulation development specialist at RTDS Technologies, Inc. His research interests include real-time simulation of power systems and high performance computation (HPC).

Jean-Philippe Hasler received his M.Sc. degree in Electrical Engineering from the Ecole Polytechnique Federale de Lausanne, Switzerland in 1986.

Mr. Hasler joined ABB in 1986 where he was developing control systems and protection algorithms for multi-terminal HVDC. Since 1993 he is conducting power system and control studies for different FACTS applications.