Setup and performances of the real-time simulation platform connected to the INELFE control system

S. Dennetière, H. Saad, B. Clerc

***Abstract*- The VSC based HVDC link between France and Spain (INELFE project: France-Spain ELectrical INterconnection) will be the most powerful VSC link by 2015. This 2000 MW interconnection is composed of 2 parallel VSC links. For system studies and maintenance purposes, replicas of the control systems are acquired by the French (RTE) and the Spanish (REE) Transmission System Operators.**

This paper describes the hardware and software setup to perform Hardware In the Loop (HIL) simulations with the INELFE control system replicas. The converters and cables models used in the real-time simulation are presented. Modular Multilevel Converters present a major challenge for real-time simulation due to the large number of sub-modules and to the nonlinearities that shall be solved : transformer saturation and nonlinear characteristic of surge arresters that protect cables against switching transients.

The paper presents how these issues have been solved in order to be able to test the control system with AC and DC faults. A complete setup has been developed in order to validate the modeling approach. Hardware-In-the-Loop (HIL) simulations have been performed which includes the real-time simulator connected to an external generic control system having the same interface than the replica. Real-time performance and simulation accuracy are fully achieved with the proposed solution.

***Keywords*: Real Time Simulation, Electromagnetic transient studies, Modular Multilevel Converters (MMC), HIL simulation**

I. INTRODUCTION

Interconnections between national electrical grids have been historically developed along with each country's internal networks. Interconnections were initially used for external support in the event of failure affecting the security of the national electrical supply. However, it has been demonstrated that interconnections are not only useful for exceptional situations, but also offer advantages under normal operating conditions, such as optimizing the electrical power stations' daily production, increasing opportunities for operation with renewable energies, the creation of competition, improvement of supply conditions and black start operation.

In France, RTE is accelerating the development of its grid and several projects involved power electronic based equipment such as HVDC links, static VAR compensators. In the longer term, the share of power electronics connections into existing ac systems will significantly increase due to the massive penetration of wind power plants and HVDC links and grids. For several years, RTE has been involved in research and development activities to model, study and mitigate potential interaction issues between close HVDC links. To support these activities, numerical tools are needed that offer detailed modeling of HVDC components and controls while maintaining a good compromise between robustness, accuracy, and flexibility.

The usage of electromagnetic transient analysis tools (EMT-type) to test new technical solutions is continuously increasing in importance. EMT studies performed for the installation of new equipment on the grid are to ensure highest levels of reliability and availability. EMT-type simulation tools (offline and real-time) must provide reliable and accurate simulation results, advanced visualization and analysis capabilities to power system engineers. Therefore, RTE continues its direct involvement in the development and improvement of such tools as explained in [1]. For instance collaborations with École Polytechnique de Montréal in Canada and École Centrale de Lille in France, have been established for the development of models and tools suitable for EMT-type studies for Modular Multilevel Converters (MMCs). Some of these models are presented in [2], [3] and [10].

After the commissioning of HVDC and FACTS devices, manufacturers usually provide customers with a black box model of their control systems. These models suitable for EMT simulations are difficult to maintain during the lifespan of equipment for the following reasons: the models are usually based on a specific version of a simulation tool that might not be supported in the future, the models usually use static libraries that can be only compiled and linked using a specific compiler version, the models cannot easily follow changes in the actual control systems because manufacturers do not necessarily maintain modeling expertise on long term basis.

The solution is to continuously update control system models for replicating real controllers and related updates. This is a time consuming activity and another possibility, presented in this paper, is to use manufacturer supplied physical replicas of control systems.

As a consequence, to validate the various modeling approaches for the different range of phenomena and to demonstrate interoperability and the absence of detrimental interactions, RTE decided to use hardware-in-the-loop architectures, with the actual replicas of the physical control systems. In this area, as part of its ongoing HVdc projects, RTE has recently assembled a hardware-in-the-loop test facility called SMARte that uses the Hypersim simulator. The Hypersim [4]-[5] software is a real-time hardware in the loop simulation platform used for the simulation and testing of control systems. A collaboration on the development of

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Hypersim has been established between RTE and Hydro-Québec in 2012. This collaboration enables sharing development efforts and expertise. RTE has acquired its own real-time simulation laboratory based on Hypersim for installing control system replicas. Hypersim is now commercialized by Opal-RT.

RTE aims to expand this facility to meet its future project needs and to participate in the future development and improvement of the simulator.

II. SMARTE LABORATORY DESCRIPTION

In order to facilitate the maintenance and operation of control and protection systems in HVDC and FACTS devices, the replica of actual control system and protection cubicles are acquired by RTE and installed in the real time simulation laboratory called SMARTE and based in Paris La Défense. A replica is an exact copy of the actual control cubicles installed on site. Two types of replicas can be ordered: Study and Maintenance.

A. Study replica

The study replica is dedicated to functional verification, dynamic performance and protection studies. The replica is delivered 6 months before the commissioning of the real installation and is used for network studies between Factory Acceptance Tests (FAT) and Site Acceptance Tests (SAT) to test the control algorithms. These investigations may lead to updates or even modifications in control algorithms.

The Study replica is provided only with equipment relevant to network studies and redundancy is not included.

From a utility point of view the modelling of HVDC control systems for EMT studies is a quite complex task because actual controls may run on multiples platforms (CPU, DSP, FPGA…) and as a consequence simulation on a single CPU would require too much time. Moreover, the HVDC controls are based on algorithms that are protected by manufacturers due to IP rights. Therefore, replicas are useful to perform network studies without any simplifications or assumptions in control systems. Off-line or real-time control system models can be also validated with replicas.

B. Maintenance replica

The Maintenance replica is intended to help the preparation of on-site maintenance operations and operator trainings. The preparation of maintenance operations includes testing and validation of the upgraded system version before field implementation. In order to perform preparations for maintenance, validation of upgraded control system, fault diagnostics and training of operators, the Maintenance replica includes a set of control- and protection cubicles identical to the original cubicles in the converter substations with the same interfaces, including any redundant equipment implemented in the converter cubicles. The Maintenance replica is delivered during the commissioning of the actual control system cubicles.

III. THE FRANCE SPAIN HVDC INTERCONNECTION

A. Context

The electrical interconnection between Spain and France currently consists of four AC lines (the last line was built in 1982): Arkale-Argia, Hernani-Argia, Biescas-Pragneres and Vic-Baixas. These lines have a total commercial exchange capacity of 1,400 MW, meaning that they represent only 3% of the current maximum demand in the peninsula. The new HVDC electrical interconnection line between Spain and France has a length of 64.5 km with 2000 MW capacity. It connects the towns of Baixàs, in the Roussillon region (France), and Santa Llogaia, in Alto Ampordá (Spain). Converter stations are designed and built by SIEMENS. Prysmian Cables & Systems has been awarded the contract for the installation of cables. More information on this project is available in [6].

This new HVDC interconnection will be the first VSC installation operated and maintained by the French (RTE) and the Spanish (REE) Transmission System Operators (TSO). RTE decided to acquire competences in modeling and simulation of VSC based equipment. Competences in this field were required for the INELFE project but, above all, were mandatory for the numerous HVDC and FACTS projects that are planned in a near future in the French grid. Some EMT models have been developed in this context and are described in [2]. EMT study examples are provided in [7]. In addition to modeling activities in the field of FACTS and HVDC, RTE decided to build a real-time laboratory that hosts replicas of the control system cubicles installed on site. Studies with the real controllers connected to the Hypersim real-time simulator will be performed. Moreover this simulation platform will give an opportunity to validate the specific EMT models of the link.

B. Interconnection description

The interconnection is composed of 2 HVDC links. Each link has two MMC stations with a rated transmission capacity of 1,000 MW (+/-300Mvar) and a DC voltage of ±320 kV. A simplified single line diagram is presented in Figure 1. Each link is composed of 2 symmetrical monopole converters, 2 step down transformers and 2 underground cables. VSC-HVDC technology, using the modular multilevel converter (MMC) topology, has been selected for this project due to the dynamic performance, power flow control requirements and the low AC short-circuit ratio of the France-Spain system. More details on the converters topology and data are available in [7].

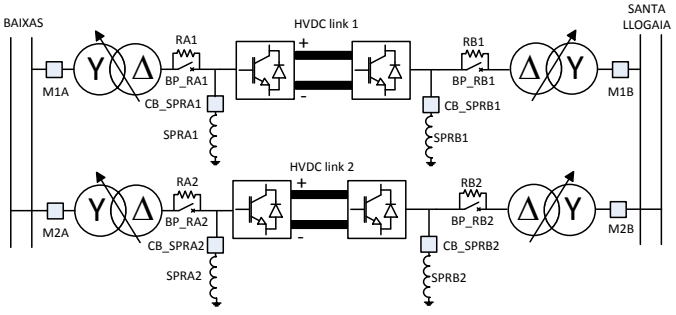

Figure 1 Single line diagram of the interconnection

C. DC bus faults and surge arresters

Due to the symmetrical monopole configuration no reference to ground is available in the delta side of the transformer. A ground fault on one pole will shift the other pole to about twice the dc voltage. Due to this overvoltage on the healthy pole, the converters of both stations have to be quickly blocked and the main ac breakers have to be tripped. This transient is not a switching overvoltage. Actually it is similar to a temporary overvoltage because it lasts 40 to 100 ms until the fault cleared by AC circuit breakers opening at both terminal stations. As explained in [8] and [9], the severe healthy pole overvoltage is limited by surge arresters installed on DC pole bus. These special surge arresters have a very high energy absorption capability.

IV. MMC MODEL FOR HIL TESTING

Several hundreds of levels are commonly used in multilevel converters. Detailed modeling of converters has been feasible in offline and real-time tools for a few years now. Some detailed models for real-time simulations are described in [10]-[12]. As explained in [13], due to the fact that the detailed simulation of the MMC requires a very high number of submodules and a massive amount of I/O, Siemens reduced the amount of hardware needed by using an equivalent circuit for the converter. The equivalent circuit is used in the real time simulation as well as in the offline simulation and helps to reduce the necessary computing power. Each of the six converter arms per station is simulated by a virtual phase module as described in Figure 2. N is the total number of SMs per arm. R_{ON} represents the linear conduction loss of an IGBT/diode device. i_{arm} is the arm current as described in Figure 4.

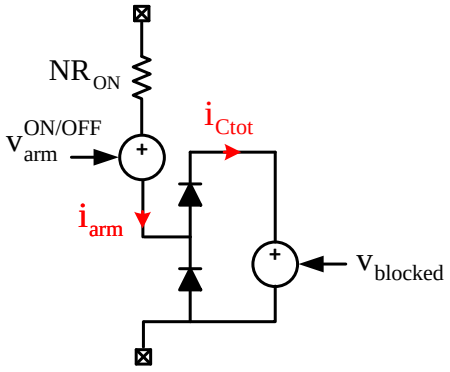

Figure 2 Equivalent circuit for a MMC half arm

Capacitor voltages in a converter arm are assumed to be perfectly balanced. As presented in [2], the validity of this assumption increases when the number of SMs per arm is increased and/or when the fluctuation amplitudes of capacitor voltages are decreased. Then the following assumption can be made :

$$v_{C_1} = v_{C_2} = \ldots = v_{C_i} = \frac{v_{C_{tot}}}{N} \quad (1)$$

The switching function of an arm can be defined as follow :

$$\frac{1}{N}\sum_{i=1}^{N} S_i = s_n \quad (2)$$

where S_i is the switching function that takes the value 0 when the state of SM_i is OFF and 1 when it is ON.

This function can be deduced at each time step by the total number of SM to insert. This number is sent by the modulation control (included in the physical controller for HIL tests). By deducing an equivalent capacitance $C_{arm}=C/N$ for each arm, the equivalent voltages can be calculated as presented in Figure 3.

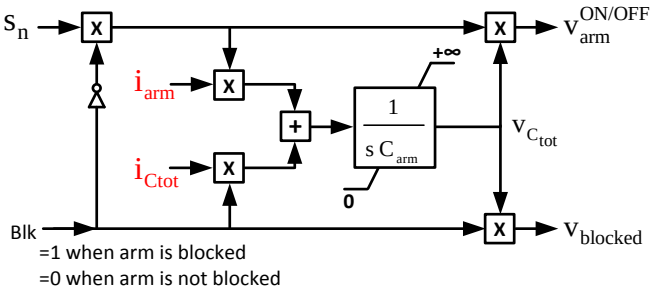

Figure 3 Equivalent capacitor voltage calculation

The equivalent circuit of a converter is presented in Figure 5. Surge arresters connected to cable terminals are represented by nonlinear resistors. The piecewise nonlinear characteristic is identical in offline and real-time simulations. It consists of 20 segments. A simplified view of the nonlinear characteristic is presented in Figure 4.

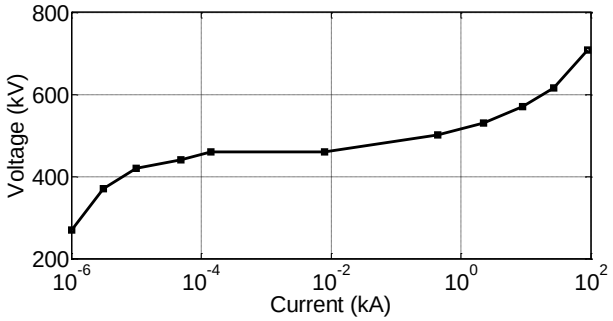

Figure 4 Nonlinear characteristic of surge arresters connected at cable terminals

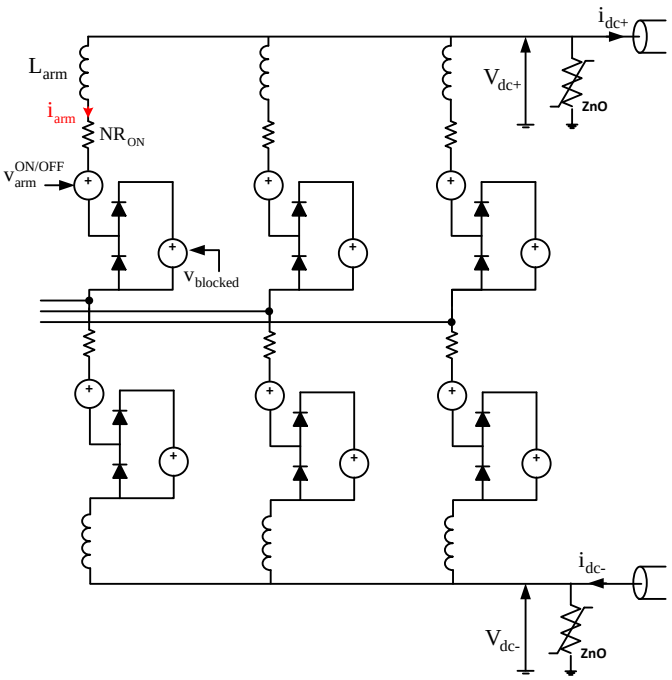

Figure 5 Equivalent circuit for a converter station

V. Presentation of the HIL setup and simulation results

A. Challenges for modeling MMC for HIL tests

Before implementing the converter model presented in section III in the real-time simulator Hypersim, this model has been implemented in the offline tool EMTP-RV [14]. As presented in [2] this simplified MMC model implemented in an offline tool has been validated against detailed converters models. It can gives accurate results for converters with more than100 SMs per arm when the capacitor voltage balancing control of SMs and the related protection system are out of scope of the studied test case. For testing actual controls for DC faults, surge arresters shall be modeled. This requirement complicates the simulation because it shall be computed with a time step smaller than 25µs (due to the Current Control sampling rate) and nonlinear characteristics of surge arresters shall be treated with iterations. These two requirements make the simulation very complex for real-time simulation even if a detailed converter model is not used.

B. Model validation

To validate the converter model implemented in Hypersim, the same converter and control models have been implemented in the offline tool EMTP-RV. The studied system is presented in [7]. Results given by these models are compared during starting sequence, ac and dc perturbations. The controllers of the MMC have been implemented in MATLAB-Simulink, exported in C code using the Embedded Coder toolbox, compiled as a DLL and imported automatically in the EMTP-RV simulation using the DLL interface. The same control model has been exported in C code and integrated with the generated code of the network modeled in Hypersim. This technical solution described in [15] is a straightforward to get rigorously the same control system in both software.

The control system model includes outer control (P/Q/Vdc/Vac control), inner control and circulating current suppression control as described in [2]. The modulation technique is the nearest level control proposed in [16]. Capacitor voltage balancing algorithm cannot be tested with this type of converter model.

The studied system includes surge arresters which characteristics are highly nonlinear when the dc voltage exceeds their protection level (see Figure 5). In order to be able to get accurate results with such nonlinear devices, nonlinear solvers are required. EMTP-RV uses a Jacobian-based nonlinear solver that is presented in [14]. Hypersim enables a nonlinear solver even for real-time simulation [17]. This is the only commercial real-time simulation software that proposes such a feature.

The real-time simulation of the studied system is achieved with a 20 µs time step. The task mapping automatically generated by Hypersim is presented inFigure 6.

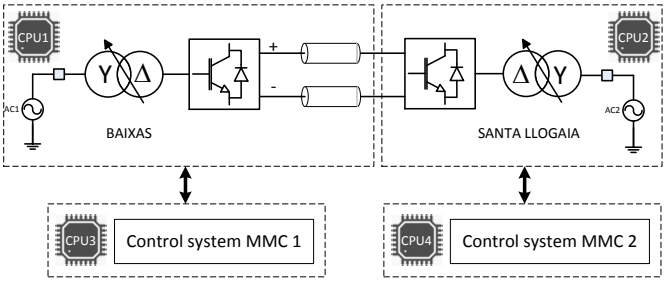

Figure 6 Task mapping of the SIL setup

The start-up sequence presented in [7] is tested on the studied system. The start-up process of the MMC is complex since at the beginning of the process all capacitors are required to be equally charged to a certain level before being able to operate. To energize link 1 (see Figure 1), let BAIXAS be the first station to be connected to the AC grid. The star point reactor is only grounded at BAIXAS (CB_SPRA1 close) to provide a voltage reference. After closing the AC grid breaker at BAIXAS (MA1), inrush currents are observed due to the saturation of transformers and capacitor charging. All module capacitors and DC cable capacitors are charged through the insertion resistors RA1 and the diodes of both sides. Upon stabilization of DC voltages, the insertion resistors are short-circuited thanks to the bypass breakers BP_RA1. Then the voltage rises across module capacitors and cables.

The DC voltage at BAIXAS (positive pole) obtained with the EMTP-RV and Hypersim models are presented in Figure 7 and Figure 8. Results given by offline and real-time tools are quite close.

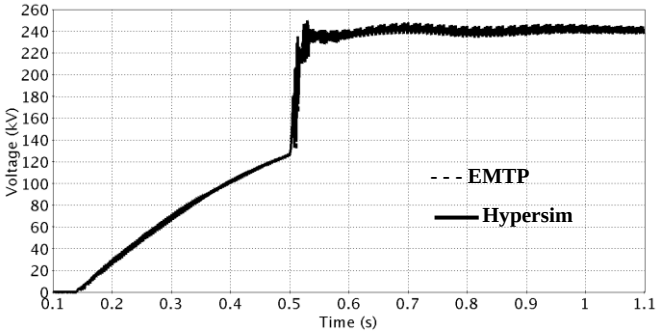

Figure 7 Positive pole voltage at cable terminal during starting sequence (Offline test)

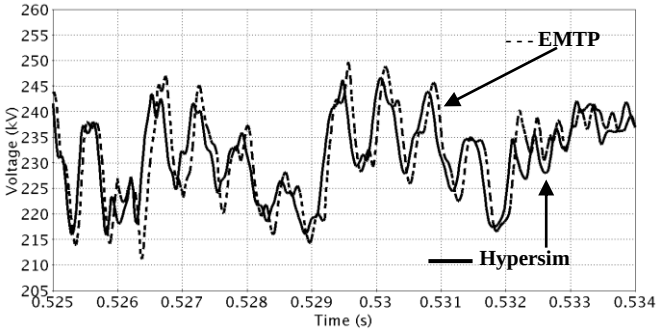

Figure 8 Zoom on positive pole voltage at cable terminals during starting sequence

Pole to ground faults are simulated in order to validate the converter models when the surge arresters conduct. When DC faults occur, pole-to-ground over-voltages on healthy pole can be observed due to the converter topology. Actually pole-to-pole voltage is controlled without any reference to ground. When a pole-to-ground fault occurs, the pole-to-ground voltage on the healthy pole can go up to 2 pu. To limit the overvoltage, converters are blocked immediately (~40 µs after fault detection), AC circuit breakers are opened after 2-3 cycles. Surge arresters play a substantial role in the limitation of DC over-voltages amplitudes. They are designed to limit the DC over-voltages and absorb a big amount of energy before the AC circuit breaker opening. When surge arresters limit the DC overvoltages, large currents are driven to the ground through the surge arresters. 5 iterations maximum are required at each time-step in Hypersim to get accurate results during this transient. These iterations do not generate any overrun during the real-time simulation at 20 µs. The voltage at cable terminal (healthy pole) is presented in Figure 9. Offline and real-time simulation results are in close agreement.

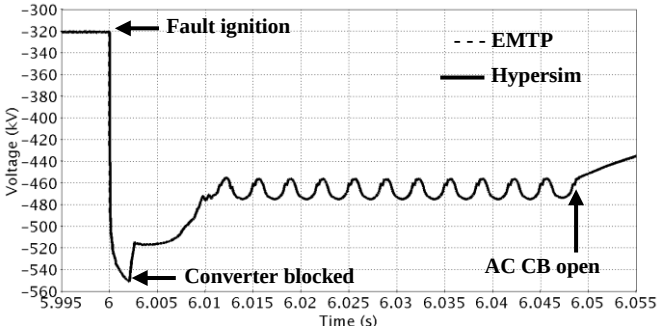

Figure 9 DC voltage at cable terminals (healthy pole) during pole-to-ground fault

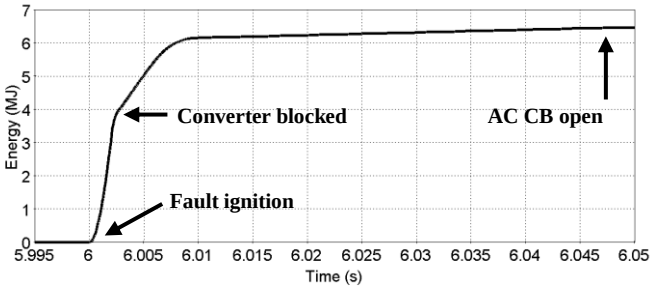

Figure 10 Energy absorbed by the surge arrester at cable terminals (healthy pole) during pole-to-ground fault

C. Model validation with HIL

For the final application, the real-time simulator shall be connected to the external controllers through copper wires by sending analog and digital signals for :

- the measured voltages and currents,
- the number of inserted sub-modules of each arm,
- the states of the circuit breakers

To validate the MMC model with HIL conditions, the control system used in the previous section for SIL testing has been implemented on a separated target as presented in Figure 11. Control systems for both converters are running in real-time on a separate target at a 20µs time-step on 2 CPU. This external control system is interfaced with the studied system through standard I/O interfaces (+/-10V for analog signals, +24V for binary signals). This interface is identical to the interface that will be provided by SIEMENS to connect the control system replica to the real-time simulator. Number and type of signals sent and received by the external controller are identical. This is particularly important to use the same I/O configuration in order to be able to test the real-time simulation performance prior to the delivery of SIEMENS control cubicles. Due to the time step used in the low level controller that is directly interfaced with the simulator, the studied system shall be simulated with a time-step smaller than 25µs.

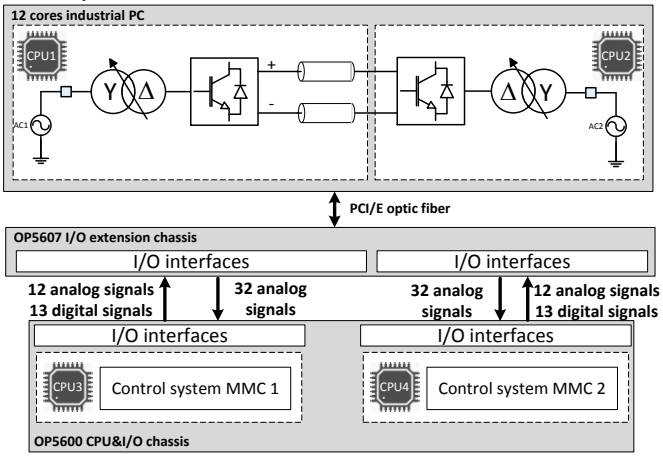

Figure 11 Overview of HIL set-up.

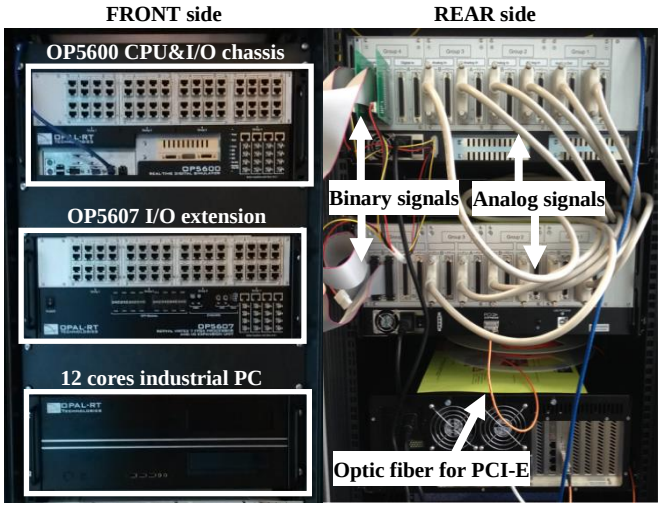

Figure 12 Hardware used for the HIL test bench.

The first test case consists in the energization of the HVDC link as described the previous section. DC voltage provided by the EMTP offline simulation and the HIL test bench are presented in Figure 13.

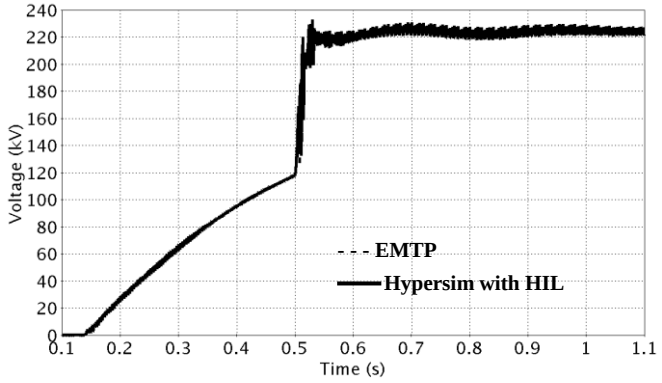

Figure 13 Positive pole voltage at cable terminal during starting sequence (HIL test)

The second test is a pole-to-ground fault as described in Figure 15.

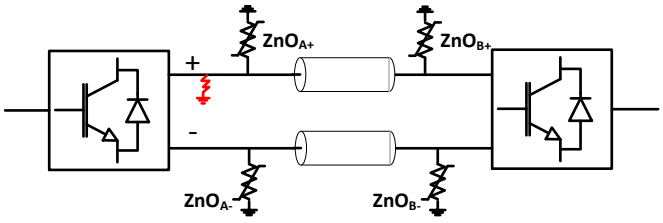

Figure 14 Pole-to-ground fault position

Converters are blocked 40 µs after fault detection and AC circuit breakers are opened 3 cycles later. Current in the surge arrester ZnO$_{A-}$ connected to the healthy pole is presented in Figure 15.

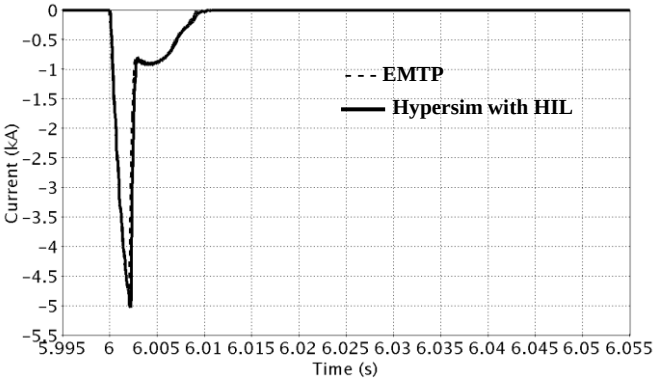

Figure 15 Current in the surge arrester connected to the healthy pole – (HIL test)

Results given by the offline simulation and the HIL platform are quite similar. The real-time simulation is achieved with a 20 µs time step even when 5 iterations are required for solving the nonlinear devices. The maximum execution time on CPU1 (see Figure 11) is 16.5µs and 13.5 µs on CPU2 when 5 iterations are required.

The voltages at cable terminals obtained with HIL are exactly the same than the voltage presented in Figure 9 with offline simulation.

VI. Conclusions

Due to the large number of HVDC equipment that will be installed in a near future on the French grid, RTE decided to be highly involved in the modeling of HVDC. MMC models for EMT studies have been developed and presented in [2] and [10]. RTE also decided to build a real-time laboratory that hosts replicas of the control system cubicles installed on site. Studies with the real controllers connected to the Hypersim real-time simulator will be performed.

This paper present a test bench that has been set up to validate the accuracy and performances of an Hypersim real-time simulation connected to a control system similar to the control cubicles that will be provided by SIEMENS in 2015. The main requirements were the following: real-time simulation shall run with a time step below 25µs and limitation of transient overvoltage by surge arresters shall be accurately modeled. The insertion of surge arresters in a real-time simulation is quite challenging because it requires iterations. This paper shows that the real-time simulation is achieved with a 20µs time step even when 5 iterations are required for solving the nonlinear devices.

This test bench is the first step to prepare the connection of the SIEMENS control replicas to the Hypersim real-time simulator. The next step will be to insert a detailed model of MMC on FPGA.

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