

Islanding detection improvement in Distributed Generation by using of mathematical morphology for frequency oscillation characterization

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Abstract—Islanding detection is one of the most challenging problems in distribution generation protection. This paper proposes an algorithm based on mathematical morphology to differentiate islanding from non-islanding events. During non-islanding events the frequency of the distribution generators oscillates at a higher frequency than in islanding events. The algorithm attenuates the higher frequency oscillation, enabling reliable island detection. The algorithm performance is evaluated and compared with the most used islanding protection algorithms, for many island and non-island events.

Keywords: *island protection, frequency protection, distributed generations*

I. INTRODUCTION

THE no intention islanding of Distributed Generators (DG) can cause risk to life, power quality deterioration, operational problems and damage to the system equipment and its loads. For these reasons the islanded operation of distribution systems has not being allowed, and the islanding detection is a requirement for connection GDs to the electrical system network.

In this way many energy utilities request the installation of remote controlled reclosers with transfer trip in the energy producer connection point. Others utilities request the construction of exclusive feeders with transfer trip. Although effective, these solutions can generate a very large financial cost, making it prohibitive for small DGs.

Many techniques have been proposed as an alternative to communication based methods, which can be divided into two categories: passive methods and active methods. The active methods inject small signs in the distribution system or force distributed generation to an abnormal situation where the connection to the system keeps the DG under normal

conditions. Disturbances in the distribution system may cause power quality deterioration and if the generators are connected next to each other, the interference created can impair the performance of these techniques.

Due to the lower cost of passive methods is common the use of anti-islanding schemes using protection functions such as: Rate of Change of Frequency (ROCOF), Under-frequency, Over-frequency, Vector Shift, Under-voltage and Over-voltage. Although these techniques are effective for islanding conditions with large power mismatch, passive methods may fail to detect low power unbalance. In addition, events like short circuits and large blocks of load switching can cause islanding erroneous detection. Therefore, the traditional passive protections do not offer effective protection against unintentional islanding in generation.

This paper proposes a passive methodology for islanding detection based on mathematical morphology. The technique differentiates the frequency of oscillations caused by short circuits and load switching from those caused by islanding. The method used was originally proposed to extract the exponential decaying DC offset in short-circuit currents [1]. In this paper this methodology is used to eliminate high frequency oscillation.

Eliminating the frequency oscillations allows the threshold reduction enabling the detection of islanding with small power mismatch and in a much smaller time. Furthermore, the technique also reduces the amount of wrong operations occurred due others disturbances.

To validate the proposed methodology simulations of load switching, short-circuits, and islanding have been done in the test system, IEEE 34 bus. This system was increased by a 3,125 MVA synchronous generator equipped with governors and voltage controls.

Over 100 tests were conducted and the methodology worked correctly in most analyzed cases. Finally, the method was compared with the protection function ANSI 81R, 81O 81U. The proposed method is significantly more reliable, robust and presents a not detection zone much smaller than the traditional protection functions and the erroneous detections are significantly reduced.

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II. ISLANDING DETECTION ALGORITHM

During synchronous DGs parallel operation to the main system, the machine frequency is given by the differential equation which is known as the swing equation of the synchronous machine. When a disturbance occurs in the distribution systems, the machine tends to oscillate at its natural damped frequency.

During an islanding, the power flowing from or to the grid is interrupted. In this condition the machine does not show oscillations but behaves as an exponential function until the governors and voltage begins to act on the generation system. The action of the governor may bring the frequency back to its nominal value making a slow oscillation. In short circuits and large loads switching without islanding, the generation systems exhibit oscillatory behavior at higher frequencies than those presented in cases of islanding.

In the next section is presented a methodology based on Mathematical Morphology to eliminate the oscillations.

A. Mathematical Morphology

Mathematical Morphology was developed mainly for use in image processing. Among other factors, the simplicity of the Mathematical Morphology (MM) operators facilitated the application in other fields. In electrical systems protection can be highlighted the following applications [1]: Phasor Measurement, Protection of Transmission Lines, Transformer Protection, Bus Protection, Ultra-High-Speed Protection, Fault Location on Transmission Lines.

Differently of Fourier transform and Wavelet transform, MM is related to the shape of a signal waveform in time domain instead of the frequency domain.

The MM aims to extract relevant structures of a data set. The extraction is done by the operation of the data with a predefined set called Structuring Element (SE), where the SE shape is predefined considering the previous knowledge of the signal shape. There are two base operations in Mathematical Morphology, Dilation (1) and Erosion (2) which are defined as follows [3]

$$X \oplus G(x) = \max_{y \in D_G} [X(x-y) + G(y)], \forall x \in D_X \quad (1)$$

$$X \ominus G(x) = \max_{y \in D_G} [X(x+y) - G(y)], \forall x \in D_X \quad (2)$$

Where, X denote a signal, G denote an SE, D_X and D_G are the domain of X and G, respectively.

Two other operators can be defined in function of Dilation and Erosion, they are Opening (3) and Closing (4).

$$X \circ G = (X \ominus G) \oplus G \quad (3)$$

$$X \bullet G = (X \oplus G) \ominus G \quad (4)$$

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he Morphological Transform (MT) given by (5) has been used to remove the exponential decaying DC offset of short circuit transient currents [1].

$$H = (X \circ G \bullet G + X \bullet G \circ G) / 2 \quad (5)$$

The transform (5) is able to eliminate all details of the waveform with width shorter than the length of G. To remove frequency oscillations, G should be flat with at least one cycle of the lowest oscillation frequency that would be removed. In this paper the length of G is 0.1 s, and all elements are 0.01.

The Fig. 1 presents a flowchart of the proposed islanding detection algorithm. The oscillations of the frequency deviation are eliminated by the MM transform present in (5). If the frequency deviation is larger than Th1, 0.5 Hz, the algorithm send a signal to disconnect the DG. Otherwise the de frequency deviation is compared with Th2. If the frequency deviation is larger than Th2, 0.04 Hz, a counter "m" will increase at each new sample and when it reaches Th3, 1024 (8 cycles of 60 Hz), a signal is sent to disconnect the DG.

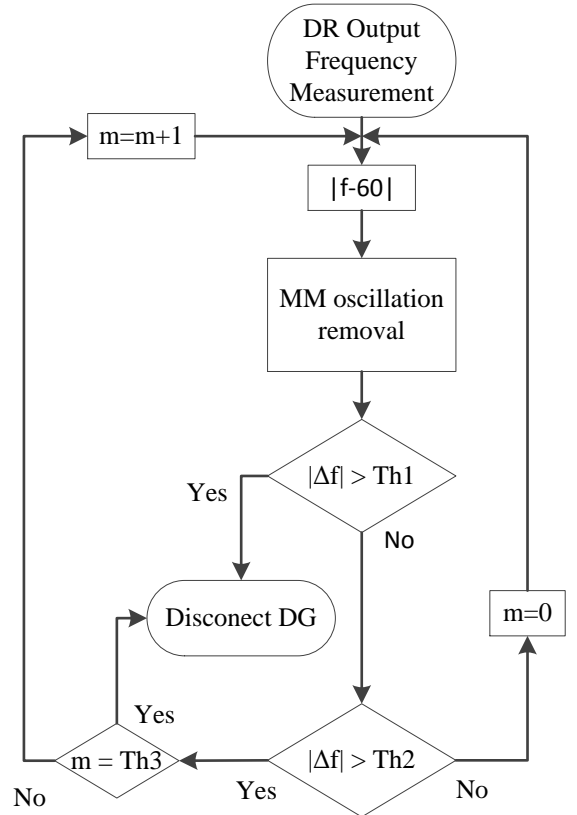


Fig. 1- Proposed island detection algorithm

In the Fig. 2 the performance of the proposed anti-islanding algorithm is presented. The Fig. 2-A shows the Frequency Deviation and the Filtered Frequency Deviation. In zero seconds a single phase short circuit happens and the frequency oscillates until the islanding at 0.35s. In the Fig. 2-B it is presented the module of the Filtered Frequency Deviation and

the thresholds given by Th1 and Th2. The Fig. 2-C shows the trip signal that the algorithm sends after the frequency pass through Th2 and elapses the timing given by Th3.

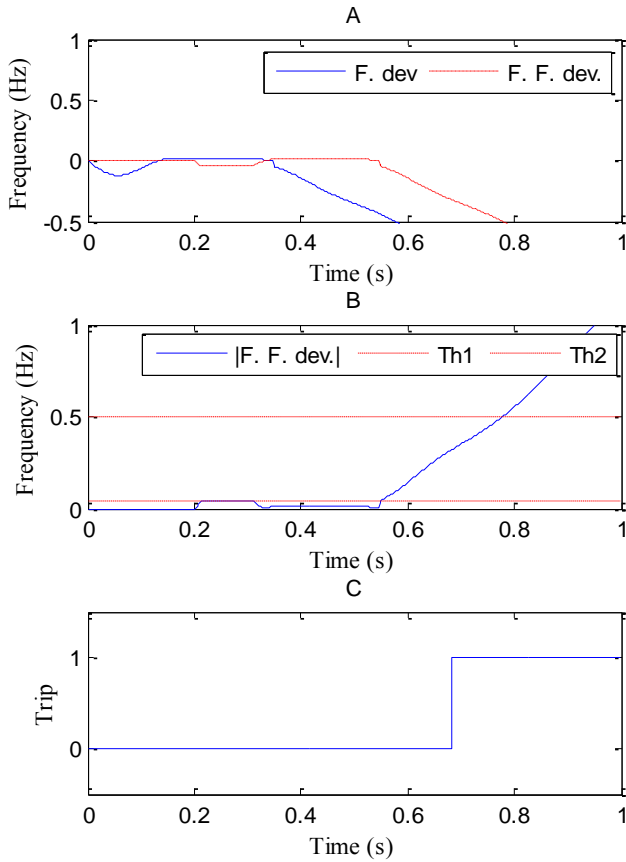


Fig. 2- Performance of the proposed island detection algorithm under a short-circuit followed by an islanding.

III. SIMULATION AND RESULTS

To evaluate the performance of the proposed methodology are tested in the IEEE 34 bus distribution test system. A distributed generator was connected to bus 854 through the transformer presented in Table 2. The distributed generator, presented in Table 3, within the voltage and frequency regulators are given in [4]. A load, 0.2 MW with power factor 0.92 inductive, is connected directly to the DG bus.

The proposed method is compared with two of the most used scheme, that is, the Rate of Change of Frequency (ROCOF, 81R) and the over/under frequency relays (81O/81U) the method was adjusted for four typical settings, which are presented in Table 1.

	81R	81O/81U
df/dt (Hz/s)	0.500	
Frequency		60.5/59.7
Delay (s)	0.150	0.150
Voltage restriction (p.u)	-	

Parameter	Value
N° of Receiving Bus	854
Three Phase Transformer	
Rated Power	3.0 MV A
Nominal Frequency	60 Hz
Rated Voltage	24.9/2.4 kV
Connection	D/yn
Vector Group	Phase Shift 1 ×30deg
Positive sequence reactance (x1)	0.059371 p.u.
Positive sequence resistance (r1)	0.008667 p.u.
Zero sequence short circuit voltage - Absolute (uk0_)	6.00%
Zero sequence short circuit voltage - Resistive (ukr0)	0.87%

Parameter	Value	Parameter	Value
Reference Machine	Not Flag	Direct axis reactance (Xd)	1.56 p.u.
Mode of Local Voltage Controller	Voltage	Quadrature axis reactance (Xq)	1.06 p.u.
Dispatch - Voltage	1.0 p.u.	Direct axis transient reactance (Xd')	0.26 p.u.
Nominal Apparent Power	3.125 MV A	Direct axis subtransient reactance (Xd'')	0.15 p.u.
Nominal Voltage	2.4 kV	Quadrature axis subtransient reactance (Xq'')	0.15 p.u.
Power Factor	0.8	Direct axis short-circuit transient time-constant (Td')	3.7 s
Connection	Yn	Direct axis short-circuit subtransient time-constant (Td'')	0.05 s
Inertia Time Constant (rated to Sgn) H	1.071 s	Quadrature axis short-circuit subtransient time-constant (Tq'')	0.05 s
x1	0.088 p.u.	Main flux saturation -Sg10	0.17 p.u.
Rotor Type	Salient pole	Main flux saturation -Sg12	0.60p.u.

The IEEE 34 bus distribution system was used during the tests and two load conditions were considered, 100% and 50%. In the first case, the loads are the same as described in the test system. In the last, all system loads where reduced to half. Table 4 present respectively, the opened line, the load condition, the power generated by the DG, the active and

reactive power interrupted by the switching, and the trip time for islanding occurrences.

It is possible to see that the proposed methodology has the islanding detection time higher than 81R and 81O/81U, however it is able to detect the islanding where the others are not.

Table 5 presents the performance of the proposed method during a non-islanding load switching. The amount of active and reactive power witch are switched off are expressed by P_{OP} and Q_{OP} , respectively. In this test all methodologies showed a good performance.

Table 6 present the performance of the methods during a short circuit that remains in the system for 350ms. After this

time the fault is cleared by circuit breakers operation causing the DG islanding. None of the methodologies identified islanding during the short circuit. However the 81R failed once and 81O/81U failed three times in islanding detection. The times presented in Table 6 corresponds to the time after the occurrence of islanding, in other words is not include the short-circuit duration.

Others temporary short circuits are tested and the methodologies result is present in the Table 7. In these cases the short circuit disappears spontaneously without causing islanding. All protection functions worked well in these cases, showing that the settings are not overly sensitive.

TABLE 4
PERFORMANCE OF ISLANDING DETECTION METHODS DURING ISLANDING EVENTS

<i>System conditions</i>					<i>Islanding Detection Time (s)</i>		
O. Lines	Load	P_G (MW)	P_{OP} (MW)	Q_{OP} (MVar)	Proposed	81R	81O / 81U
800 - 802	100%	2.5	-0.38	-0.11	0.235	0.150	0.185
830 - 854	100%	2.5	-0.75	-0.18	0.228	0.150	0.179
800 - 802	50%	2.5	-1.32	-0.67	0.235	0.150	0.185
830 - 854	50%	2.5	-1.61	-0.71	0.228	0.150	0.179
800 - 802	100%	1.0	1.12	0.13	0.246	0.150	0.172
830 - 854	100%	1.0	0.72	0.04	0.280	0.150	0.187
800 - 802	50%	1.0	0.05	-0.31	0.355	I. not det.	I. not det.
830 - 854	50%	1.0	-0.13	-0.49	0.396	I. not det.	I. not det.

TABLE 5
PERFORMANCE OF ISLANDING DETECTION METHODS DURING LOAD SWITCHING

<i>System conditions</i>					<i>Islanding Detection Time (s)</i>		
O. Line	Load	P_G (MW)	P_{OP} (MW)	Q_{OP} (MVar)	Proposed	81R	81O / 81U
854 - 852	100%	2.5	1.511	0.107	I. not det.	I. not det.	I. not det.
834 - 842	100%	2.5	0.565	-0.376	I. not det.	I. not det.	I. not det.
854 - 852	50%	2.5	0.754	-0.381	I. not det.	I. not det.	I. not det.
834 - 842	50%	2.5	0.285	-0.593	I. not det.	I. not det.	I. not det.
854 - 852	100%	1.0	1.507	0.112	I. not det.	I. not det.	I. not det.
834 - 842	100%	1.0	0.563	-0.374	I. not det.	I. not det.	I. not det.
854 - 852	50%	1.0	0.75	-0.375	I. not det.	I. not det.	I. not det.
834 - 842	50%	1.0	0.284	-0.558	I. not det.	I. not det.	I. not det.

TABLE 6
PERFORMANCE OF ISLANDING DETECTION METHODS DURING SINGLE PHASE SHORT-CIRCUITS, REMAINING FOR 350MS, AND FOLLOWED BY ISLANDING

<i>System conditions</i>					<i>Islanding Detection Time (s)</i>		
S.C..Bus	O. Line	Z _{fault} (Ω)	Load	P _G (MW)	Proposed	81R	81O / 81U
802	802 - 806	0	100%	2.5	0.333	0.150	0.273
802	802 - 806	60	100%	2.5	0.336	0.150	0.307
816	816 - 824	0	100%	2.5	0.360	0.189	0.395
816	816 - 824	60	100%	2.5	0.342	0.150	0.402
830	830 - 854	0	100%	2.5	0.412	0.208	0.454
830	830 - 854	60	100%	2.5	0.355	0.150	I. not det.
802	802 - 806	0	50%	2.5	0.334	0.401	I. not det.
802	802 - 806	60	50%	2.5	0.334	I. not det.	I. not det.
816	816 - 824	0	50%	2.5	0.257	0.490	0.207
816	816 - 824	60	50%	2.5	0.287	0.540	0.238
830	830 - 854	0	50%	2.5	0.251	0.490	0.201
830	830 - 854	60	50%	2.5	0.268	0.527	0.218
802	802 - 806	0	100%	1.0	0.229	0.128	0.162
802	802 - 806	60	100%	1.0	0.227	0.150	0.161
816	816 - 824	0	100%	1.0	0.228	0.150	0.160
816	816 - 824	60	100%	1.0	0.230	0.150	0.163
830	830 - 854	0	100%	1.0	0.229	0.150	0.161
830	830 - 854	60	100%	1.0	0.232	0.150	0.164
802	802 - 806	0	50%	1.0	0.301	0.123	0.197
802	802 - 806	60	50%	1.0	0.298	0.150	0.191
816	816 - 824	0	50%	1.0	0.333	0.150	0.211
816	816 - 824	60	50%	1.0	0.333	0.150	0.212
830	830 - 854	0	50%	1.0	0.333	0.150	0.226
830	830 - 854	60	50%	1.0	0.333	0.150	0.230

I. CONCLUSION

In this paper an island detection algorithm based on mathematical morphology was proposed. The algorithm aims to attenuate the high frequency oscillation and extract the constant part of the generator frequency deviation. The oscillatory behavior is characteristic of non-islanding events, while low frequency oscillations are characteristics of islanding events. Attenuating these high frequency oscillation allows the algorithm to distinguish frequency deviations

caused by short circuits, load switching or other events from those caused by islandings.

The proposed methodology was compared with traditional islanding protection scheme. The results show that the MM requires more time to identify an islanding condition. However, the algorithm proved to be more efficient to detect islanding since it is more tolerant to small power mismatch than the two others.

TABLE 7
PERFORMANCE OF ISLANDING DETECTION METHODS DURING TEMPORARY SINGLE PHASE SHORT CIRCUIT, 350MS

System conditions				Islanding Detection Time (s)		
S.C..Bus	Zfault	Load	P _G (MW)	Proposed	81R	81O / 81U
802	0	100%	2.5	I. not det.	I. not det.	I. not det.
802	60	100%	2.5	I. not det.	I. not det.	I. not det.
830	0	100%	2.5	I. not det.	I. not det.	I. not det.
830	60	100%	2.5	I. not det.	I. not det.	I. not det.
852	0	100%	2.5	I. not det.	I. not det.	I. not det.
852	60	100%	2.5	I. not det.	I. not det.	I. not det.
842	0	100%	2.5	I. not det.	I. not det.	I. not det.
842	60	100%	2.5	I. not det.	I. not det.	I. not det.
802	0	50%	1.0	I. not det.	I. not det.	I. not det.
802	60	50%	1.0	I. not det.	I. not det.	I. not det.
830	0	50%	1.0	I. not det.	I. not det.	I. not det.
830	60	50%	1.0	I. not det.	I. not det.	I. not det.
852	0	50%	1.0	I. not det.	I. not det.	I. not det.
852	60	50%	1.0	I. not det.	I. not det.	I. not det.
842	0	50%	1.0	I. not det.	I. not det.	I. not det.
842	60	50%	1.0	I. not det.	I. not det.	I. not det.
802	0	100%	2.5	I. not det.	I. not det.	I. not det.
802	60	100%	2.5	I. not det.	I. not det.	I. not det.
830	0	100%	2.5	I. not det.	I. not det.	I. not det.
830	60	100%	2.5	I. not det.	I. not det.	I. not det.
852	0	100%	2.5	I. not det.	I. not det.	I. not det.
852	60	100%	2.5	I. not det.	I. not det.	I. not det.
842	0	100%	2.5	I. not det.	I. not det.	I. not det.
842	60	100%	2.5	I. not det.	I. not det.	I. not det.
802	0	50%	1.0	I. not det.	I. not det.	I. not det.
802	60	50%	1.0	I. not det.	I. not det.	I. not det.
830	0	50%	1.0	I. not det.	I. not det.	I. not det.
830	60	50%	1.0	I. not det.	I. not det.	I. not det.
852	0	50%	1.0	I. not det.	I. not det.	I. not det.
852	60	50%	1.0	I. not det.	I. not det.	I. not det.
842	0	50%	1.0	I. not det.	I. not det.	I. not det.
842	60	50%	1.0	I. not det.	I. not det.	I. not det.

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