

# Internal Converter- and DC-Fault Handling for a Single Point Grounded Bipolar MMC-HVDC System

S. Wenig, M. Goertz, W. Schulze, S. Beckler, M. Kahl, J. Christian, M. Suriyah, T. Leibfried

**Abstract**—In order to address challenges caused by an increasing need for energy transmission, embedded bipolar HVDC links utilizing Modular Multilevel Converter (MMC) technology present a preferred solution as several operational and dynamic advantages compared to conventional ac grid enforcement are provided. In this paper, an approach to quickly detect and handle internal as well as dc-side faults in a full-bridge bipolar MMC-HVDC link is presented. Due to non-technical reasons and environmental constraints, the system is comprised of mixed overheadline-cable (OHL-cable) transmission and single point solid grounding with dedicated metallic return (MR). To validate and evaluate the proposed concept, effects of modified transmission system design as well as transient voltage and current stresses, detailed EMTP simulations are performed.

**Keywords**—active fault clearing, bipolar MMC-HVDC, control and protection, dc fault, full-bridge, overheadline-cable transmission;

## I. INTRODUCTION

TECHNOLOGICAL progress in power electronics and controls led to advanced voltage source converter (VSC) HVDC technology [1]. In particular, the commercial introduction of state of the art Modular Multilevel Converters (MMC) triggered numerous projects and research to connect remote offshore wind power resources [2]. Today, increasingly powerful designs additionally provide promising means to transmit renewable energy from coastal locations to the main load centres within existing ac grids.

Especially in Europe, the ongoing energy system transition is significantly changing power generation patterns in the upcoming years. Therefore, bulk power embedded HVDC links are proposed by involved authorities. To avoid high transmission capacity outages in case of contingencies, bipolar systems with dedicated metallic return (MR) and full-bridge (FB) submodules to extend operational flexibility have been recently approved or are discussed for upcoming projects. Furthermore, due to a lack of social acceptance for visible transmission system equipment, for some countries cable solutions are prioritized by law. However, local geographical constraints might still lead to a significant share of scattered

overheadline (OHL) segments. Triggered by these circumstances, this work investigates occurring fault transients in a 525 kV single point grounded bipolar FB-MMC scheme with mixed OHL-cable transmission path. In contrast to previous research [3], [4] and extended to [5], FB submodules are actively controlled during dc-side contingencies. This enables a continuing STATCOM functionality, as submodules are only blocked in case of internal converter faults. To differentiate between fault locations, a fast detection and differentiation methodology based on initial considerations given in [6] is presented.

This paper is organized as follows. Section II introduces basics of bipolar MMC-HVDC and highlights suitable fault clearing possibilities with FB-MMC technology. Section III introduces a detection concept, which allows a reliable and fast differentiation between different system faults. Section IV introduces the investigated scenario and technological specification. Section V presents obtained detailed results for two different fault scenarios as well as some general evaluation and further research opportunities. Section VI concludes the work.

## II. BIPOLAR MMC-HVDC

A bipolar MMC-HVDC terminal ( $T_x$ ), where  $x$  is an index numbered consecutively according to the system expansion, consists of a series connected upper and lower converter ( $C_{xp}$ ,  $C_{xn}$ ). At the converter dc clamp contact point, called terminal midpoint, either a dedicated MR path or a solid grounding electrode are present. On the ac-side, each converter is connected with a wye-delta transformer to the grid.

### A. Control Basics

To derive the basic control concept, the upper converter equivalent circuit of a non-grounded terminal T1 shown in Fig.1 is analysed for a single phase. This leads to, neglecting resistive components:

$$u_{ac,N0}^{C1p} + u_{ac,1N}^{C1p} + u_{p,1}^{C1p} + i_{p,1}^{C1p} \cdot L_{arm} - u_{dc}^{C1p} - u_{dc,MR}^{T1} = 0 \quad (1)$$

$$u_{ac,N0}^{C1p} + u_{ac,1N}^{C1p} - u_{n,1}^{C1p} - i_{n,1}^{C1p} \cdot L_{arm} - u_{dc,MR}^{T1} = 0 \quad (2)$$

Equivalent to [7]–[9], a full decoupling of an alternating current (ac) and phasemodule current (phm) system can be executed. Therefore, we define

$$i_{ac,1}^{C1p} = i_{p,1}^{C1p} - i_{n,1}^{C1p} \quad (3)$$

---

This work is supported and funded by TransnetBW GmbH. S. Wenig, M. Goertz, W. Schulze, M. Suriyah and T. Leibfried are with Karlsruhe Institute of Technology (KIT), Institute of Electric Energy Systems and High Voltage Technology (IEH), Karlsruhe, BW 76131 Germany (e-mail of corresponding author: simon.wenig@kit.edu). S. Beckler, M. Kahl and J. Christian are with the TransnetBW TSO, Stuttgart, BW 70173 Germany (email: s.beckler@transnetbw.de).

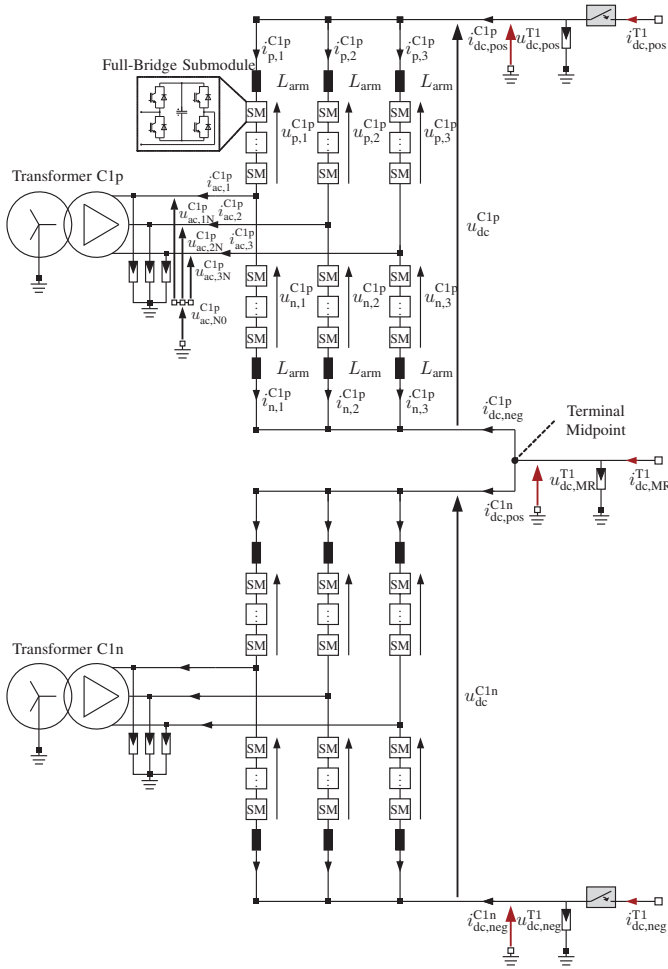


Fig. 1. Bipolar MMC-HVDC terminal three-phase equivalent circuit (terminal T1, non-grounded)

as well as

$$i_{\text{phm},1}^{\text{C1p}} = \frac{i_{\text{p},1}^{\text{C1p}} + i_{\text{n},1}^{\text{C1p}}}{2} \quad (4)$$

and perform  $[(1) \mp (2)] / 2$ . An independent control of dc- and ac-side quantities can be realized by adjusting sum and delta components of arm output voltages, which becomes apparent when inspecting

$$u_{\Sigma,1}^{\text{C1p}} = \frac{u_{\text{p},1}^{\text{C1p}} + u_{\text{n},1}^{\text{C1p}}}{2} = -i_{\text{phm},1}^{\text{C1p}} \cdot L_{\text{arm}} + \frac{u_{\text{dc}}^{\text{C1p}}}{2} \quad (5)$$

and

$$u_{\Delta,1}^{\text{C1p}} = \frac{u_{\text{n},1}^{\text{C1p}} - u_{\text{p},1}^{\text{C1p}}}{2} = i_{\text{ac},1}^{\text{C1p}} \cdot \frac{L_{\text{arm}}}{2} + u_{\text{ac},1\text{N}}^{\text{C1p}} + \text{Offset}. \quad (6)$$

The highlighted offset due to the chosen bipolar system configuration, as shown in (6), consists solely of dc components ( $u_{\text{ac},\text{N}0}^{\text{C1p}}$ ,  $u_{\text{dc}}^{\text{C1p}}/2$ ,  $u_{\text{dc},\text{MR}}^{\text{T1}}$ ) and is equal for all three phases. Therefore, it is neglectable as no zero-sequence component can propagate to the ac-side due to the chosen transformer setting.

### B. Converter Control and Energy Balancing

The introduced control concept outlined for a single phase in section II-A can be expanded to a full three phase scheme, see

[6], [9]. As a result, five degrees of freedom to regulate ac- and dc-side terminal as well as internal quantities are present for each converter within a bipolar terminal. Also for commercial applications, similar concepts seem to be utilized as indicated in [10]. Besides ac current control, which is realized by a conventional grid frequency rotating frame approach (set  $u_{\Delta,d/q}$  to regulate  $i_{\text{ac},d/q}$ ), dc-side power is modified in case of a current controlled station by adjusting the phasemodule zero sequence component (set  $u_{\Sigma,0}$  to adjust  $i_{\text{phm},0}$ ). Under steady state conditions, this current is equivalent to  $i_{\text{dc}}/3$ . Furthermore, in dc voltage control mode the terminal clamp voltage across submodule stacks and arm inductors can be quickly influenced (set  $u_{\Sigma,0}$  to adjust  $u_{\text{dc}}^{\text{C1p}}$ ).

In terms of energy balancing, especially compared to conventional VSC technology, short term power imbalance buffering (caused by different instantaneous power output setpoints at ac and dc clamps, e.g. rapid power ramp up/down, active fault ride through) between both sides is possible. Here, individual submodule capacitors offer a limited dynamic decoupling control reserve with respect to technical limitations. Nevertheless, due to the increasing system complexity, also internal imbalances between different phases (horizontal direction) or between upper and lower arms (vertical directions) can occur for MMC-HVDC during dynamic operating point adjustments or subsequent to fault ride through sequences. To rearrange this internal energy distribution, the remaining two controllable currents  $i_{\text{phm},\alpha/\beta}$  are impressed to balance the system in a horizontal (between the three phase-modules consisting of upper and lower arm) or in a vertical (between upper and lower arm) manner.

### C. Advanced Fault Handling with FB-MMC

In case of half-bridge submodules, immediate blocking subsequent to faults avoids high overcurrents in power electronic switches. Nevertheless, fault clearance times lay within a range of a few full ac grid cycles - as ac circuit breakers need to be opened to interrupt fault current propagation - excluding additional reclosure delays. While this has been suitable for typical monopolar systems with full cable transmission, the situation significantly changes for schemes with OHL segments. As fault likeliness is significantly higher and transmission capacities are hitting one Gigawatt, requirements for clearing and reclosure actions with minimized impact on the interconnected or even surrounding ac network gain increased attention.

Previous research in [11] has shown and briefly evaluated the full range of possible post-fault operation strategies of a monopolar FB-MMC scheme with mixed OHL-cable transmission. To reflect the outcome in terms of converter basic design requirements as well as transient phenomena, only dc fault current control and module blocking are considered as suitable clearing strategies in this work:

1) *post-fault current control*: Regardless if the chosen converter regulates dc-side current or voltage during normal operation, a current reduction is triggered by switching the dc current reference value to zero after a fault event has been detected. As modules are not blocked, the remaining controllability enables a continuing reactive power supply on the ac-side. If the converter has controlled the dc voltage prior to the

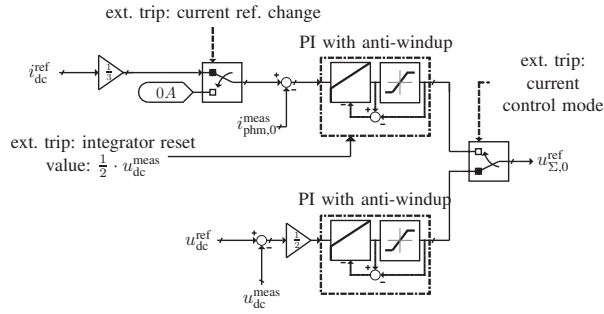


Fig. 2. DC-side control loops including post-fault current control switches

fault, half of the currently measured dc voltage at the clamps is initially set as integrator offset for the current control loop to obtain a smooth transition, see Fig. 2. Corresponding fault clearing transients strongly depend on the chosen controller parameters as well as on the controller output limits. These are influenced by the underlying transmission scenario, technical device limitations as well as detection delays.

2) *module blocking*: Even though active fault current reduction represents the most favourable choice in terms of operational aspects, blocking of FB submodules can not be avoided in some situations. Especially during low impedance internal faults, critical current limits are quickly reached as current rate of rise is significantly faster than a control response can be triggered. This is due to the absence of large inductances within the fault current loop. But, in contrast to HB solutions, turning off all IGBT devices and commutating the current into the anti-parallel diodes immediately result in a countervoltage quickly reducing module current to zero.

### III. EXTENDED FAULT DETECTION

Module stack overcurrent detection is a major criterion for MMC-HVDC systems to avoid severe damage in case of system contingencies. However, differentiated clearing strategies depending on the fault location are difficult to implement, as any maximum current threshold validations must strictly lead to immediate converter blocking actions. This work discusses an extension with a superimposed concept, which enables immediate classification of internal as well as different dc-side faults (positive and negative pole to ground, pole to pole) before individual arm overcurrent thresholds are hit. In consequence, active clearing possibilities during dc-side faults remain. A scheme of this multi-stage protection concept is shown in Fig. 3, individual parts are subsequently described.

#### A. Internal Fault Detection

The proposed method monitors currents flowing into and out of six converter-individual protection zones (pz) and triggers in case of an imbalance. In Fig. 4, all zones as well as related current measuring points are marked in grey boxes or are emphasized with arrows, respectively. Internal faults are detected if one of the conditions given in Table I is violated. The triggering threshold should be selected slightly higher than the worst case measurement uncertainty within one of the protection zones.

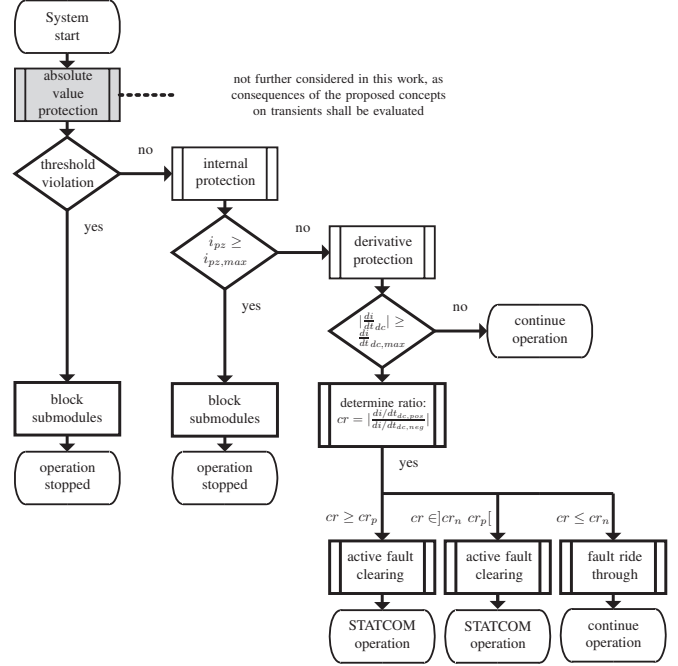


Fig. 3. Detection Flowchart: Example for an upper Converter  $C_{xp}$

#### B. DC Fault Detection

Current derivative based concepts represent a promising methodology to detect dc faults at an early stage, as incoming travelling waves cause steep transient slopes long before absolute values become critical. Therefore, the terminal dc currents at the positive and negative dc clamps, as marked in Fig. 1 ( $i_{dc,pos/neg}^{T1}$ ), are continuously observed and post-processed. Here, the initial trigger conditions equals:

$$\max \left( \left| \frac{di}{dt}_{dc,pos} \right|, \left| \frac{di}{dt}_{dc,neg} \right| \right) \geq \frac{di}{dt}_{dc,max} \quad (7)$$

Subsequently, a comparative fault-characterising ratio ( $cr$ ) is determined within a period of several hundred microseconds. Here, it is made use of the fact that measurable slopes differ during distinct fault scenarios. Depending on the obtained value, a clear differentiation between positive / negative pole to ground and pole to pole faults can be achieved. The suitability of this method has been initially shown in [6] with simplified transmission line and cable models.

TABLE I  
INTERNAL FAULT DETECTION

Protection Zone ID	Normal Operation Condition
C1p-phm1	$i_{p,1}^{C1p} - i_{n,1}^{C1p} - i_{ac,1}^{C1p} < i_{pz,crit}$
C1p-phm2	$i_{p,2}^{C1p} - i_{n,2}^{C1p} - i_{ac,2}^{C1p} < i_{pz,crit}$
C1p-phm3	$i_{p,3}^{C1p} - i_{n,3}^{C1p} - i_{ac,3}^{C1p} < i_{pz,crit}$
C1p-ac	$i_{ac,1}^{C1p} + i_{ac,2}^{C1p} + i_{ac,3}^{C1p} < i_{pz,crit}$
C1p-bbp	$-i_{p,1}^{C1p} - i_{n,1}^{C1p} - i_{p,3}^{C1p} + i_{dc,pos}^{C1p} < i_{pz,crit}$
C1p-bbn	$+i_{n,1}^{C1p} + i_{n,2}^{C1p} + i_{n,3}^{C1p} - i_{dc,neg}^{C1p} < i_{pz,crit}$

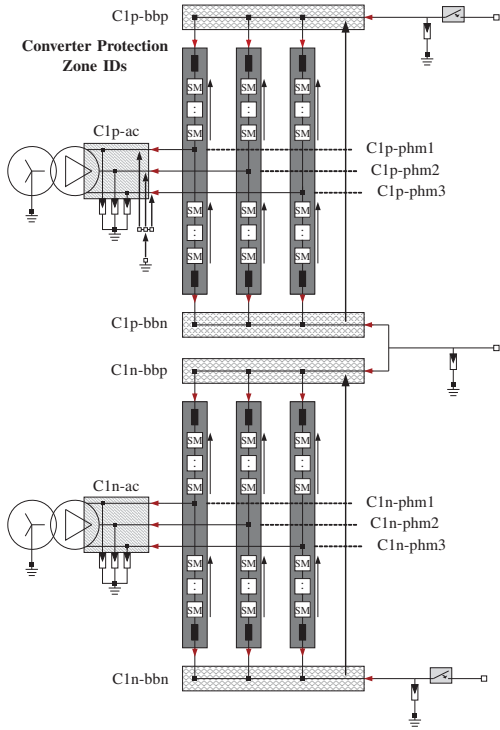


Fig. 4. Bipolar MMC internal protection zone overview (Terminal T1, non-grounded)

#### IV. SCENARIO

The investigated bipolar MMC-HVDC link is a single point solidly grounded bipolar system with a rated power of 1.05 GW per subsystem (upper and lower) and FB sub-modules. Terminal T2 acts as voltage regulating station during normal operation and transmits two Gigawatts to the dc current controlled Terminal T1. Results are obtained using the electromagnetic transient simulation PSCAD-EMTDC. This includes frequency dependent transmission line and cable models, overvoltage protection devices on the ac- as well as dc-side and transformers including saturation effects. The implemented submodule stacks, which are classified as Type 3 models according to [12], represent IGBTs and diodes as ideal switches with corresponding on- and off-resistance value, respectively. This is beneficial in terms of computational efficiency for initial EMT-type system level studies. Nevertheless, limitations regarding further modelling refinements at a later stage do exist [13]. A schematic overview, including faults that are discussed later on, is presented in Fig. 5.

#### V. SIMULATION RESULTS

To validate the proposed concept, faults with varying location, polarity, phase shift and resistance have been applied to the MMC-HVDC link. This section discusses - besides detailed transients for two selected cases - general performance and limitations of the introduced concepts for a 700 km long mixed OHL-cable system.

##### A. Busbar Fault Terminal 2 (converter hall bushing)

In Fig. 6, transient response of the bipolar link to a positive pole to ground fault at the busbar of MMC C2p at  $t = 0.61$  s

is shown. The fault resistance is  $1 \text{ m}\Omega$ . Terminal 2 detects the internal fault in protection zone C2p-bbp at  $t = 0.61012$  s. Consequently, MMC C2p is immediately blocked, which can be seen in quickly decreasing arm currents. Nevertheless, the directly connected dc cable is still discharging, which is obvious when looking at the rapidly overshooting dc current  $i_{\text{dc,pos}}^{\text{T2}}$ . The resulting travelling wave due to the rapid fault current increase propagates towards Terminal 1. Here, an external fault within the positive subsystem is detected at  $t = 0.61468$  s and leads to an active dc current reduction within the positive subsystem. In contrast to the blocked converter MMC C2p, ac-side power reduction and control-wise dc current interruption can be seen in the arm currents of MMC C1p. Due to the correct classification of a positive pole to ground fault at Terminal 1, the lower converter is not tripped and remains in normal operation mode. The dc current commutates into the metallic return, which causes a permanent midpoint voltage offset. Regarding transient cable insulation stresses, polarity reversals at a level of approximately 0.3 pu occur at MMC C1p and at both cable-OHL transitions.

##### B. Pole to Ground Fault Cable-OHL Transition 1 (DC Yard)

In Fig. 7, transient response of the bipolar link to a positive pole to ground fault at Transition 1 at  $t = 0.61$  s is shown. The fault resistance is  $1 \text{ m}\Omega$ . Terminal 1 and Terminal 2 detect the positive dc fault at  $t = 0.61196$  s and  $t = 0.61228$  s, respectively. According to the determined classification, both terminals reduce the dc current actively to zero. This includes a control mode transition to current control mode of MMC C2p. In the desired manner, the lower subsystem is again not tripped, remains in normal operation mode and is able to ride through the post-fault transients affecting metallic return and negative pole transmission line and cable. Regarding

TABLE II  
BIPOLAR SYSTEM SPECIFICATION

Main Parameters	Value
nominal dc voltage (pole to ground)	+/- 525 kV
nominal ac voltages (grid / conv.)	400 kV / 320 kV
ac network X/R ratio	10
line frequency	50 Hz
submodules per arm	270
submodule capacitor	8.5 mF
arm sum capacitor voltage ref. value	675 kV
grounding resistance	0.7 $\Omega$
<b>Varistor Ratings</b>	<b>Value</b>
dc varistor MCOV	535 kV
dc midpoint MCOV	90 kV
ac varistor MCOV	555 kV
varistor protective level	1.8 pu
<b>Controller Parameters</b>	<b>Value</b>
dc-current P-gain	291
dc-current time constant	$2.34 \cdot 10^{-5}$ s
dc-voltage P-gain	0
dc-voltage time constant	$18.25 \cdot 10^{-3}$ s
ac-current P-gain	23.8
ac-current time constant	$0.376 \cdot 10^{-3}$ s
<b>Control and Protection</b>	<b>Value</b>
control system delay	40 $\mu$ s
protection zone fault detection delay	60 $\mu$ s
protection zone current threshold	0.04 kA
derivative dc current fault detection delay	200 $\mu$ s
derivative dc current threshold	0.5 kA/ms
comparator ratio $cr_p, cr_n$	$\frac{3}{2}$ and $\frac{2}{3}$

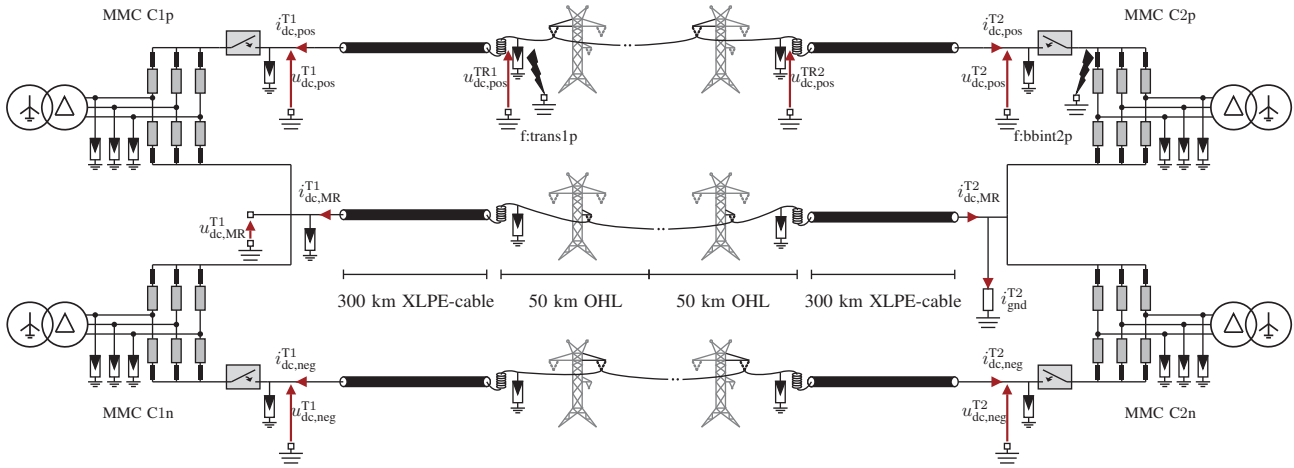


Fig. 5. Bipolar schematic overview (single point solidly grounded with dedicated metallic return, mixed OHL-cable transmission with a length of 700 km)

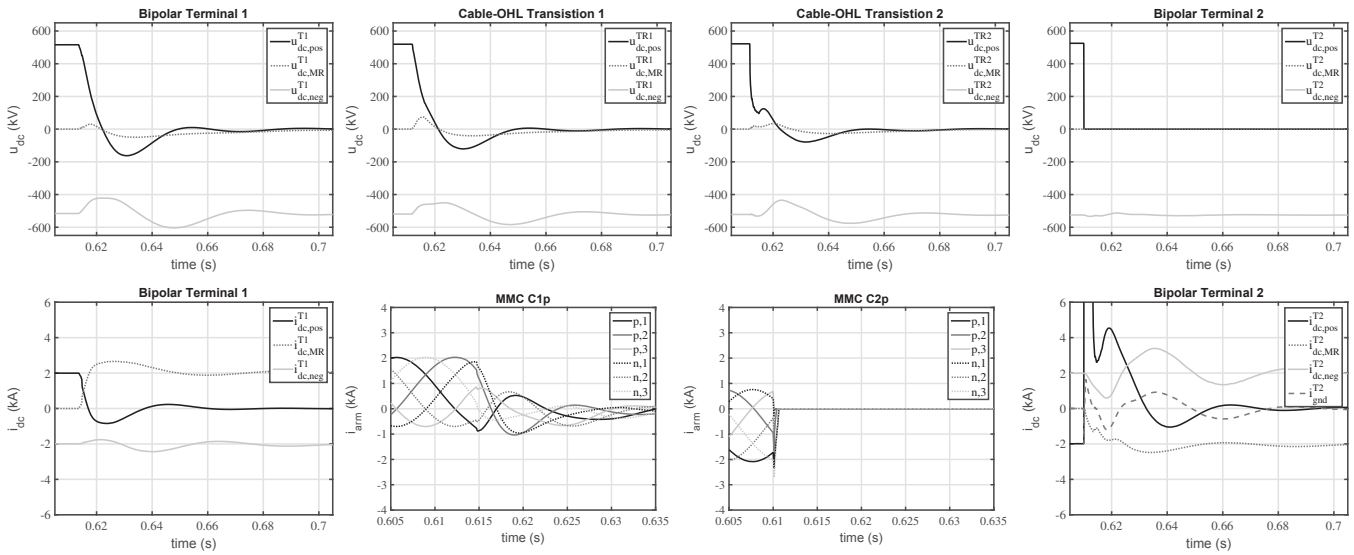


Fig. 6. Transient system response to a busbar fault at MMC C2p (converter hall bushing, internal fault Terminal 2, f:bbint2p): transient terminal voltages at converters and cable-OHL transitions (top plots, from left to right, Terminal 1, Transition 1, Transition 2, Terminal 2), transient terminal dc currents and converter arm currents (bottom plots, from left to right, Terminal 1, MMC C1p, MMC C2p, Terminal 2).

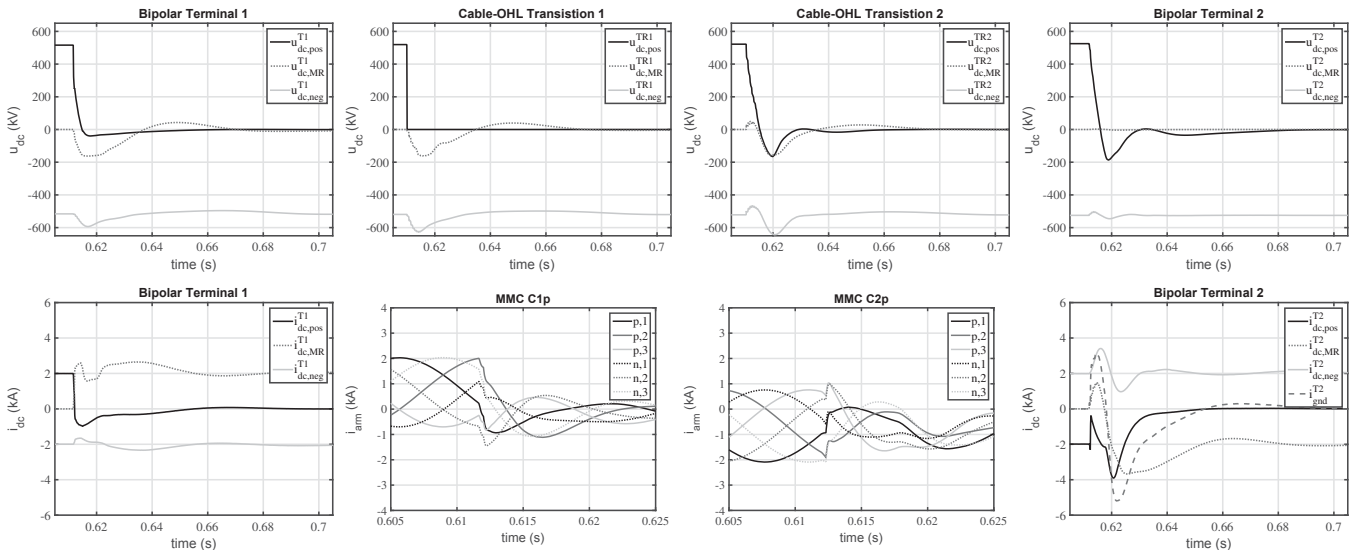


Fig. 7. Transient system response to a fault at cable-OHL Transition 1 (transition yard, external fault, f:trans1p): transient terminal voltages at converters and cable-OHL transitions (top plots, from left to right, Terminal 1, Transition 1, Transition 2, Terminal 2), transient terminal dc currents and converter arm currents (bottom plots, from left to right, Terminal 1, MMC C1p, MMC C2p, Terminal 2).

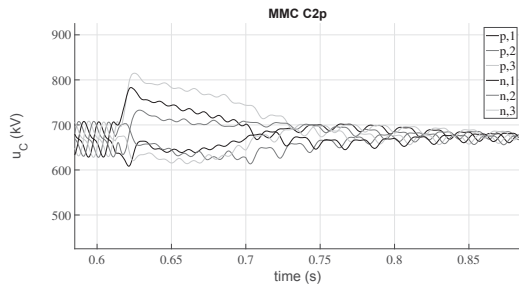


Fig. 8. Impact of active clearing strategies on submodule capacitor sum voltages of MMC C2p, fault  $f$ :trans1p,  $1\text{ m}\Omega$ , converter clears fault current actively, continuing reactive power supply subsequent to the fault

transient cable insulation stresses, a polarity reversal with approximately 0.35 pu occurs at MMC C2p and at OHL-cable Transition 2.

### C. Generalized Evaluation

In total, a broad range of fault cases has been simulated to obtain a robust assessment of effects, advantages but also limitations of the proposed detection and fault clearing concepts. The following list provides an overview of relevant characteristics and improvement potential beyond the main scope of this work:

- Submodule voltages change during active fault clearing in contrast to module blocking, as highlighted in Fig. 8. As significant deviations can be noticed, further investigations need to reflect energy balancing dynamics, modified energy storage requirements and module overvoltage protection in case of mixed transmission lines with a significant share of cable segments.
- Common internal converter faults (tested up to  $100\ \Omega$  and for different ac phase positions) are properly identified and lead to converter blocking.
- During symmetrical bipolar link operation, faults in zone Cxp-bbn, Cxn-bbp or on the dedicated metallic return have different characteristics and need to be investigated independently, as they cannot be detected with conventional methods.
- DC-side faults are appropriately identified on the OHL segments. Fault resistances range from  $1\text{ m}\Omega$  to  $100\ \Omega$ .
- Current derivatives at Terminal 1 in case of dc faults located near Terminal 2 are below the chosen threshold (medium to high fault resistances, large effective inductance towards the ground electrode), but also uncritical in terms of transient stresses. Lowering the  $di/dt$  threshold might lead to unwanted tripping in normal operation. From a technical perspective, achievable current derivative sample times and related accuracy limitations must also be considered. As a consequence, adapted (slowly-triggered) additional dc over- / undervoltage criteria should be considered in future studies.
- Ongoing investigations may tackle the following two aspects. First, as recently discussed in [14], modelling refinements regarding ac-side grid connection are mandatory to understand better resonances and ACDC interaction phenomena during normal operation and subsequent

to faults. Additionally, integration and coordination of derivative, internal as well as absolute value protection (neglected in this paper) need to be carried out. Similar to considerations for dc grids in [15], a backup protection extension for bipolar systems is essential.

## VI. CONCLUSION

This work introduces an extended fault detection and classification concept for bipolar MMC-HVDC schemes. Besides this, conventional module blocking is avoided in case of dc-side contingencies as active fault clearance methods to reduce the dc-side current are utilized to comply with tightened requirements on dynamic performance and system reliability. This is especially useful due to novel transmission corridor designs with mixed OHL-cable segments, which significantly increase fault likeliness. Detailed transient studies indicate that the proposed approach is suitable for a wide range of contingencies.

## REFERENCES

- [1] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. IEEE Power Tech Conf., Bologna*, vol. 3, June 2003, pp. 1–6.
- [2] L. Cai, U. Karaagac, and J. Mahseredjian, "Simulation of startup sequence of an offshore wind farm with MMC-HVDC grid connection," *IEEE Trans. on Power Del.*, in press.
- [3] Y. Xue and Z. Xu, "On the bipolar MMC-HVDC topology suitable for bulk power overhead line transmission: Configuration, control, and DC fault analysis," *IEEE Trans. Power Del.*, vol. 29, no. 6, pp. 2420–2429, Dec. 2014.
- [4] J. Chen, B. Li, B. Dong, Q. Ren, and X. Qi, "Simulation and analysis of fault characteristics of the MMC-HVDC system under bipolar connection mode," in *Proc. IEEE PES APPEEC*, Oct. 2016, pp. 2534–2538.
- [5] S. Beckler, J. Lehner, A. Arnold, A. K. Kamga, K. Frey, and K. Rudion, "DC fault currents for FB-MMC HVDC with bipolar configuration," in *Proc. Int. ETG Congress, Bonn, Germany*, Nov. 2015, pp. 1–6.
- [6] S. Wenig, M. Goertz, M. Suriyah, and T. Leibfried, "Active dc fault management of a bipolar full-bridge mmc-hvdc scheme with metallic return," in *Proc. IEEE Int. Energy Conf. (ENERGYCON), Leuven, Belgium*, Apr. 2016, pp. 1–6.
- [7] P. Munch, D. Gorges, M. Izak, and S. Liu, "Integrated current control, energy control and energy balancing of modular multilevel converters," in *Proc. 36th Ann. Conf. IEEE Industrial Electronics Society, Phoenix*, Nov. 2010, pp. 150–155.
- [8] J. Kolb, F. Kammerer, M. Gommeringer, and M. Braun, "Cascaded control system of the modular multilevel converter for feeding variable-speed drives," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 349–357, Jan. 2015.
- [9] S. Wenig, F. Rojas, K. Schoenleber, M. Suriyah, and T. Leibfried, "Simulation framework for DC grid control and ACDC interaction studies based on modular multilevel converters," *IEEE Trans. Power Del.*, vol. 31, no. 2, pp. 780–788, Apr. 2016.
- [10] M. Dommaschk, J. Dorn, I. Euler, J. Lang, Q. Tu, and K. Würflinger, "Control of a modular converter with distributed energy storage devices," Patent, Jun., 14, 2011, US Patent 7,960,871.
- [11] S. Wenig, M. Goertz, J. Prieto, M. Suriyah, and T. Leibfried, "Effects of DC fault clearance methods on converters in a full-bridge monopolar MMC-HVDC link," in *Proc. IEEE Innovative Smart Grid Tech. - Asia, Melbourne, Australia*, Nov. 2016, pp. 850–855.
- [12] R. Wachal *et al.*, "Guide for the development of models for HVDC converters in a HVDC grid," Cigré TB604 (WG B4.57), Paris, Tech. Rep., Dec. 2014.
- [13] A. Beddard, M. Barnes, and R. Preece, "Comparison of detailed modeling techniques for MMC employed on VSC-HVDC schemes," *IEEE Trans. Power Del.*, vol. 30, no. 2, pp. 579–589, Apr. 2015.
- [14] H. Saad, Y. Fillion, S. Deschanvres, Y. Vernay, and S. Dennetiere, "On resonances and harmonics in HVDC-MMC station connected to AC grid," *IEEE Trans. Power Del.*, in press.
- [15] W. Leterme, S. P. Azad, and D. V. Hertem, "A local backup protection algorithm for HVDC grids," *IEEE Trans. Power Del.*, vol. 31, no. 4, pp. 1767–1775, Aug 2016.