Accurate and High Speed Electromagnetic Transient Modeling of Two-Port Sub-Modules based MMC-HVDC Converters

Jianzhong Xu, A. M. Gole, Shengtao Fan and Chengyong Zhao

***Abstract*—Various two-port sub-modules (SMs) are emerging as candidate topologies for Modular Multi-level Converters (MMC) used for HVDC transmission. This paper presents fast and accurate electromagnetic transient (EMT) models for cascaded two-port SMs based MMC-HVDC converters. The approach uses the Schur's Complement technique to eliminate internal nodes of all the two-port SMs to reduce the nodes in admittance matrix, so that only four terminal nodes are included in the EMT admittance matrix for each MMC arm. While doing this reduction, as in previously developed approaches for the single-port half-bridge SMs based MMCs, all internal information such as individual SM capacitor voltages is preserved and can be output by the program if needed. This increases the bookkeeping effort, but the overall reduction in matrix size more than compensates for any resulting time-penalty. Approximately two orders of magnitude speedup over a straightforward implementation in an EMT program is achieved.**

***Keywords*: Modular multilevel converter (MMC), Schur's Complement, electromagnetic transient (EMT), two-port sub-modules (SMs), high speed modeling.**

I. Introduction

ELECTROMAGNETIC transient (EMT) simulation of MMC inverters on EMT programs is a challenge, due to their extremely large component count and high number of nodes in the topology. To address this issue, a popular approach in EMT algorithms which has been successfully used for one-port sub-modules (SMs) (e.g., half-bridge or full-bridge SMs) [1]-[5] to represent the arm as a Thevenin equivalent source and resistance. This greatly reduces the node count and significantly speeds up the program, albeit at the expense of more bookkeeping effort. The equivalent algorithms take advantage of the fact that the same bridge arm current flows through all the series-connected SMs, entering at the positive terminal and exiting out of the negative terminal of the single-port, and thus the equivalent circuit of the cascaded SMs can be simply obtained by adding the individual SM equivalent circuits [1].

Recently, novel MMC topologies are emerging [6]-[10], which are aiming to add specific functions such as the dc fault current clearance and capacitor voltage self-balance capability etc. Inevitably, they will include the two-port SMs based MMC topologies, a two-port example is shown in Fig. 1, which are structurally different from the half-bridge and full-bridge configurations. Unlike the one-port systems analyzed earlier, one cannot rely on a common current between SMs that allows one to simply cascade individual Thevenin equivalents. Modeling these using detailed EMT simulation models becomes time-expensive, and so there is a need to develop high speed models without sacrificing accuracy for such devices.

This paper will present a generalized strategy for modeling various emerging MMC topologies for HVDC transmission, that are about two orders of magnitude faster than detailed models.

II. Two-port Submodule Topology

The series-parallel MMC converter is presented in detail in the literature [6] and [7], the basic SM topology is shown in Fig. 1, with two ports (P_A, P_B) and (N_A, N_B). The following identity is satisfied by the terminal currents: $I_{PA} + I_{PB} = I_{NA} + I_{NB}$ (note that the term "port" is used loosely in this paper for convenience, as a strict definition would require the current entering and leaving any port to be the same, e.g., $I_{PA} + I_{PB} = 0$, which is not the case here).

The interconnection of two SMs through a pair of SM ports enables series connectivity of the SM capacitors in two polarities and bypass as known from traditional MMC and parallel connectivity across several SMs, i.e. the capacitor voltages are self-balanced accordingly, see Fig. 2.

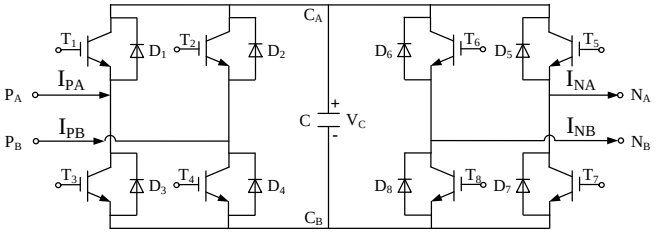

Fig. 1. A two-port MMC SM topology.

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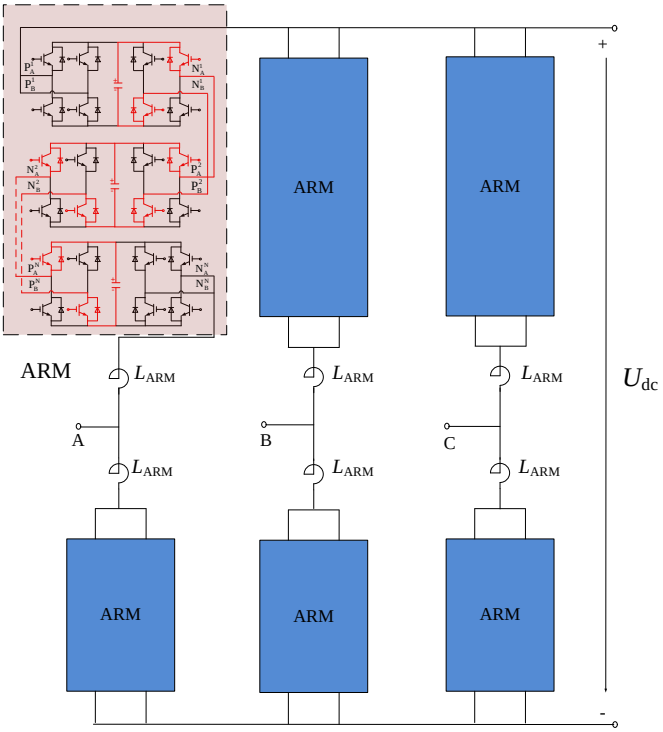


Fig. 2. Two-port SMs based MMC topology.

Although the number of distinct switches in Figs. 1 and 2 is increased compared to traditional half-bridge MMC, the circuit does not require more silicon. The reason is that in every SM state the two-port MMC can use two switches in parallel to carry the current that the traditional MMC would handle with a single switch. Consequently, each two-port MMC switch can have half of the current rating of a MMC switch. The switching logic (i.e. nine switching states for each SM) provided in [6] and [7] is used in this paper.

III. Proposed Approach

A. Recursive Solution Algorithm

The proposed algorithm in this paper includes several steps to obtain the equivalent circuit of the cascaded two-port SMs. First, the internal capacitor nodes within each SM are eliminated. Next, the first SM (call it Block 1) is combined with the next SM and internal nodes are once again eliminated in this new block, say Block 2. This block is then combined with the next, and again, internal nodes are eliminated and the new Block 3 now contains three SMs. The process ends when Block N, with N SMs is now the entire bridge arm leaving only four nodes per arm to be included in the external system's EMT solver. This is what results in the simulation efficiency as the representation of the arm in the main EMT simulation (PSCAD/EMTDC in this case) has a very small number of nodes.

Once the solution for the arm's external nodes is obtained, the internal nodes of Block N can be solved for. Once these are known, the internal node solution for Block N-1 is determined, which is required to calculate history terms for the next time step, and this continues in a recursive manner until Block 1 or the individual SM is solved for. This process is similar to that described in [11].

B. Nodes Elimination within Each SM

The companion circuit of the two-port SM in Fig. 1 is shown in Fig. 3, and is referred to as Block 1. It has 6 nodes, in which external nodes 1 to 4 are interface nodes and internal nodes 5 and 6 are the capacitor terminals. Assuming a remote ground, the Nodal Conductance Matrix of the circuit is shown in (1).

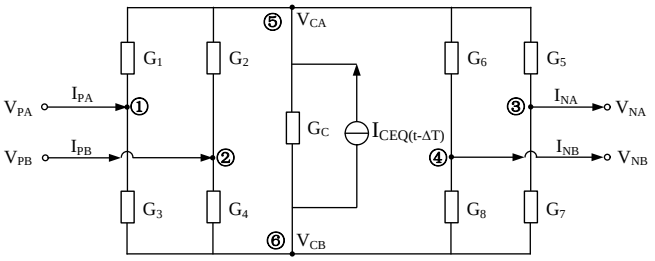


Fig. 3. Companion circuit of the two-port SM (Block 1).

$$\begin{bmatrix} G_1+G_3 & 0 & 0 & 0 & -G_1 & -G_3 \\ 0 & G_2+G_4 & 0 & 0 & -G_2 & -G_4 \\ 0 & 0 & G_5+G_7 & 0 & -G_5 & -G_7 \\ 0 & 0 & 0 & G_6+G_8 & -G_6 & -G_8 \\ -G_1 & -G_2 & -G_5 & -G_6 & G_1+G_2+G_5+G_6+G_C & -G_C \\ -G_3 & -G_4 & -G_7 & -G_8 & -G_C & G_3+G_4+G_7+G_8+G_C \end{bmatrix}$$

$$\begin{Bmatrix} V_{IF} \\ V_{IN} \end{Bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ \hline I_{CEQ}(t-\Delta T) \\ -I_{CEQ}(t-\Delta T) \end{bmatrix} + \begin{Bmatrix} I_{IF} \\ J_{IN} \end{Bmatrix} \begin{bmatrix} I_{PA} \\ I_{PB} \\ -I_{NA} \\ -I_{NB} \\ \hline 0 \\ 0 \end{bmatrix}$$

$$\begin{Bmatrix} V_{IF} \\ V_{IN} \end{Bmatrix} = \begin{bmatrix} V_{PA} \\ V_{PB} \\ V_{NA} \\ V_{NB} \\ \hline V_{CA} \\ V_{CB} \end{bmatrix}$$

or

$$YV=J+I \tag{1}$$

In (1), the two-value conductance G_i ($i \in \{1,2,...,8\}$) is used to represent the IGBT switch (i.e. the parallel connection of an IGBT and a diode) in the companion circuit. It is either the on state conductance G_{ON} or the off state conductance G_{OFF} of the IGBT switch, depending on the triggering signals, G_C is the Norton conductance of the capacitor. $V=[V_{PA}, V_{PB},\ldots,V_{CB}]^T$ are the node voltages. $I_{CEQ}(t-\Delta t)$ is the history Norton equivalent current and $J=[0, 0, 0, 0, I_{CEQ}(t-\Delta t), -I_{CEQ}(t-\Delta t)]^T$ is the history current vector. $I=[I_{PA}, I_{PB}, -I_{NA}, -I_{NB}, 0, 0]^T$ is the interface current vector of the injected currents from any externally connected circuit. Equation (1) is partitioned where V_{IF} is the voltage vector of interface nodes and V_{IN} of internal nodes (the subscript "IF" stands for interface in this paper). Partitioning the admittance matrix Y and (1) is re-written as

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix}\begin{bmatrix} V_{IF} \\ V_{IN} \end{bmatrix}=\begin{bmatrix} 0 \\ J_{IN} \end{bmatrix}+\begin{bmatrix} I_{IF} \\ 0 \end{bmatrix} \quad (2)$$

Eliminating V_{IN} using Schur's Complement gives (3):

$$\begin{aligned} &(Y_{11}-Y_{12}Y_{22}^{-1}Y_{21})V_{IF}=-Y_{12}Y_{22}^{-1}J_{IN}+I_{IF} \\ &or \\ &Y_{IF}V_{IF}=J_{IF}^{Tsf}+I_{IF} \end{aligned} \quad (3)$$

V_{IF} is calculated using the recursive method described in Section III.A and further discussed in Section III.C. Once the interface node voltages V_{IF} are obtained, the internal node voltages can be updated using (4), to give the capacitor voltage solutions, necessary for computing the history currents J_{IN} in the next time step.

$$V_{IN}=Y_{22}^{-1}[J_{IN}-Y_{21}V_{IF}] \quad (4)$$

C. Nodes Elimination between SMs

This section describes how the node elimination procedure is recursively extended to include other connected two-port SMs. The first step is to eliminate nodes between the first SM and the adjacent SM to get Block 2, then extend it by adding one additional SM and so on until a single equivalent for the whole arm consisting of only 4 interface nodes results. This arm equivalent circuit can then be interfaced to the main interface solver.

After elimination of the internal nodes the interface node equivalent equation given in the lower part of (3) for the first two-port SM can be written as (5). In (5) the vectors are represented as those corresponding to the interface left-hand side nodes (P_A and P_B) and right-hand side nodes (N_A and N_B). The right-hand side nodes N_A and N_B, will be connected to the left-hand side interface nodes of the next SM.

$$Y_{IF}\cdot\begin{matrix} V_L \\ V_R \end{matrix}\left\{\begin{bmatrix} V_{PA} \\ V_{PB} \\ V_{NA} \\ V_{NB} \end{bmatrix}\right.=\begin{matrix} J_L \\ J_R \end{matrix}\left\{\begin{bmatrix} J_{IF\_PA}^{Tsf} \\ J_{IF\_PB}^{Tsf} \\ J_{IF\_NA}^{Tsf} \\ J_{IF\_NB}^{Tsf} \end{bmatrix}\right.+\begin{matrix} I_L \\ -I_R \end{matrix}\left\{\begin{bmatrix} I_{PA} \\ I_{PB} \\ -I_{NA} \\ -I_{NB} \end{bmatrix}\right. \quad (5)$$

Equation (5) is re-labelled to indicate left and right side vectors, then partitioning the 4×4 matrix Y_{IF} into four 2×2 sized daughter matrices and (5) is re-written as

$$\begin{bmatrix} Y_{LL} & Y_{LR} \\ Y_{RL} & Y_{RR} \end{bmatrix}\begin{bmatrix} V_L \\ V_R \end{bmatrix}=\begin{bmatrix} I_L \\ -I_R \end{bmatrix}+\begin{bmatrix} J_L \\ J_R \end{bmatrix} \quad (6)$$

Moving current vectors I_L and I_R to the left-hand side of (6), re-arranging and re-labelling into (7).

$$\begin{bmatrix} Y_{LL} & -\begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix} & Y_{LR} & \begin{pmatrix} 0 & 0 \\ 0 & 0 \end{pmatrix} \\ Y_{RL} & \begin{pmatrix} 0 & 0 \\ 0 & 0 \end{pmatrix} & Y_{RR} & \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix} \end{bmatrix}\cdot\begin{matrix} X_L \\ X_R \end{matrix}\left\{\begin{bmatrix} V_L \\ I_L \\ V_R \\ I_R \end{bmatrix}\right.=\begin{bmatrix} J_L \\ J_R \end{bmatrix} \quad (7)$$

In (7), partitioning the 4×8 matrix into four 2×4 submatrices and re-write (7) into:

$$\begin{bmatrix} A_{LL} & A_{LR} \\ A_{RL} & A_{RR} \end{bmatrix}\begin{bmatrix} X_L \\ X_R \end{bmatrix}=\begin{bmatrix} J_L \\ J_R \end{bmatrix} \quad (8)$$

Equation (8) is a generic form of a single SM with all the internal nodes eliminated. In order to show how to eliminate the interface nodes between two adjacent SMs, let superscripts 1 and 2 respectively indicate the SMs 1 and 2 in (9) and (10).

$$\begin{bmatrix} A_{LL}^1 & A_{LR}^1 \\ A_{RL}^1 & A_{RR}^1 \end{bmatrix}\begin{bmatrix} X_L^1 \\ X_R^1 \end{bmatrix}=\begin{bmatrix} J_L^1 \\ J_R^1 \end{bmatrix} \quad (9)$$

$$\begin{bmatrix} A_{LL}^2 & A_{LR}^2 \\ A_{RL}^2 & A_{RR}^2 \end{bmatrix}\begin{bmatrix} X_L^2 \\ X_R^2 \end{bmatrix}=\begin{bmatrix} J_L^2 \\ J_R^2 \end{bmatrix} \quad (10)$$

As indicated in Fig. 2, the right-hand side nodes of SM 1 (i.e. nodes N_A^1 and N_B^1) are connected to the left-hand side nodes of SM 2 (i.e. nodes P_A^2 and P_B^2), indicating that the node voltages and currents are identical at this interface, i.e.,

$$X_{RL}\ \square\ X_R^1=X_L^2 \quad (11)$$

Substituting (11) into (9) and (10), and restructuring, gives (12) and (13)

$$\left\{\begin{bmatrix} A_{LL}^1 & 0 \\ 0 & A_{RR}^2 \end{bmatrix}-\begin{bmatrix} A_{LR}^1 \\ A_{RL}^2 \end{bmatrix}\begin{bmatrix} A_{RR}^1 \\ A_{LL}^2 \end{bmatrix}^{-1}\begin{bmatrix} A_{RL}^1 & 0 \\ 0 & A_{LR}^2 \end{bmatrix}\right\}\cdot\begin{bmatrix} X_L^1 \\ X_R^2 \end{bmatrix}$$

$$=\begin{bmatrix} J_L^1 \\ J_R^2 \end{bmatrix}-\begin{bmatrix} A_{LR}^1 \\ A_{RL}^2 \end{bmatrix}\begin{bmatrix} A_{RR}^1 \\ A_{LL}^2 \end{bmatrix}^{-1}\begin{bmatrix} J_R^1 \\ J_L^2 \end{bmatrix}$$

or

$$\begin{bmatrix} A_{LL}^{1-2} & A_{LR}^{1-2} \\ A_{RL}^{1-2} & A_{RR}^{1-2} \end{bmatrix}\cdot\begin{bmatrix} X_L^1 \\ X_R^2 \end{bmatrix}=\begin{bmatrix} J_L^{1-2} \\ J_R^{1-2} \end{bmatrix} \quad (12)$$

$$X_{RL}=\begin{bmatrix} A_{RR}^1 \\ A_{LL}^2 \end{bmatrix}^{-1}\begin{bmatrix} J_R^1 \\ J_L^2 \end{bmatrix}-\begin{bmatrix} A_{RR}^1 \\ A_{LL}^2 \end{bmatrix}^{-1}\begin{bmatrix} A_{RL}^1 & 0 \\ 0 & A_{LR}^2 \end{bmatrix}\begin{bmatrix} X_L^1 \\ X_R^2 \end{bmatrix} \quad (13)$$

The superscript "1-2" in the lower part equation of (12) indicates that SMs 1 and 2 are combined into a single block (Block 2), which has an identical structure as that of Block 1

given by (8). Block 2 is next combined with the next SM to give a similar block.

Note that at each stage we require the external interface node voltages to calculate internal voltages V_R^1 and V_L^2, and history terms of the SMs. Assuming these are known (13) can be used to calculate the history terms and internal voltages.

D. MMC Arm Equivalent

Once all the internal nodes of the N cascaded two-port SMs are eliminated, we obtain a form similar to the equation in (12), as in (14).

$$\begin{bmatrix} A_{LL}^{1\text{-}N} & A_{LR}^{1\text{-}N} \\ A_{RL}^{1\text{-}N} & A_{RR}^{1\text{-}N} \end{bmatrix} \begin{bmatrix} X_L^1 \\ X_R^N \end{bmatrix} = \begin{bmatrix} J_L^{1\text{-}N} \\ J_R^{1\text{-}N} \end{bmatrix} \tag{14}$$

Partitioning the matrix in (14) gives (15).

$$\begin{bmatrix} A_{LL}^{1\text{-}N} & A_{LR}^{1\text{-}N} \\ A_{RL}^{1\text{-}N} & A_{RR}^{1\text{-}N} \end{bmatrix} = \begin{bmatrix} a_{LL}^{1\text{-}N} & \alpha_{LL}^{1\text{-}N} & a_{LR}^{1\text{-}N} & \alpha_{LR}^{1\text{-}N} \\ a_{RL}^{1\text{-}N} & \alpha_{RL}^{1\text{-}N} & a_{RR}^{1\text{-}N} & \alpha_{RR}^{1\text{-}N} \end{bmatrix} \tag{15}$$

Substituting (7) and (15) into (14) we obtain an admittance matrix form as in (16):

$$\begin{bmatrix} -\alpha_{LL}^{1\text{-}N} & \alpha_{LR}^{1\text{-}N} \\ -\alpha_{RL}^{1\text{-}N} & \alpha_{RR}^{1\text{-}N} \end{bmatrix}^{-1} \begin{bmatrix} a_{LL}^{1\text{-}N} & a_{LR}^{1\text{-}N} \\ a_{RL}^{1\text{-}N} & a_{RR}^{1\text{-}N} \end{bmatrix} \begin{bmatrix} V_L^1 \\ V_R^N \end{bmatrix} = \begin{bmatrix} -\alpha_{LL}^{1\text{-}N} & \alpha_{LR}^{1\text{-}N} \\ -\alpha_{RL}^{1\text{-}N} & \alpha_{RR}^{1\text{-}N} \end{bmatrix}^{-1} \begin{bmatrix} J_L^{1\text{-}N} \\ J_R^{1\text{-}N} \end{bmatrix} + \begin{bmatrix} I_L^1 \\ -I_R^N \end{bmatrix} \tag{16}$$

or

$$Y_{IF}^{1\text{-}N} V_{IF}^{1\text{-}N} = J_{IF}^{1\text{-}N} + I_{IF}^{1\text{-}N}$$

Equation (16) now permits the MMC model to be interfaced with the main EMT solver (PSCAD in this case), which has a structure as in (17), with Y_{EX}, V_{EX} and J_{EX} being the admittance matrix, nodal voltage vector and internal current injection vectors of the external network. I_{EX} represents the currents injected from the interface. Thus its elements are zero for non-interface nodes, and equal to the corresponding entries from $I_{IF}^{1\text{-}N}$ for interface nodes.

$$Y_{EX} V_{EX} = J_{EX} + I_{EX} \tag{17}$$

Similarly, $V_{IF}^{1\text{-}N}$ is a vector of nodal voltages only at the 4 interface nodes, which are also part of the external circuit. Hence, to obtain the final admittance matrix for the entire system, the elements of the reduced MMC admittance matrix $Y_{IF}^{1\text{-}N}$ are added to the elements of Y_{EX} for the corresponding node pairs to give (18)

$$Y_N V_N = J_N \tag{18}$$

The external EMT network solver then can solve for all node voltages in V_N, which includes the external system voltages as well as the 4 interface node voltages, but not he internal node voltages inside the MMC. However, once the 4 interface node voltages are calculated, we can recursively calculate the node voltages of all internal nodes using the procedure described in section III.A. These are required for finding the history terms of the internal Blocks 1 to N for the next solution time step.

Note that $Y_{IF}^{1\text{-}N}$ is of size 4×4, and so the MMC does not increase the number of nodes in the external circuit. If a direct solution were attempted, it would have added all the internal nodes of the MMC to the external circuit, thereby significantly increasing its size and the corresponding solution effort. It must be realized however, that the price paid for the reduction in size is the added complexity of the recursive procedure.

IV. Simulation Results

Through some representative simulations, this section discusses the speedup afforded by the proposed equivalent algorithm in comparison with a full simulation in which the two-port SMs are modelled within the main EMT solver. It also shows that the proposed approach does not suffer from loss of accuracy.

A. Test System

The circuit shown in Fig. 4 is used for testing the algorithm. It models only a single arm of the SM consisting of N cascaded two-port SMs and 4 external excitation voltage sources with impedances. For the tests, the number of SMs N ranges between 48 and 576. In Fig. 4, the ac fundamental frequency f_0 = 60Hz, the SM capacitance C = 2mF and the excitation voltage source parameters are listed in Table I.

TABLE I
Excitation Source Parameters

Source	Value (L-G, RMS)	Initial phase	Impedance	Value
U_{S1}	3.0 kV	0°	R_{S1}	6.0 Ω
U_{S2}	1.5 kV	30°	R_{S2}	1.0 Ω
U_{S3}	1.8 kV	45°	R_{S3}	2.0 Ω
U_{S4}	0.8 kV	25°	R_{S4}	8.0 Ω

The computer used in this paper is an Intel(R) Core(TM) i7-6700 3.40GHz CPU with 16GB RAM and 64-bit Windows 10 Operating System. All the models were implemented on PSCAD/EMTDC Professional V4.6. The simulation time step is 20 μs and the duration is 1s.

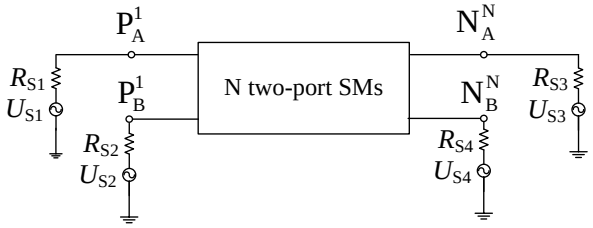


Fig. 4. The test cascaded two-port SMs circuit.

B. Accuracy

In this scenario, a MMC arm with 12-cascaded two-port SMs is simulated using both detailed and proposed models. The capacitor voltages in SMs 1 and 7 from both models are plotted in Figs. 5 and 6.

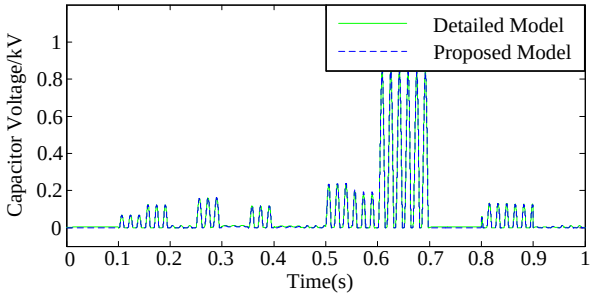


Fig. 5. The capacitor voltages comparison in SM 1.

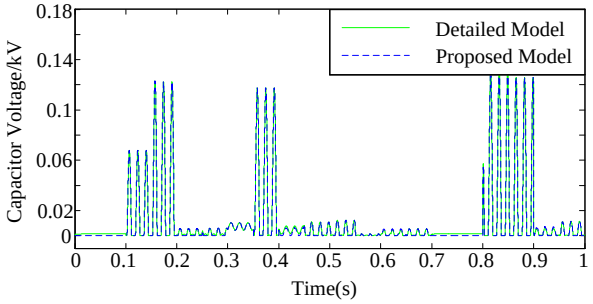


Fig. 6. The capacitor voltages comparison in SM 7.

Figs. 5 and 6 indicate that with the same circuit configuration and triggering signals, the internal capacitor voltages from both models are essentially identical. Note that the capacitor voltages will never go negative otherwise the diodes in Fig. 2 would turn on to discharge the capacitors.

The interface nodal voltages V_{PA}, V_{PB} and the interface branch currents I_{PA}, I_{PB} from both models are compared in Figs. 7 and 8 respectively.

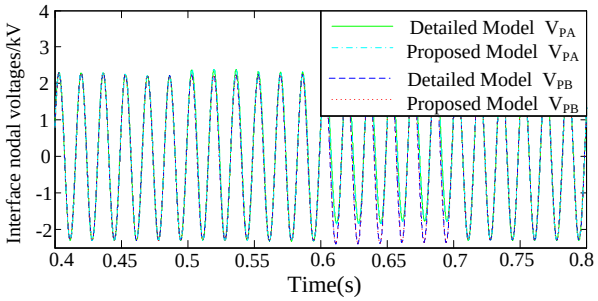


Fig. 7. The interface nodal voltages comparison.

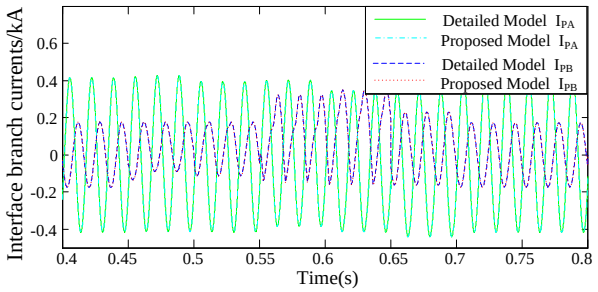


Fig. 8. The interface branch currents comparison.

The interface nodal voltages and branch currents agree perfectly as well which indicate that the proposed equivalent model can faithfully reproduce the behaviors of the entire cascaded two-port SMs from the detailed model without losing accuracy.

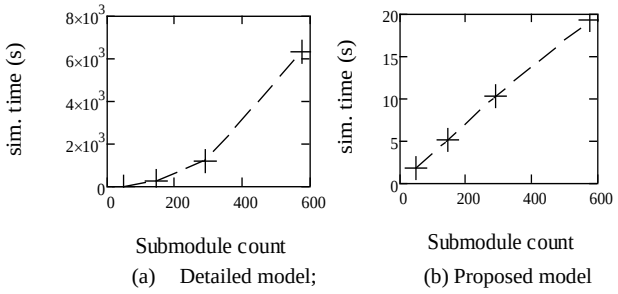
C. Speedup Factor

The MMC arm with 48, 144, 288 and 576 cascaded two-port SMs both in the detailed and proposed models are simulated and the computational times as well as the speedup factor are listed in Table II. For a SM count larger than 288, there is a speedup of approximately 2 orders of magnitude. For example, with 576 SMs, the proposed model gives a speedup factor of 328.6, which is over 2.5 orders of magnitude faster than the detailed model. This approaches the speedups for previous algorithms for the simpler one-port MMC converter topologies with half or full-bridge SMs [1]-[5].

TABLE II
SIMULATION TIMES TEST

SM count	Simulation times (s) (detailed model)	Simulation times (s) (proposed model)	Speedup factor
48	30.0	1.9	15.8
144	237.7	5.2	45.7
288	1171.7	10.4	112.7
576	6343.2	19.3	328.6

The simulation times in Table II are also graphically shown in Fig. 9. An interesting observation is that the simulation time for the proposed model is almost linear with the SM count, however, for the detailed model, the simulation time shows a quadratic relationship with the SM count.



(a) Detailed model; (b) Proposed model

Fig. 10. Simulation times of the MMC models.

V. CONCLUSIONS

In this paper, a high speed and accurate electromagnetic transient modeling approach of the MMC-HVDC converters composed of two-port SMs is developed. It sequentially combines SM blocks into larger blocks until a single equivalent is realized for the bridge arm with only four external interface nodes. The resulting small (4×4-size) admittance matrix is overlaid onto the external systems admittance matrix, and the history current contributions from the MMC circuit are added to the history current contributions of the external network only at the interface nodes. This greatly reduces the computational burden on the main EMT solver and achieves at significant speedup. Although internal nodes are eliminated in this approach, their values are recovered by a recursive procedure that works inwards once the interface nodes are solved for by reversing process by which the blocks were created.

The developed high-speed two-port MMC models are validated by comparison with an EMT simulation of the detailed model with each SM modelled separately. Simulation results show that the proposed models are accurate and simulation time scales linearly with the SM count, as opposed

to quadratically with a detailed model. For SM counts over 300, the speedup is over 2 orders of magnitude.

VI. Acknowledgment

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VII. References

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