Development of Protective Method based on Superposition Principle along with Fault Current Limiter in Low Voltage DC Distribution System

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***Abstract*—Low Voltage DC (LVDC) distribution system is the future technology, which the researchers are looking towards, to supply the power to end-users. However, one major obstacle in implementing LVDC distribution system is protecting the system against faults. This is because dc faults have much different characteristics than the traditional ac system faults, which brings new challenges for protection devices and protection schemes. Therefore, in this paper, a new fault detection scheme based on superimposed current components is proposed. A fault current limiting method along with isolation technique is proposed while considering dc fault characteristics. Once a fault is detected, a high impedance fault current limiter is introduced for few milliseconds to keep the sensitive devices safe and to improve the reliability of the system in case of temporary faults. Also, the method is helpful to reduce the circuit breaker stress during fault interruption.**

***Keywords*: DC short-circuit fault, fault detection, Low Voltage DC distribution system, protection system.**

I. Introduction

DEVELOPMENTS in power electronics have led us to consider the dc system, since most of the electronic devices need dc supply. Conventional ac system supplies power to these electronic devices with internal and individual conversion methods, which cause power losses. On the other hand, the integration of distribution generation (DG) with the distribution system is getting wider attention by researchers. Most of these DG sources are of dc inherent (Solar cells, converter fed sources) [1]. Considering both sources and loads of being dc nature, recently Low Voltage DC (LVDC) distribution system is proposed as a solution to reduce the conversion losses, improve efficiency and easier integration with DG [2], [3].

Although, LVDC distribution system can easily integrate various types of DGs because of absence of frequency and phase angle, dc technology itself is more complex compared to ac technology [4], [5]. The biggest barrier in implementing LVDC distribution system is its protection during abnormal conditions [6]. Protection of the power electronics devices used in dc system is the vital task to be considered, to avoid the damage to them. Moreover, (customer) loads must be protected on high priority basis. These devices are very sensitive to the transients and cannot sustain high magnitude of dc fault current.

DC fault has different characteristics from ac fault. Unlike ac fault, there is no zero crossing in dc fault current. In addition, the large inductance of generators and transformers in ac grid limits the short circuit current. In contrast, a dc grid has very low inductance and the short-circuit current is mainly limited by the resistance [7]. A dc grid is mainly fed by converters, so, when a fault occurs on a line, the smoothing capacitor of ac/dc converter discharges very fast, it decreases the rise time and increases the magnitude of the fault current like a catalyst [8]. These characteristics of dc fault create a big challenge for protection devices to act very fast and accurately.

This paper proposes a new protection scheme for the short circuit faults in an LVDC distribution system. In the proposed scheme, fault is detected by high speed relays which use superimposed quantities. The method uses superposition principle to assess the voltage and current changes occurring in the line during transients and faults. An algorithm is developed to provide fault current limiter (RL circuit) as an alternate path through Solid State (SS) switches to these steep rising high magnitude fault currents. Finally, circuit breaker is used to isolate the faulted line.

The method is implemented in a typical LVDC distribution system with several dc loads using ElectroMagnetic Transients Program (EMTP), which is very effective software for transient studies in the power system. High speed relays are placed beside grid connected ac/dc converter and at the beginning of each line. Faults are considered at the main busbar, distribution line and end-user side. The study shows that the proposed method is quick and reliable to detect the fault within minimum amount of time and the faults are cleared in safe limits to protect sensitive electronic devices and loads.

II. Fault Characteristics of An LVDC Distribution System

An LVDC distribution system mainly consists of grid connected ac/dc converters, dc distribution lines and dc/dc converters for suitable customer voltage level. Fault

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characteristics of a grid-connected converter based LVDC distribution system are much different than ac type distribution system [9]. When a fault occurs in the dc distribution system, IGBT switches of ac/dc converter are blocked for self-protection and filter capacitor of the converter quickly discharges and acts like a catalyst to the fault, thus, making fault current severe [9], [10].

There are two types of dc faults, 1) line-to-line fault and 2) line-to-ground fault. Line-to-ground faults are more frequent but less critical and line-to-line or short-circuit faults are less frequent but more critical. The line-to-ground fault characteristics depend upon the grounding method of the distribution system. A line-to-line fault forms an RLC circuit. An equivalent circuit of dc short-circuit fault is shown in Fig. 1.

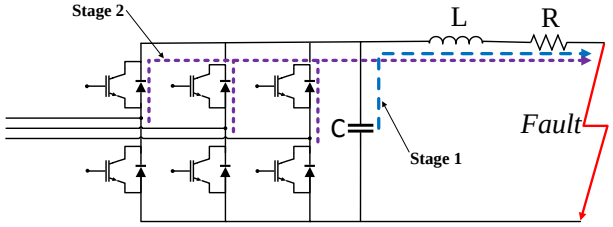

Fig. 1. The short circuit current response of a grid connected LVDC distribution system.

The response of a dc short-circuit fault can be categorized into three steps. 1) Capacitor discharge step (Natural response), 2) Diode freewheel step (it starts once capacitor is fully discharged V_c=0), 3) Grid-side current feeding step.

1) Capacitor discharge stage - At first, Capacitor discharge takes place exponentially as (1), until its voltage in (2) becomes zero [11].

$$i_c = C\frac{dV_c}{dt} = -\frac{I_0\omega_0}{\omega}e^{-\delta t}\sin(\omega t-\beta)+\frac{V_0}{\omega L}e^{-\delta t}\sin\omega t \quad (1)$$

$$V_c = \frac{V_0\omega_0}{\omega}e^{-\delta t}\sin(\omega t+\beta)-\frac{I_0}{\omega C}e^{-\delta t}\sin\omega t \quad (2)$$

Where, i_c is the capacitor discharge current, V_c is the voltage across the capacitor, I_0 and V_0 are the initial current and voltage of filter capacitor respectively. C is the capacitance, $\omega_0=\sqrt{\delta^2+\omega^2}$, $\beta=\arctan(\omega/\delta)$, $\delta=R/2L$, and $\omega=\sqrt{1/LC-(R/2L)^2}$.

The capacitor voltage drops to zero by the time

$$t_1 = t_0+(\pi-\gamma)/\omega \quad (3)$$

where,

$$\gamma = \arctan[(V_0\omega_0 C\sin\beta)/(V_0\omega_0 C\sin\beta - I_0)] \quad (4)$$

2) Diode freewheel stage - Once the capacitor is fully discharged, the antiparallel diodes of ac/dc converter will be forward biased and will continue to supply the fault during this stage. The fault current of dc cable inductance will circulate in the diodes, which is given as

$$i_L = I_0^{'}e^{-(R/L)t} \quad (5)$$

where $I_0^{'}$ is the initial value of inductor current at t_1.

3) Grid supply stage - After second stage when the transient has passed, the connected grid will supply a steady state dc fault current through the diodes. Each leg of the converter will pass its phase current [12].

$$i_{ga} = I_m\sin(\omega_s t+\alpha-\phi)+[i_{m0}\sin(\alpha-\phi_0)-I_m\sin(\alpha-\phi)]e^{-t/\tau} \quad (6)$$

Where, ω_s is the synchronous angular frequency, α is the voltage angle of phase a, and

$$\phi = \tan^{-1}(\omega_s(L_g+L)/R) \quad (7)$$

Where, $\tau=(L_g+L)/R$ and I_m is the magnitude of the grid current, I_{m0} is the amplitude of the initial grid current, ϕ_0 is the initial phase angle, L_g is the grid inductance. This is the current contribution for phase A. The sum of all three phase currents i_{ga}, i_{gb}, i_{gc} will give the total current contribution to the dc steady state fault current by the grid.

III. State-of-The-Art Research on Protection of the DC Distribution System

As described earlier, a grid-connected dc fault current can be categorized into three stages, each stage has its own challenges. Considering this fact, different protection schemes have been proposed.

Earlier, protection from ac-side circuit breaker for dc faults were proposed [13], but due to an increasing interest on dc network, focus has been shifted to directly interrupt a dc fault. An approach of interrupting dc fault through current zero crossing was proposed in [14]. This was attained forcefully by using a series reactor along with electromagnetic circuit breaker.

Recently, researchers have focused on directly interrupting dc fault from dc side with no current zero crossing. Modified overcurrent based scheme [15], differential and travelling wave approach are proposed while considering dc fault characteristics. Overcurrent based protection is widely applied for currents at distribution system. This is because overcurrent based protection is very simple and economical [16]. An overcurrent protection for high resistance faults such as 10 Ω to 200 Ω is proposed in [15].

A protection scheme with an arrangement of ac and fast acting electronic devices is proposed in [12], the method is suitable for detecting the fault through current directions, but there is no direct protection for ac/dc converter from dc side which is the main supply. This problem is solved in [17], but both are communication based schemes. DC faults must be interrupted within few milli-seconds therefore, a small delay or failure in communication system could lead towards system vulnerability.

A differential protection scheme protects a bounded zone of the system and cannot operate for the faults outside of that zone. Moreover, a challenge to differential protection is to guarantee the fast and accurate protection operation within coordinated time frame allocated at different points for a dc distribution system. To avoid the communication delay, in [18] a high bandwidth communication system is suggested to operate the protection within derived operating times. A central processing unit based high speed differential protection scheme against dc distribution system fault is proposed in [19]. A master/slave based differential protection for a loop-type dc

bus microgrid is proposed in [7].

The travelling wave approach for detecting and locating the fault attracted researchers due to the Global Positioning System (GPS) receivers for an accurate time synchronization. Nevertheless, the requirement of phasor information, two terminal measurements, and high sampling rate limit the practicality of the method. Furthermore for dc systems, there is an inherent limitation of lack of frequency and phasor information [8]. In addition, travelling wave approach for fault detection seems unfeasible for distribution system due to its short cable length in comparison with the transmission lines [20].

Fault detection through initial rate of change of dc current is proposed in [21], [22], a central processing unit is used for protecting a ring dc bus [23].

In conclusion, different schemes for protecting against dc faults are proposed for different network topologies. However, still there are challenges that exist for the practicality of these schemes. In addition, more research and in-depth study is still required for a high speed fault detection and interruption in LVDC distribution system, for reliable and quality supply to end-users.

IV. Proposed Protection Scheme

A new fault detection technique based on the transient characteristics of the fault current is proposed. In the proposed scheme, fault is detected by high speed relays which use superimposed quantities. The method uses superposition principle to assess the voltage and current changes occur in the line during transient or fault. An algorithm is developed to provide a high impedance fault current limiter to reduce the strength of the steep rising high magnitude short circuit fault current through SS Switches. Finally, Circuit Breaker can easily isolate the faulty line.

A. Superimposed current components

In the power system when fault occurs, superimposed components appear in the system. They contain fault signatures and are independent of the normal operating conditions of the system [24]. The idea is based on superposition theorem, in which the system can be categorized into two parts (Pre-fault condition and post-fault condition). The post-fault quantities do not exist during normal operating condition. Thus, any value they have due to a fault condition represents a change or delta quantity. Therefore, they are called incremental or superimposed quantities [25].

For voltage

$$v_{post-fault} = v_{pre-fault} + \Delta v \tag{8}$$

Similarly, for current

$$i_{post-fault} = i_{pre-fault} + \Delta i \tag{9}$$

Where subscript *pre-fault* denotes a quantity before the occurrence of a fault and *post-fault* denotes a quantity after the fault appearance. ‘ Δ ’ describes change in the current or voltage due to fault transient.

Historically, delta filters were used to extract the superimposed quantities. The basic delta filter generates a delay signal from the input signal which follows the input signal with a time delay. The applied delay time is called Delta-filter delay and the delayed signal is called reference signal [25], [24]. Fig. 2. shows the concept of a basic delta filter for a dc current.

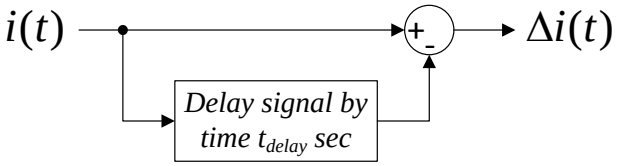

Fig. 2. The concept of a delta filter for dc current signal.

B. Relay operation to detect the fault current

The relay calculates the superimposed current using (9). Once a pre-set threshold value is crossed, a constant but very short time delay is executed to verify whether it is a fault or not. Both these conditions are transformed into binary signals and passed through a logic gate as shown in Fig. 3. If both the conditions become true, the relay generates a fault signal and commands for an interruption of the fault described in detail in next section.

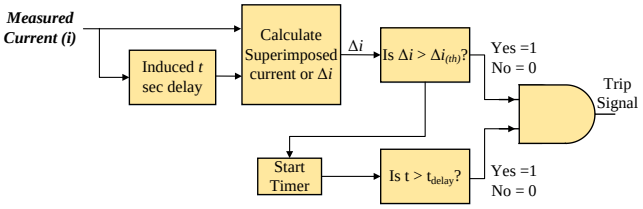

Fig. 3. Relay algorithm for detecting the fault current.

C. Fault Current Limiter and Circuit Breaker Operation

Previous experiences have shown that up to 80% - 90% of the overhead distribution line faults are temporary in nature, which can go for several milliseconds [16]. In conventional ac distribution system, these faults are detected and isolated by tens of milliseconds. Moreover, circuit breaker recloser option decides whether a fault is temporary or permanent, and acts accordingly.

However, an LVDC distribution system consists of different type of converters spread in every part of the network, which contain charged filter and dc link capacitors. When a low impedance fault occurs in this type of the distribution system, these capacitors discharge in few milliseconds, and if a fast enough protection scheme has not been applied, the system will start acting vulnerably. Because such a fast protection operation is required, it becomes very difficult to analyze or differentiate between a transient, temporary or permanent fault. Since the reclosing option of circuit breaker will make the dc distribution system more vulnerable. In addition, locating the fault in such a short duration becomes very much challenging.

Therefore, in the proposed scheme when a high speed relay detects a low impedance fault, it introduces a high impedance fault current limiter through SS switches. The fault current limiter, which consists of an RL circuit, reduces the strength of the fault current magnitude and resists the filter capacitors

from discharging. Once the faulty line undergoes the fault current limiter, it enters into the critical mode. Fig. 4 shows the current flow during normal operation and during a fault. The snubber circuit is used to eliminate the voltage spikes and to limit dv/dt produced across the SS switch during switching transient. An RCD charge-discharge type snubber is used here [7].

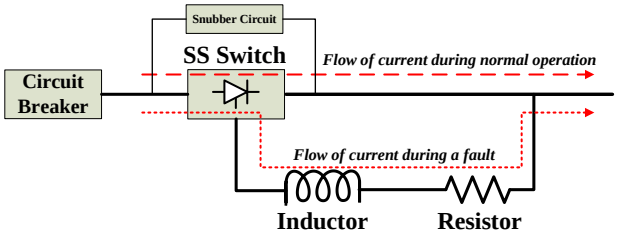

Fig. 4. The flow of current during normal operation and during a fault.

The use of fault current limiter prevents the dc link voltage from dropping to zero. Hence, freewheel diode conduction stage of converter (which is the most challenging stage during a fault) can easily be avoided.

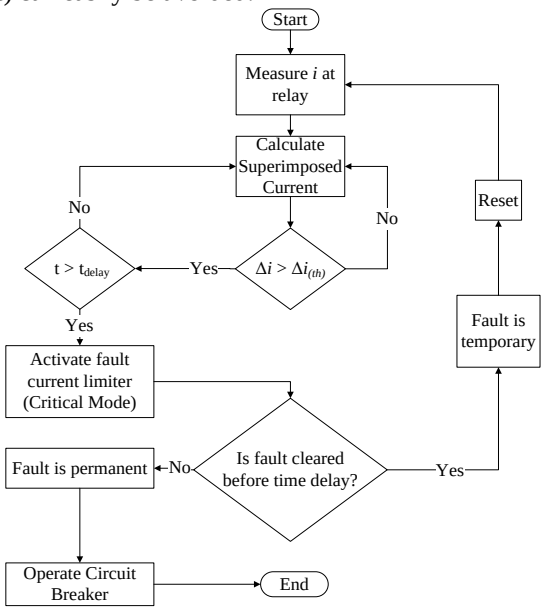

Fig. 5. Flowchart describing complete protection action.

In the critical mode, the faulty line is allowed to operate for a specific time delay through the fault current limiter. This time delay may contain several milliseconds depending upon the system configuration and flexibility. Once the delay time elapsed, the relay checks whether the fault is still present in the system or not. If the fault vanishes during the critical mode after a short transient period, the current magnitude will reach to a steady state value lower than its actual rated current, observed before the occurrence of the fault. The current is less than the pre-fault current because of the impedance of the fault current limiter. As a result, the relay will act and restore the system from its critical mode to normal operating mode. On the other hand, if the fault still exists, which can be analyzed by another threshold value (set by the relay under critical mode), the fault is considered as permanent fault and the relay will send a trip command to the circuit breaker to isolate the faulty section. Fig. 5. Shows the flowchart of protection operation by the relay for temporary and permanent faults.

V. Case Study

To verify the effectiveness of the proposed scheme, a radial unipolar grounded (TN) distribution system is implemented in ElectroMagnetic Transient Program (EMTP) as shown in Fig. 6. Radial systems are widely used in distribution system due to their simplicity and economic benefits. The distribution system provides 1500 Vdc voltage level to 35 kW connected load. The customers are supplied power through dc/dc buck converters by reducing voltage level to 380Vdc. The cable length for each line is 4 km and its parameters are R=0.164Ω/km and L=0.24mH. The relays along with the fault current limiter and circuit breaker are applied at the output of ac/dc converter (main supply source) R_1, and at the start of each distribution line R_2 and R_3. A value of 5 Ω and 10 mH are used here for the fault current limiter RL circuit. The system is unipolar and fault current limiter is employed on both the lines. Short circuit faults are considered at four different locations as shown in Fig. 6.

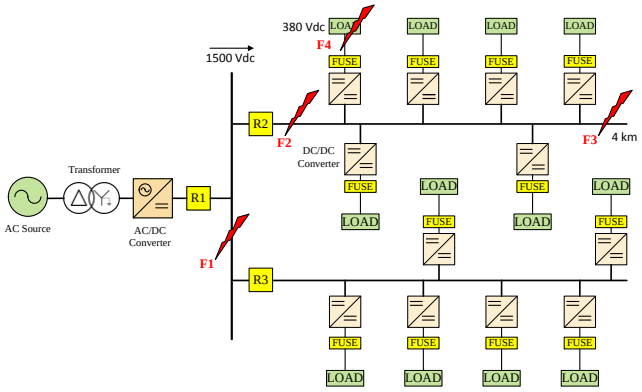

Fig. 6. One-line diagram of a Unipolar, grounded, radial type LVDC distribution system

Fault F_1 occurs at the busbar, is the most critical fault location. It can seriously damage the main converter. Therefore, a relay along with fault current limiter and circuit breaker are employed at the ac/dc converter output R1 in particular, to protect the converter from the faults at location F1 as shown in Fig. 6.

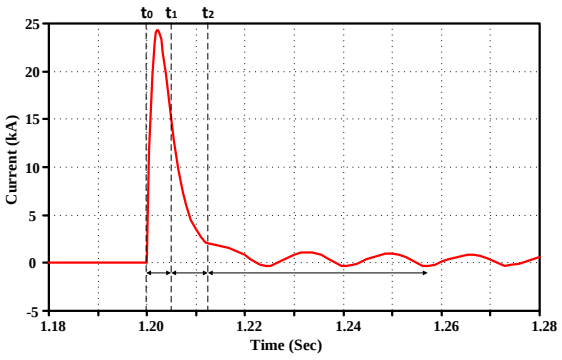

Fig. 7. Actual Current observed at R1 during a short-circuit fault at F1 with fault resistance 0.01Ω.

A short-circuit fault of 0.01Ω is considered and three stages of the fault current i.e. 1) Capacitor discharge stage, 2) Diode Freewheel stage and 3) Grid supply stage are shown in Fig. 7. The fault occurs at t_0=1.2 sec. The capacitor discharges fully after t_1 = 5.1ms, and stage 2 completes after t_2 = 12ms, after that a steady-state current is supplied by the grid. The circuit observes oscillation because of low resistance and it responds underdamped i.e. $R < 2\sqrt{L/C}$.

Faults F2, F3 and F4 occur at start of the line, end of the-line and at the end-user, respectively. Faults initiate at 1.20 sec. Superimposed currents calculated by the relay at R2 for the faults F2, F3 and F4 with fault resistance 0.1 Ω are shown in Fig. 8. These are purely fault currents, which are zero before the fault inception.

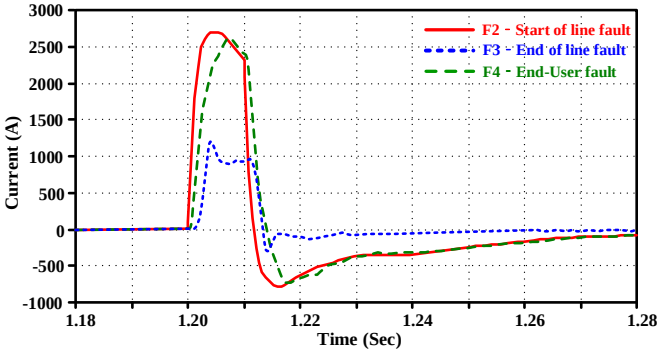

Fig. 8. Superimposed currents calculated at R2 for line-to-line faults at F2, F3, F4 without protection (fault resistance 0.1 Ω).

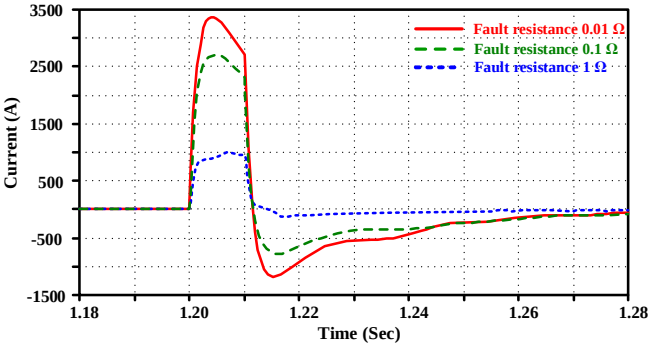

Fig. 9. Superimposed currents calculated at R2 for line-to-line faults at F2 with resistances 0.01 Ω, 0.1 Ω and 1 Ω without protection.

Fault detection time can be affected by many factors, such as exact fault location, fault resistance or network topology etc. Moreover, faults with different resistances (0.01 Ω, 0.1 Ω and 1 Ω) at the same location F2 are shown in Fig. 9 and it can be confirmed that fault resistance clearly effects superimposed currents.

Fig. 10 shows the actual currents of the fault F2, observed at the relay R2 without and with the proposed protection scheme. The pickup current (Δi_{th}) for the relays at R2 and R3 are set as double of the rated current i.e 20 A with a constant time delay (t_{delay}) of 1 ms. The current reaches upto 1.6 kA within this time before the fault current limiter is activated. The current reaches that high because of the fast discharge of the smoothing capacitor. The fault current limiter lowers the current magnitude and can easily be tripped without putting stress on the circuit breaker, even with a low rated circuit breaker. A delay time of 0.1 sec is set for the critical mode here. After the applied delay, if the fault still exists, a trip command is sent to the local circuit breaker as shown in Fig. 11. The converter output voltage also improves from collapsing during this process as shown in Fig. 12.

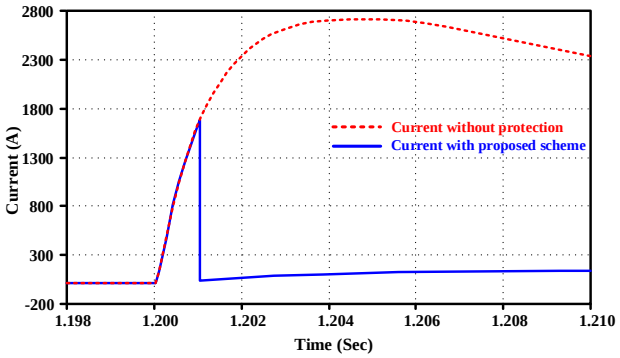

Fig. 10. Actual currents observed by the relay at R2 during line-to-line fault at F2 without and with proposed protection scheme.

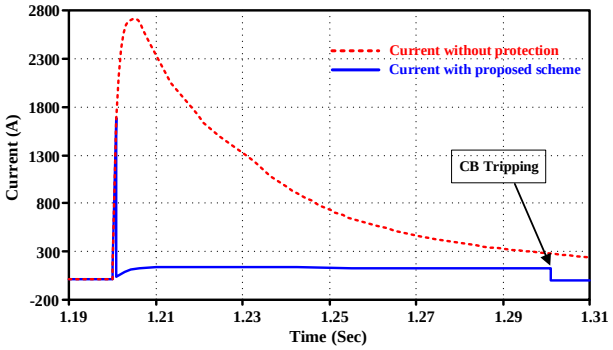

Fig. 11. Tripping a long duration fault through proposed protection scheme.

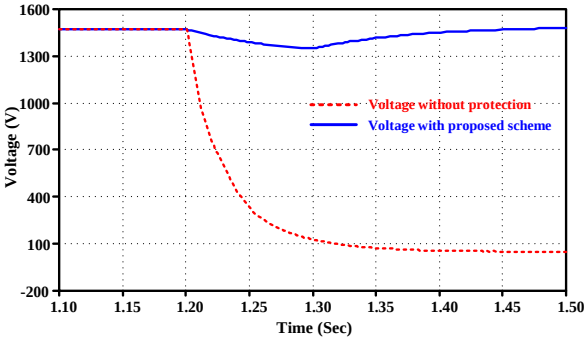

Fig. 12. The converter output voltage with and without proposed protection scheme.

Furthermore, a short duration fault at the same location F2 is applied. Fault started at 1.20 sec and vanished at 1.25 sec. After the delay time surpassed, system is restored at 1.29 sec. Actual current observed at the relay R2 is shown in Fig. 13. Current oscillates at first due to the LC contribution before reaching to its steady state value.

Ac/dc converter output voltage and customer voltage is shown in Fig. 14 and Fig. 15 respectively.

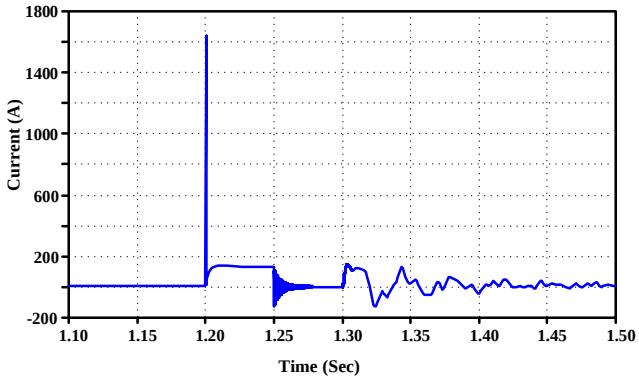

Fig. 13. Actual current at R2 for a short duration fault with proposed protection scheme.

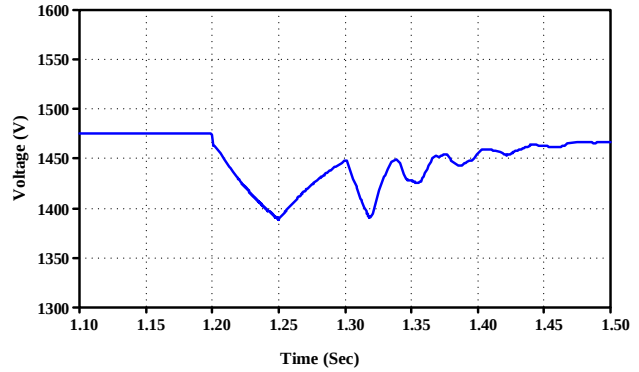

Fig. 14. Converter output voltage for short duration fault at F2 with proposed protection scheme

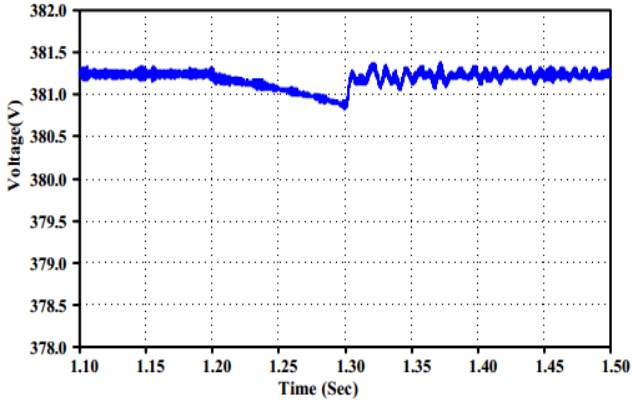

Fig. 15. Customer voltage for short duration fault at F2 with proposed scheme

VI. Conclusion

The paper proposed a new fault detection scheme based on superimposed fault current components. To achieve this, a reference current signal is extracted from actual current with a time delay and both the signals are compared. Simulation results have shown that fault can be detected fast enough (within 1 ms). As superimposed current value does not exist during steady state operation of the system, the relay threshold value can be lowered.

A fault current limiter is introduced for high magnitude, steep rising converter based dc fault current. Through fault current limiter dc fault current is limited for a while and surveilled. If fault is for a short duration, system restores back to its normal path without isolating it. For a permanent fault, relay sends a trip signal to circuit breaker. Reliability of the system can be improved through proposed protection scheme. Circuit breaker can interrupt the fault without much stress, because the fault current limiter limits the fault current magnitude. The simulation results showed the effectiveness of the proposed scheme. To derive the exact values of R and L, and selection of the particular SS switches will be discussed in future for the practicality of the proposed protection scheme.

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