Transient and Steady-State Analysis of Flyback Converter with Non-Dissipative LC Snubber

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***Abstract*—High voltage spikes occur in a switching transistor during turn off in a power converter with a transformer, resulting high power dissipation. The objective of this study is to reduce the voltage spikes and the power loss of a DC-DC converter. An LC snubber circuit reduces the voltage spikes which are caused by the magnetic energy stored in the transformer leakage inductance and transfers the stored energy effectively to the input side of the power converter. In this study, a non-dissipative LC snubber is employed with a flyback converter, operating in continuous conduction mode (CCM). The LC snubber is utilized to attain zero voltage switching (ZVS) and/or zero current switching (ZCS) operation for the switching transistor during turn off/ turn on and soft switching for power diodes. The operating principle, design methodology and analysis of a flyback converter with an LC snubber are presented with a designed example of a 15W (15V/1A) DC-DC converter, operating at a switching frequency of 300kHz. Digital simulations are carried out in SIMULINK/ MATLAB.**

***Keywords*: Switching transients, flyback converter, LC snubber circuit, leakage energy, zero voltage switching.**

I. Introduction

A flyback converter is one of the most widespread topologies of the isolated DC-DC converters which is used in low power applications due to its simplicity, low cost and low parts count. The flyback transformer serves as an energy storage medium and converter isolation in practical applications. However, the leading shortcomings of a conventional flyback converter are as follows:

- A large surge voltage arises during transistor turn off in a power converter with a transformer due to resonance between the transformer leakage inductor and the output capacitor of the switch.
- To achieve high power density, these converters are operated at high switching frequencies, resulting in high power dissipation and reduction in the power efficiency.
- High voltage stress on a switch at turn off increases the conduction losses.
- The output diode is functioned at hard switching, and the reverse recovery is high.

To overcome the aforementioned drawbacks, it is inevitable to employ some soft switching techniques like zero-voltage switching (ZVS) and/or zero-current switching (ZCS) on the main switch and output rectifier. An RCD snubber [1] limits the voltage spikes across the main switch, but the stored energy dissipates through resistor, thus reduces efficiency. Active clamp snubber, consisting of a switch and a capacitor is proposed [2]-[4] to reduce the voltage spikes and recycling of stored energy in leakage inductance, but the auxiliary switch requires a complex control and a gate driver circuit. Active zeta converter [5] achieves ZVS turn-on of the switches. However, it requires more circuit elements. In low voltage applications, output diode is replaced with an MOSFET [6] but the gate drive of this switch is proportional to the voltage applied.

Two-switch pulse width modulation (PWM) flyback converters [7], [8] limit the voltage spikes, but the control structures become complex and the cost increases. In many soft switching techniques, including passive and active ones, the stored energy in the snubber circuit is transferred to the input [9], [10]. In [11], a lossless passive snubber is presented that transfers the stored energy to the output side. A non-dissipative LC turn-off reduces the voltage spikes on a switching circuit [12]. A high efficiency flyback converter with an energy regenerative snubber is presented in [13]. A Boundary Mode Forward-Flyback Converter (BMFFC) uses an auxiliary circuit consists of an LC to provide ZVS condition for primary switch during turn off instances [14].

In this paper, we present a flyback converter operating in the continuous conduction mode (CCM) which employs a non-dissipative LC snubber circuit, consisting of a capacitor, inductance and two diodes. This study highlights the operating characteristics of the proposed design under transient and steady-state conditions. The converter takes into account some major parasitics present in the circuit like transistor output capacitance and transformer leakage inductance to highlight its performance. The proposed LC snubber circuit recovers the energy stored in the leakage inductance of the flyback transformer effectively, thus increases the energy conversion efficiency. This design is also used to achieve ZVS operation at turn off and ZCS at turn on for the switch so as to minimize the effects of the transformer leakage inductance.

We present the evaluation of a single switch PWM flyback converter with an LC snubber circuit for DC-DC conversion applications. A designed example of 15W, 15V/1A CCM flyback converter with an LC snubber circuit is presented and simulated. The basic principle of operation is analyzed and a design procedure is developed. The results demonstrate that the circuit components parameters derived in this study meet the desired objectives.

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This study is conducted through a systematic approach of following steps:-

- Detailed design methodology and optimal values of the proposed snubber circuit elements are achieved.
- Voltage ratings of the transistor and diodes are recognized.
- Operating principles, transient and steady-state analyses of the proposed design are explained.
- Analysis of the transistor power loss is made.

The major contributions of this study are as follows:

- Efficient suppression of voltage surges arises during turning off the transistor.
- Recovery of the magnetic energy stored in the transformer leakage inductance.
- ZVS/ZCS operation for the transistor is possible.

The rest of this paper is organized as follows: In Section II, circuit configuration is illustrated. The design guidelines of the converter with an LC snubber circuit are provided in Section III. In Section IV, simulation results and analysis are presented. Finally, the paper is concluded in Section V.

II. Circuit Configuration

The proposed design of a flyback converter with an LC snubber circuit is shown in Fig. 1. A flyback converter has two phases: energy storage and transfer. In energy transfer phase, the transistor is turned on and the transformer may be treated as a series inductor, while the output diode is reverse biased. In energy transfer phase, the primary current drops to zero, while the output diode starts to conduct and current flows.

The symbols used in Fig. 1 are as follows:

Q Power transistor
L_m Magnetizing inductance
L_{leak} Leakage inductance
D_o Output diode
C_o Output filter capacitance
R_o Load resistance
C_{sn} Snubber capacitor
L_{sn} Snubber inductance
D_1,D_2 Snubber diodes
C_{oss} Transistor output capacitor
N_{ps} Transformer turns ratio
V_{in} Input supply voltage
V_{out} Output voltage
F_{sw} Switching frequency
T_{sw} Switching time
t_{on} Turn on time
t_{off} Turn off time
P_{out} Output power
V_{gs} Transistor gate-to-source voltage
V_f Voltage across output diode
D_{max} Maximum duty cycle

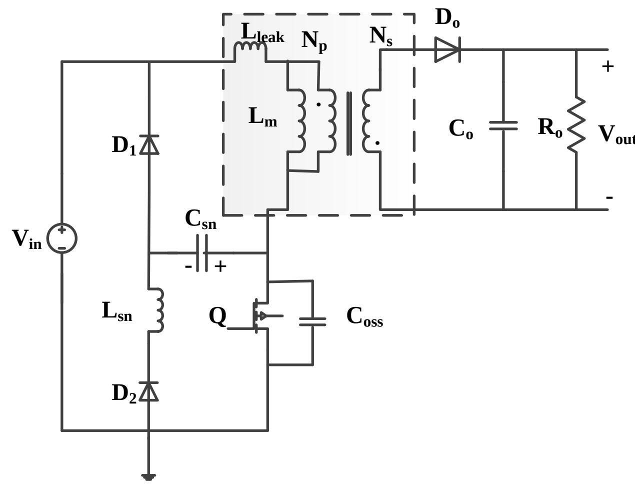

Fig. 1. Flyback converter with an LC snubber circuit

Table I shows the comparison of the proposed method with different design methods, whereas Table II shows the comparison of the proposed design with similar works cited in this paper. In both tables, the number of components used and feedback control system are selected as cost performance indicators.

TABLE I
Comparison of the Proposed Method with Different Design Methods

Parameter	**Methods**					**Proposed Method**
	RCD [1]	**Active Clamp [2-4]**	**Active Zeta [5]**	**Synchronous [6]**	**Two-switch [7]**	
Components count	Transformers 1No. Switch 1No. Capacitors 2No. Diodes 2No.	Transformer 1No. Switches 2No. Capacitors 2No. Diode 1No.	Transformers 2No. Switches 2No. Inductor 1No. Capacitor 1No. Diode 1No.	Transformer 1No. Switches 2No. Capacitor 1No.	Transformer 1No. Switches 3No. Inductor 1No. Capacitors 2No. Diodes 3No.	Transformer 1No. Switch 1No. Inductor 1No. Capacitors 2No. Diodes 2No.
Cost	Low	High	High	High	High	Low
Turn on switching	Hard	ZVS	ZVS	Hard	Hard	ZCS
Turn off switching	Hard	ZVS	ZVS	Hard	Hard	ZVS
Switch voltage stress	Limited	None	None	Limited	None	None
Rectifier diode switching	Hard	Hard	Soft	ZVS	Hard	ZCS/ZVS
Control system	Simple	Complex	Complex	Complex	Complex	Simple

TABLE II

COMPARISON OF THE PROPOSED METHOD WITH SIMILAR DESIGN METHOD

PARAMETER	[8]	[12]	[13]	PROPOSED
Components count	Transformer 1No. Switches 2No. Inductor 1No. Capacitors 2No. Diodes 5No.	Transformer 1No. Switch 1No. Inductor 1No. Capacitors 2No. Diodes 2No.	Transformer 1No. with a reset winding Switch 1No. Capacitors 2No. Diodes 2No.	Transformer 1No. Switch 1No. Inductor 1No. Capacitors 2No. Diodes 2No.
Cost	High	N/A	High	Low
Start-up transients	N/A	N/A	N/A	Discussed <=330μs
Switch turn on/off	ZCS/ZVS	Discussed	ZCS/ZVS	ZCS/ZVS
Rectifier diode switching	ZCZVS	N/A	N/A	ZCS/ZVS
Feedback control system	Complex	N/A	Complex	Simple

III. DESIGN PROCEDURE

A brief design procedure of the proposed converter design is described here. Design specifications are given in Table III.

TABLE III

DESIGN SPECIFICATIONS

S.NO.	PARAMETER	SYMBOL	VALUE
1	Input voltage	V_{in}	5V
2	Output voltage	V_{out}	15V
3	Output current	I_{out}	1A
4	Output power	P_{out}	15W
5	Switching frequency	F_{sw}	300kHz

A. Designing of flyback converter components

The conversion ratio of flyback converter in CCM is:

$$\frac{V_{out} - V_f}{V_{in,\min} - V_{gs(on)}} = \frac{1}{N_{ps}}\left[\frac{D_{\max}}{1 - D_{\max}}\right] \quad (1)$$

For CCM, the switching period is:

$$T_{sw} = t_{on} + t_{off} \quad (2)$$

In a flyback converter, the center of ramp of secondary side current is:

$$I_{\sec} = \frac{I_o}{1 - D_{\max}} \quad (3)$$

The primary side current is:

$$I_{pri} = \frac{I_{\sec}}{N_{ps}} \quad (4)$$

When the transistor turns on, the primary current I_p increases at a rate specified by:

$$\frac{di_p}{dt} = \frac{V_{in}}{L_m} \quad (5)$$

The leakage inductance on the primary side of the transformer is given by:

$$L_{leak} = (1 - k)L_m \quad (6)$$

Where, k represents the coupling coefficient of the coupling inductors.

The output filter capacitor is:

$$C_o \geq \frac{D_{\max} P_{out}}{F_{sw} V_{out} \Delta V_{out}} \quad (7)$$

Where, ΔV_{out} is the output voltage ripple.

B. Designing of LC snubber

The value of snubber capacitor C_{sn} is selected so as the peak drain-to-source voltage V_{ds} should not exceed a chosen limit $V_{ds,max}$, administered by the breakdown voltage of the transistor. Therefore,

$$C_{sn} \geq \frac{I_{pri}^2 L_{leak}}{[V_{ds,\max} - V_{in} - N_{ps}(V_{out} + V_f)]^2} \quad (8)$$

To minimize the influence of resonance, the time interval is limited to one half of the t_{on}.

$$\frac{t_{on}}{2} \geq \pi\sqrt{L_{sn}C_{sn}} \quad (9)$$

The snubber inductance is calculated as:

$$L_{sn} \leq \frac{(t_{on}/2)^2}{\pi^2 C_{sn}} \quad (10)$$

C. Maximum ratings of MOSFET and diodes

The maximum value $V_{ds,off}$ in OFF state is [15]:

$$V_{ds,off} = V_{in} + \frac{(V_{out} + V_f)}{N} + I_p\sqrt{\frac{L_{leak}}{C_{lump}}} \quad (11)$$

The maximum reverse voltage across the output diode D_o can be calculated as:

$$V_{do,off} = V_{out} + \frac{V_{in}}{N_{ps}} \quad (12)$$

The maximum reverse voltage across the snubber diodes D_1 and D_2 can be written as:

$$V_{d1,off} = V_{d2,off} = V_{in} + \frac{(V_{out} + V_f)}{N_{ps}} \quad (13)$$

D. Designing of feedback system

State-space averaging method is used to design the feedback controller for the proposed design. The block diagram of the closed loop control system is shown in Fig. 2. The pulse of switch gate is controlled by ideal controlled voltage. The output voltage is compared with a reference value and the generated error signal is applied to the compensator block. The output of the compensator is fed to the controlled voltage source. This block is capable to maintain a specified voltage at its output regardless of the current passing through it and its output is given to the PWM generator which feeds the switch gate.

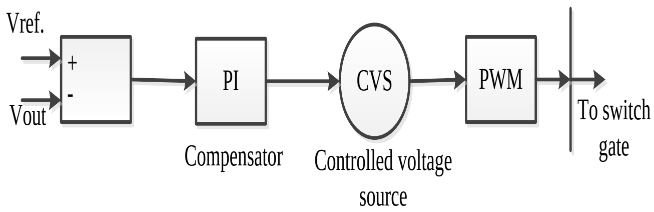

Fig. 2. Closed loop control diagram

IV. Simulation Results And Analysis

To make the analysis simple, the following assumptions are made in this study:

- The coupling coefficient of the coupled inductors is taken as 0.99.
- The coupled inductors are ideal; only the leakage inductance is considered.
- MOSFET parameters are taken from a datasheet. The gate-drain capacitance is kept constant and the model is independent of temperature variations.
- The voltage drop across the diodes are taken as 0.5V.
- The inductors and the capacitors are taken as ideal.
- The output filter capacitance is large enough to keep the output voltage constant.

The simulation time is taken as 5msec and the maximum step size is 0.1µsec. The system parameters of the designed circuit are given in Table IV. The potential applications of the model are RF power, piezo actuator and small DC motor.

TABLE IV
Design Parameters

S.No.	Parameter	Symbol	Value
1	Turns ratio	N_{ps}	1/3.5
2	Magnetizing inductance	L_m	0.6µH
3	Leakage inductance	L_{leak}	6pH
4	Snubber capacitor	C_{sn}	53.4nF
5	Snubber inductance	L_{sn}	1.25µH
6	Output capacitor	C_o	100µF

A. Transient Analysis

In this study, transient analyses are divided into start-up and switching transients.

Start-up Transients: It is common that DC-DC converters draw huge amounts of input current at start-up. It is clearly indicated in Fig. 3. The maximum input current touches the limit of 75A. The designed converter takes 330µs to acquire the steady-state.

At this time, the output voltage extents to its desired value. Although, soft-start circuits are usually employed in the power supplies at the input side to reduce the inrush current but it increases the cost and include extra time to extent the specified output voltage. The introduction of the start-up circuit depends on the customer requirements.

In our designed example, the selected components are capable of withstanding the starting inrush current. Due to limited start-up time, no start-up circuit is included in this design.

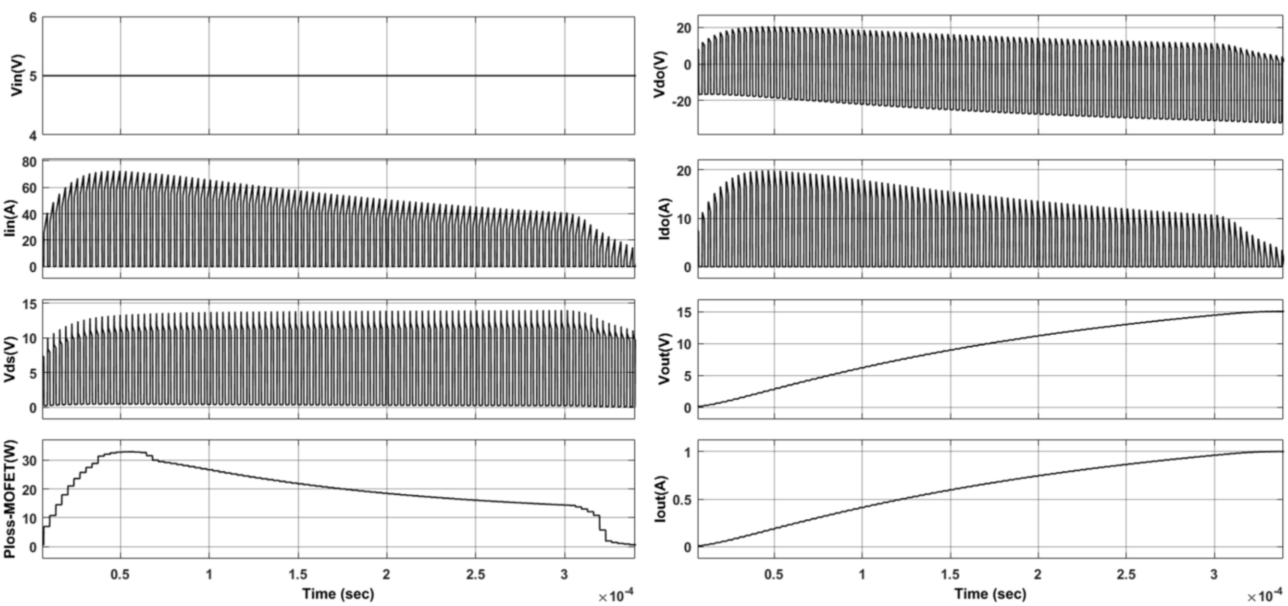

Fig. 3. Start-up transient waveforms

Switching Transients: When the transistor turns off, the voltage $V_{ds,off}$ reaches from 0V to a value given by (11) and appears across the parasitic C_{oss}. It takes very short time due to small value of C_{oss} and large primary current. A resonance occurs between L_{leak} and C_{oss}. After the resonance period, $V_{ds,off}$ changes from (11) to (14):

$$V_{ds,off} = V_{in} + \frac{(V_{out} + V_f)}{N_{ps}} \quad (14)$$

Transients also occur when the transistor gets a turn on pulse and continue during this period. The voltage V_{ds} gains some value due to presence of parasitic in the circuit components and is shown in Fig. 4.

B. Steady-state Analysis

To make the steady-state analysis, the operating modes are divided into four time slots to describe a complete switching cycle. The steady-state waveforms of all important parameters and circuit schemes of all operating modes are shown in Figs. 5 and 6, respectively.

Mode 1 ($t_o \leq t \leq t1$): The switching cycle starts when the transistor is just turned on. Prior to time $t=t_o$, the voltage across snubber capacitor C_{sn} has some positive value and stored energy in the magnetizing inductance L_m is transferred to the output. The current through output diode D_o falls to zero simultaneously at the start of this mode under ZCS.

At $t=t_o$, the transistor turns on. The current in magnetizing inductance increases linearly and the energy is stored in the transformer. During this mode, C_{sn} discharges first and transfers the energy to the L_{sn} and after then charges. The current through L_{sn} increases almost linearly first and decreases after some time.

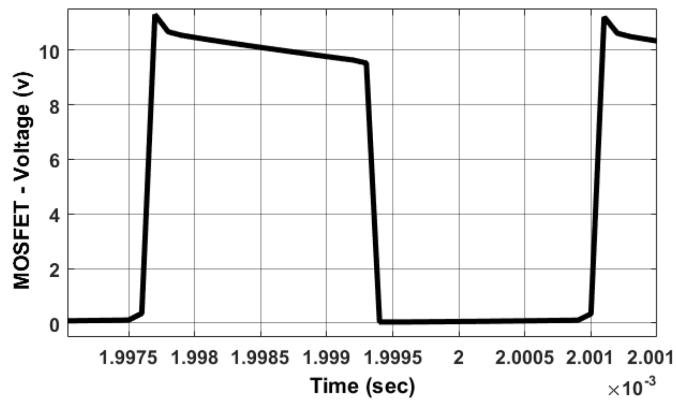

Fig. 4. Switching transients

Mode 2 ($t_1 \leq t \leq t_2$): During this mode, the transistor remains ON and the output diode D_o is reverse biased. The current through L_m increases linearly, while the current through L_{sn} is zero. The diode D_o remains OFF during this mode. The voltage across C_{sn} clamps at some negative value. This mode continues till the turn off pulse is applied.

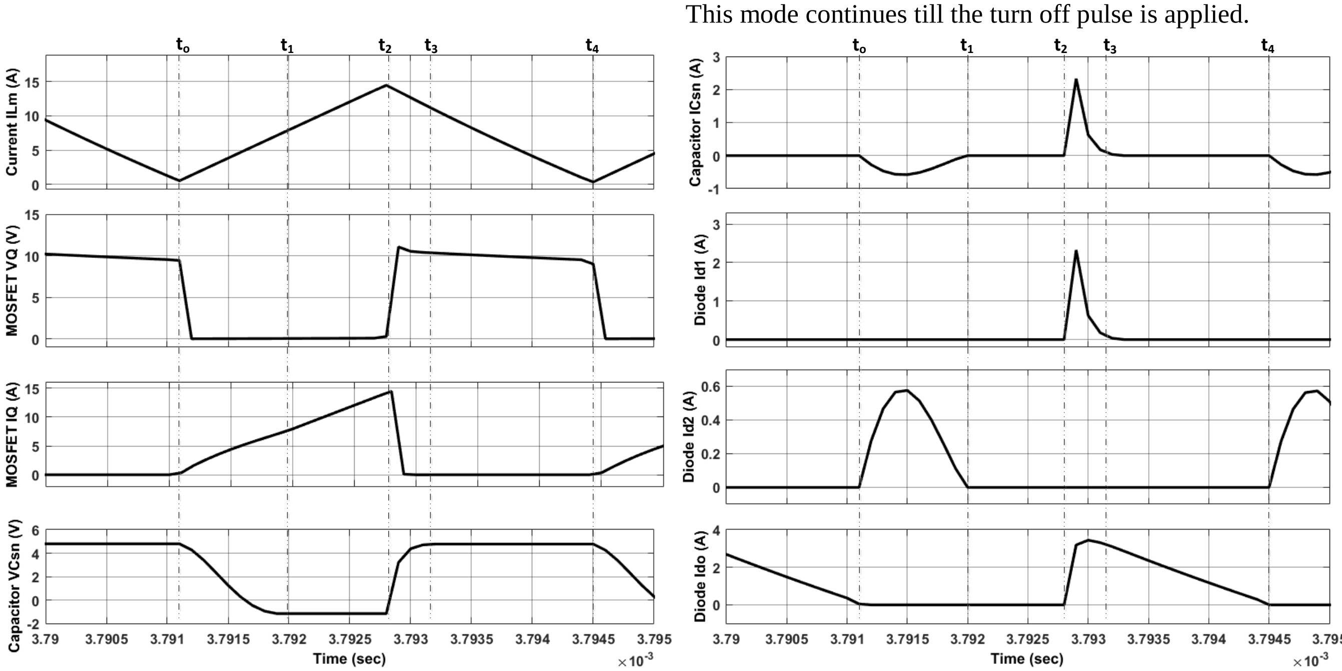

Fig. 5. Steady-state waveforms

Mode 3 ($t2 \leq t \leq t3$): During this operating mode, the transistor turns off under ZVS. The voltage across the transistor parasitic C_{oss} reaches from 0V to a value given by (11). It takes very short time due to small value of C_{oss} and large primary current. A resonance occurs between L_{leak} and C_{oss}. The resonant circuit is composed of C_{oss}, L_{leak} and L_m. The capacitor C_{sn} is charged quickly through the stored energy of the leakage inductance. After the resonance period, the $V_{ds,off}$ changes from (11) to a value, given by (15).

$$V_{clamp} = \frac{(V_{out} + V_f)}{N_{ps}} \tag{15}$$

This energy transfers back to the source due to large value of the snubber capacitor. The energy stored in the magnetizing inductance transfers to the output side. In this time interval, diode D_1 starts to conduct and continues till the voltage across C_{sn} clamps at some positive value given by (15).

This mode ends when the diode D_1 stops to conduct.

Mode 4($t_3 \leq t \leq t_4$): In this mode, the transistor remains OFF and the current through L_m continues to decrease. The output diode D_o remains in conducting state and delivers the energy to the load till the end of this stage. The snubber diodes D_1 and D_2 are reverse biased. This mode ends with the start of the next switching cycle.

C. Transistor ZVS/ ZCS

The designed circuit achieves the ZVS/ZCS of the transistor (Fig. 7).

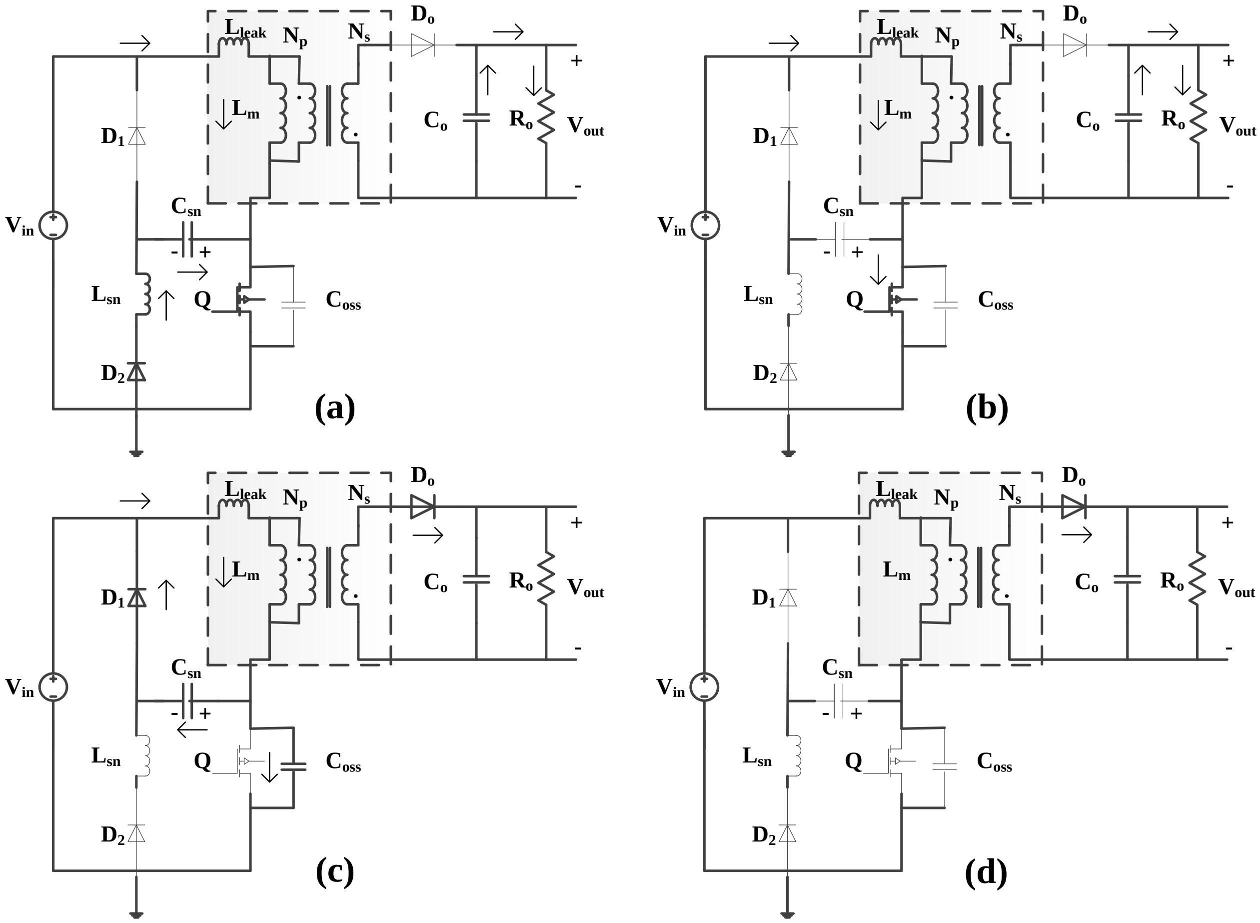

Fig. 6. Equivalent circuit schemes of the operating modes: a) Mode 1, b) Mode 2, c) Mode 3, d) Mode 4

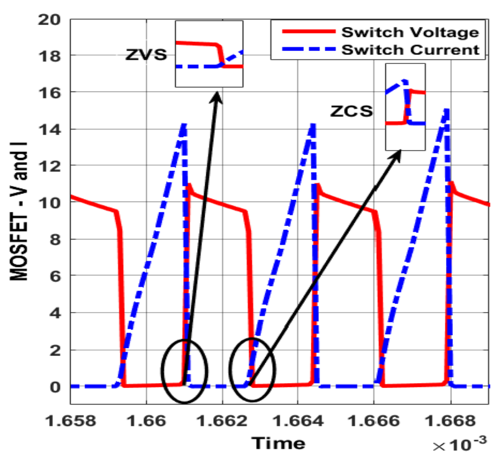

Fig.7. Transistor ZVS/ZCS

D. Transistor power loss

The proposed design significantly reduces the transistor power loss. The power loss is high during the start-up period due to high input current, nearly 33W and gradually decreases (Fig. 8). After 330µs, when the output voltage reaches to its final value, the power loss reduces to 0.7W or less afterwards.

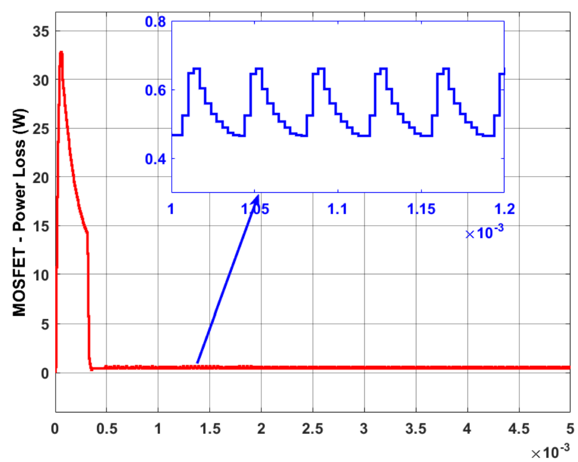

Fig. 8. Transistor power loss

V. CONCLUSIONS

In this study, an LC snubber circuit was employed with a single switch PWM flyback converter to reduce the voltage spikes and power loss. ZVS/ZCS operation of the transistor was made possible through the snubber circuit. The proposed LC snubber circuit was capable to recycle and transfer the energy stored in the transformer leakage inductance to the input side. The design methodology, operating principles and comprehensive analyses of the proposed design have done. A 15W, 15V/1A CCM flyback converter with an LC snubber circuit was designed and simulated. The results demonstrated that all the desired objectives met with the application of an LC snubber circuit.

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