Modeling of nonlinearities in MMC stations for real-time and offline simulation

S. Dennetière, H. Saad, J. Mahseredjian, T. Ould-Bachir

***Abstract*—Multilevel Modular Converters (MMCs) are used in several HVDC projects around the world. Several hundreds of levels are commonly used in MMCs. Detailed modeling of converters has been demonstrated in offline and real-time tools, but several solutions are still under development to improve accuracy and performance of models. This paper focuses on modeling of nonlinear components in MMC station: surge arresters, transformer magnetization and switching valves. It presents an MMC based benchmark for demonstrating accuracy needs in the simulation of MMC stations with nonlinearities. The proposed benchmark is used to validate real-time simulation results in comparison with EMT offline solutions. It shows the compromise between computation speed for real-time constraint and simulation accuracy in the presence of nonlinear devices.**

***Index Terms*—Real-time simulation, nonlinear systems, HVDC, Modular multilevel converter (MMC), Voltage-Source Converter (VSC).**

I. Introduction

The modular multilevel converter (MMC) topology offers significant benefits compared to previous voltage source converter (VSC) technologies. To study the global performance of MMCs in a grid, real-time simulation tools with actual controllers in the loop (Hardware In the Loop – HIL) are frequently used by HVDC manufacturers and owners. The main advantage of real-time simulation in this context is to validate the real controllers under various network conditions.

MMC modeling in electromagnetic transient type (EMT-type) tools is very challenging, because of the large number of semiconductors used in such converters. This constraint usually imposes numerical integration time steps of a few µs and large amounts of I/Os. Several MMC models for EMT studies are presented in [1]. MMC models for real-time simulation are proposed in [2]-[8]. Compared to EMT offline simulation, HIL simulation offers great opportunities for performing detailed EMT studies with actual controls. But real-time electromagnetic transient simulation has always been a compromise between computation speed for real-time constraint and simulation accuracy. As a consequence, nonlinearities are often neglected or simplified to meet the real-time constraint especially when small time steps are used. In most real-time applications with HVDC controls, this simplification is acceptable. For instance, the nonlinear characteristics of surge arresters are usually not modeled in the real-time simulation of HVDC-LCC (Line Commutated Converter) type controls, since they have limited impact during ac and dc faults. This is not necessary the case for HVDC-MMC link. Modeling MMCs in real-time has been addressed in many papers, however, to the authors' best knowledge, the nonlinear characteristics of components in MMC-HVDC links have not been accounted for and their impact on simulation accuracy has not been analyzed.

This paper presents an MMC-HVDC link benchmark for analyzing accuracy issues under various conditions. Validation is based on an accurate offline EMT-type iterative solver. It is shown that without iterations, real-time simulation results may become less accurate, but the iterative solution requires more computing time and consequently there is a tradeoff between accuracy and computing time. This issue is especially complex when actual MMC controls are inserted in the simulation loop because they require very small time steps. This is due to the high sampling rates of controllers used to efficiently balance capacitor voltages of hundreds of submodules in each arm. Models implemented on FPGA boards are usually required in this context. A mixed platform composed of FPGA and CPU increases further the complexity of real time simulation. The communication latency between CPU and FPGA may lead to numerical issues and compromise model accuracy. This paper proposes and tests simplifications (compromises) to accurately solve MMCs on such platforms. The main compromise is to avoid iterations to solve switching states in converter arms.

Part of the work presented in this paper has been performed in the context of the INELFE (France-Spain ELectrical INterconnection) interconnection. This 2,000 MW interconnection is composed of 2 parallel HVDC-VSC links including 4 XLPE cables (64.5 km long each).

This paper starts with a description of nonlinear devices involved in an MMC station. The proposed arm model switching state calculation simplifications for avoiding iterations in real-time, are presented next. A brief overview on iterative solution techniques presently available in real-time simulation tools is presented in section III. Section IV provides practical test cases that demonstrate the impact of accurate modeling of nonlinear devices in converter stations.

II. Nonlinearities in MMC stations

A simplified single line diagram of an HVDC link composed of 2 MMC converters and dc cables is presented in Fig. 1.

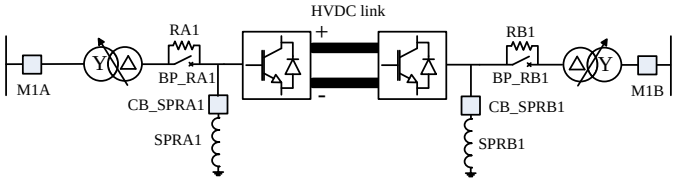

Fig. 1 Simplified single line diagram of an HVDC link with MMC

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The number of I/O signals and the sampling rates used by the VSC controllers are the main constraints imposed on real-time simulators. For one HVDC link similar to the INELFE interconnection, the number of I/O signals is greater than 10,000. The sampling time for low level controls is below 10µs for such converters as explained in [2]. The sampling time plays an important role on the dynamic performance of the system.

A. Switching devices

1) MMC models for EMT simulations

Various EMT-type models for MMCs have been presented in [1]. Model 1 is the most detailed. It models the nonlinear characteristics of diodes and IGBTs, requires an iterative solver and consequently causes very high computing times. This model is not suitable for real-time simulation, but it can be used to validate and calibrate simplified models.

Model 2 [1] avoids the nonlinear IGBT and diode models through the usage of switchable resistances (Ron/Roff). This approach allows performing a converter arm circuit reduction for eliminating internal electrical nodes and uses a Norton equivalent for each MMC arm. The model still considers each submodule (SM) separately and maintains a record for each individual capacitor voltage. In [1] and [3] an iterative process is activated during the SM blocking state to obtain accurate results. EMT studies with detailed controls can be performed with this type of model. For MMCs with large number of levels (251 levels and more), the calculation time step shall be smaller than 15µs [2] to respect the smallest time interval between two different levels and actual low level controllers usually need a sampling rate below 10µs.

In Model 3 [1] each arm is averaged using the switching function concept of a half bridge converter. This model assumes that capacitor voltages of each arm are perfectly balanced. Real-time implementation of this type of model has been proposed in [6] and [7]. Second harmonic circulating current controllers can be tested with this type of model. But it is not possible to test capacitor voltage balancing controllers. Some solutions have been proposed to implement Model 3 interfaced with detailed arm model to overcome this limitation [9].

Model 4 [1] is the classical average value model. It is not suitable for interfacing with real MMC controls because several controls loops cannot be tested with this type of model.

2) MMC models for real-time simulation

Model 2 is currently the best candidate for real-time implementation on CPU and FPGA. Due to time-step constraints imposed by real-controllers to efficiently balance capacitor voltages, FPGA implementation is required. Accurate solutions must be found without iterations with the electrical network nodal equations. These constraints are analyzed in this section.

A Model 2 implementation for real-time is proposed in [2] but it does not support the blocking state. A Model 2 implementation is also proposed in [3], but iterations with the nodal equations are required to get correct results. Implementation on FPGA of this solution is not feasible with the currently available hardware technologies due to communication latency between CPU (electrical circuit nodal solution) and FPGA (arm model).

The computation of ON/OFF states is a straightforward process since only gate signal values are required. When the blocked state is set (i.e. no gate signal is sent to IGBT), only the freewheeling diodes can conduct. The diode conduction states depend on voltage and current variables. The discontinuities in state variables due to the blocked state can cause numerical oscillations. This issue is addressed through an iterative process for offline simulation in [1]. To apply a similar iterative process in real-time, CPU implementation cannot currently meet the calculation time constraints. FPGA implementation is required. But FPGA implementation must include all component models in the converter station with the solution of nodal equations and refactorization at each solution time-point. New high performance sparse matrix solvers have been proposed on FPGA [10], but implementation of such computationally demanding EMT models on FPGA remains complex and requires further research. A non-iterative approach is proposed below.

The SM states for blocking mode are presented in Fig. 2. When the arm current is positive, the diode D1 conducts and the SM is in ON state. The diode D2 voltage is positive and equal to the capacitor voltage. When the current decreases and crosses zero, D1 stops conducting. Then, depending on D2 voltage, D2 can conduct (the SM is in OFF state) or stay in blocked state (the SM is in high impedance – HZ – state). During this commutation, the D2 voltage waveform and its impact on D2 state change depend on many parameters such as the external circuit connected to the arm (arm inductance, cables…) and the rate of rise of the arm current. In some cases, the SM goes from ON state to OFF state without passing in HZ state. In other cases, the SM goes from ON state, to HZ state for few ms and then goes to OFF state.

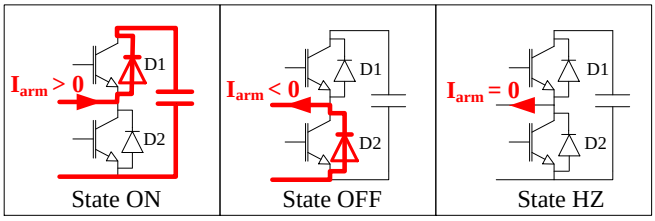

Fig. 2 SM states for blocking mode

When iterations are not performed to find the correct state, a solution is to force the arm current used to update the model, to zero during one time-step when current crosses zero. This is equivalent to forcing the HZ state during one time-step. This solution has been implemented in the paper.

The discretized equivalent circuit for each SM is presented in Fig. 3 (see also [1]). The state of each submodule is selected based on arm current direction and diode voltages (V_{D1}^{i} and V_{D2}^{i}). Therefore this selection can be determined from arm current I_{arm} and the equivalent current history source of capacitor I_{ci}^{h}. The arm model is reduced into a Norton equivalent ($R_n(t)$, $I_n(t)$) as presented in [1], and updated at each solution time point based on the calculation of each individual cell.

When the zero current crossing is detected, the arm current

is set to zero. This setting forces all SMs in the arm to be in HZ state. The following steps are performed at each time-step for the proposed model:

1. Get Pulses(t) and $V_{arm}(t)$
2. $I_{arm}(t) = V_{arm}(t)/R_n(t-\Delta t) + I_n(t-\Delta t)$
3. If at least 1 SM is blocked goto 4, else goto 6
4. If $I_{arm}(t)*I_{arm}(t-\Delta t)>0$ goto 6, else goto 5
5. $I_{arm}(t)=0$
6. For each SM: select state based on $I_{arm}(t)$ and $I_{ci}^h(t-\Delta t)$
7. Solve nodal equations, next time step and goto 1

Step 3 is only done when the arm was not in HZ state at the previous time point and when the arm was blocked (no pulse received).

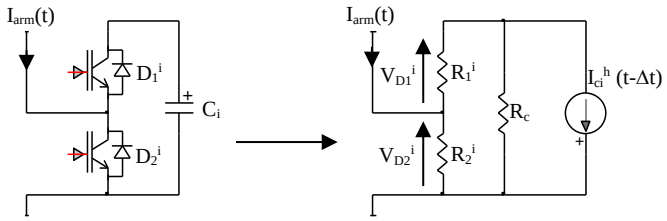

Fig. 3 Discretized equivalent circuit for ith submodule

The reduced voltage (320 V, 50 Hz) test system presented in Fig. 4 is used to compare the simulation results of the proposed arm model against the offline EMTP Model 2 presented in [1] which includes an iterative process. In Model 2 the trapezoidal integration rule is switched to the Backward Euler (BE) method for the next time point solution for eliminating numerical oscillations [11] caused by discontinuities in trapezoidal integration. EMTP Model 2 is the reference model used to validate the proposed model.

In Fig. 4, the arm is composed of 5 submodules. The proposed model uses the BE integration method with a 30 µs time step in this case. BE is used here to avoid numerical oscillations and it is sufficiently accurate when the integration time step is small.

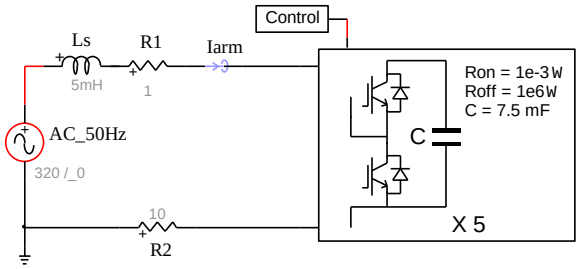

Fig. 4 Simple test circuit for comparing arm models

The arm is de-blocked between t=0.1s and t=0.2s. The arm current is presented in Fig. 5 and Fig. 6. The voltage of the first capacitor is presented in Fig. 7.

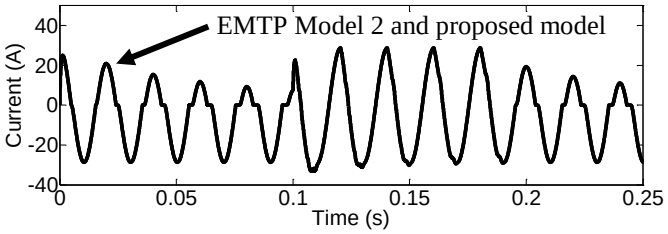

Fig. 5 Arm current of the simple test case in Fig. 4

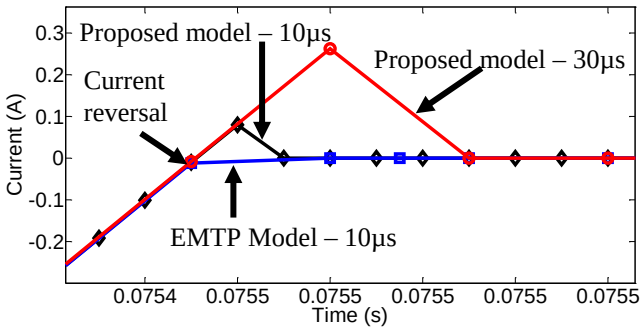

Fig. 6 Arm current (Zoom of Fig. 5) during blocking state

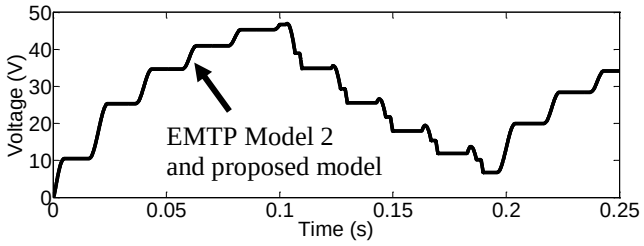

Fig. 7 Voltage of the first capacitor

Both models give similar results. The only differences are noticeable at zero current crossing (small spike), as presented in Fig. 6. When current reversal is detected, the arm current used in the arm model is set to zero to quickly account for state change (from ON/OFF to HZ) in the calculation of I_{ci}^h. The arm current resulting from the Norton equivalent provided to the nodal solution is not zero because it is deduced from the nodal solution at the previous time step. Fig. 6 compares simulation results performed with 30µs and 10µs time steps. It demonstrates that when the time step is smaller, the solution is more accurate, as expected.

B. Surge arresters

Surge arresters are located on the dc and ac sides. The dc side arresters are shown in Fig. 8.

When dc fault occurs at converter terminal (see fault location in Fig. 8), pole-to-ground overvoltage on the healthy pole can be observed due to the converter topology.

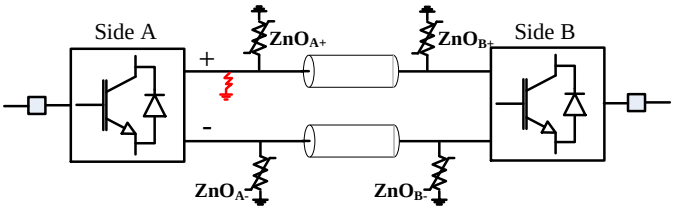

Fig. 8 Pole-to-ground fault location and dc side arresters

Due to the symmetrical monopole configuration, no

reference to ground is available on the dc side. A ground fault on one pole will shift the other pole to about twice the dc voltage. To limit the overvoltage on the healthy pole, the following solution is usually implemented (see Fig. 8).

First, the severe healthy pole overvoltage is limited by surge arresters installed on the dc pole bus as explained in [12]. These special surge arresters have a very high energy absorption capability because the overvoltage can last several tens of ms. This transient is similar to a temporary overvoltage because it lasts 2-5 cycles. Second, the converters are blocked immediately (~ 40 µs after fault detection) and the ac circuit breakers at point of connection (point of common coupling - PCC) are opened after 2-5 cycles.

The surge arresters are designed to limit the dc overvoltages and absorb a significant amount of energy before the ac circuit breaker opening. Large currents are driven to ground by the surge arresters when limiting the dc overvoltages. The protection levels of arresters for this application are typically around 1.8 pu.

For testing actual (real) controls with dc faults, the surge arresters must be modeled. This need increases the real time simulation complexity because a time step typically smaller than 30µs (due to the controller sampling rate) must be used and the nonlinear characteristics of surge arresters must be treated with iterations.

The presented test case (see Fig. 1) includes delta connection on secondary side of transformers. Some VSC solutions [13] use Y/Y configuration (instead of Y/D) where the converter-side star point is ungrounded. In this case, pole-to-ground faults lead to overvoltages at cable terminals and also at the converter side star point of transformer, which is protected by a surge arrester. As a consequence, similar numerical challenges exist in this configuration and the impact on accuracy of the iteration solver with surge arrester is addressed in the next section.

C. Transformer saturation

HVDC converter stations consist of power converters, transformers, cables/lines and filters (in some cases) are characterized by low impedance paths. When converter stations are energized, they may cause a large inrush current due to capacitor charging and energization of transformer and cables. This results in system voltage distortion, undesired harmonics and overvoltages leading to potential malfunctioning of protection equipment, equipment failures and non-compliance with the grid codes.

Insertion resistors are usually installed to limit inrush currents during converter energization. In [14] pre-insertion resistors are installed on the grid side (primary side of converter transformers) to limit transformer and capacitor inrush currents. In the proposed test system, the pre-insertion resistors are installed on the converter side (see RA1 and RB1 in Fig. 1). This solution is effective to limit capacitor inrush currents, but not transformer inrush currents.

The Point-On-Wave (POW) controllers is implemented on the ac circuit breakers (M1A and M1B in Fig. 1). This solution can provide several technical and economic benefits, but may not be reliable on the long term to limit inrush currents (controller failure, variation of the circuit breaker mechanical performances…).

In the proposed test case (Fig. 1), converter transformers are composed of 3 single phase units of 350 MVA each. Each single phase unit has 2 wound legs and 2 unwound legs. This type of core provides a magnetic path for zero sequence flux, but can have remanent flux when the transformers are switched off. The POW controllers implemented on site do not take into account remanent flux in the calculation of the switching times [17].

That is why the HVDC control and protection systems must be tested by taking into account high inrush currents. Therefore, magnetization branch of transformer, should be included in the model to study such inrush current.

D. High impedance grounding devices

High impedance grounding devices (named star point reactor in the present converter station) are installed between transformer secondary side and ac side of converter arms to provide a reference to ground. This equipment does not provide a strong reference to ground, because its impedance is very high (several thousand of Henry) but it can be used to detect any voltage unbalance generated by a dc fault [12]. In some cases (high impedance dc fault analysis) the saturation of this device must be modeled.

III. Iterative Solutions for Nonlinear Functions in Real-Time Simulations

This section briefly describes the numerical techniques used to solve nonlinearities in real-time simulation tools. These techniques have been recently implemented in the eMEGAsim [18]-[19] and Hypersim [20] real-time simulators. Simulation results have been compared and validated against results given by the offline simulation tool EMTP [22]. EMTP uses a fully iterative and simultaneous solver for all nonlinearities.

Since transmission lines introduce decoupling in the network solution, the subnetworks separated by transmission lines can be identified and solved independently. This is the traditional method to perform parallel processing in real-time. Hypersim and eMEGAsim tools provide an iterative solver adapted to real-time simulation. They use an iterative setup within each subnetwork that includes nonlinear models. Surge arresters are modeled by piecewise linear resistors. Each segment j is represented by a linear equation of current i_j as a function of voltage v_j:

$$i_j = K_j v_j + I_{N_j}$$

which defines a Norton equivalent with admittance K_j and Norton current source I_{Nj}. Nonlinear devices are required to return their discretized Norton equivalent through linearization at the given operating point for each iteration. After each nodal solution, the nonlinear models retrieve back their voltages to identify which segment of the nonlinear characteristic is active. If the current segment is different than the previous one, the nodal admittance matrix of the subnetwork is updated with the new segment and re-factorized within. The Norton current vector is updated as well. The iterative process ends when convergence is achieved. When the iteration process requires

too much time for real-time simulation, mitigation solutions must be used, such as reducing the convergence precision condition in order to decrease the number of iterations and meet the real-time constraint. eMEGAsim uses a combined State-Space Nodal Method proposed in [18] to account for nonlinearities.

IV. Test Cases on a Real MMC Installation

The France Spain HVDC interconnection is used here as an application example. Converter, transformer and cable data is available in [15]. Surge arrester data is provided in [16].

As explained in [2], real-time simulation of MMC models with more than 161 levels can only be achieved with FPGA-based models due to computation effort. The arm model presented in section II.A.2) has been implemented on an FPGA and integrated into the Hypersim platform. Real-time simulation requirements are fulfilled here for a 401 level converter. To model converters with such high number of levels, gating signals cannot be generated on a CPU due to the number of I/Os and the latency between CPU and FPGA. The solution is to implement the balancing algorithm that generates the gating signals on an FPGA. It can be implemented on the same FPGA used for the valve models or on an additional FPGA (actual controller). This solution has been initially tested in [2] and improved in [21]. It drastically reduces the number of I/Os and makes the interface much simpler on the CPU. Only 6 reference voltages are sent to the FPGA by the CPU at each time step. This limited number of I/Os enables the use of smaller time steps on CPU and thus modeling of converters with high numbers of levels.

The simulation setup for 1 converter station is presented in Fig. 9. The complete setup is composed of 2 converter stations and 2 dc cables. The converter model is solved on CPU with a 20µs time step (trapezoidal integration method). The arm models are solved on FPGA with a 1.25µs time step and using Norton equivalent (or Thevenin equivalent). The balancing algorithm is executed on FPGA at 5µs.

The electrical circuit solved on CPU is independent from the number of submodules in each arm. The conclusions drawn in this paper regarding the modeling of the presented system with-nonlinearities, are applicable to converters with various numbers of levels.

A total of 11 surge arresters are modeled with nonlinear resistors. The nonlinear characteristics are composed of 10 segments. The characteristics of the surge arrester connected to the dc cables are provided in [16].

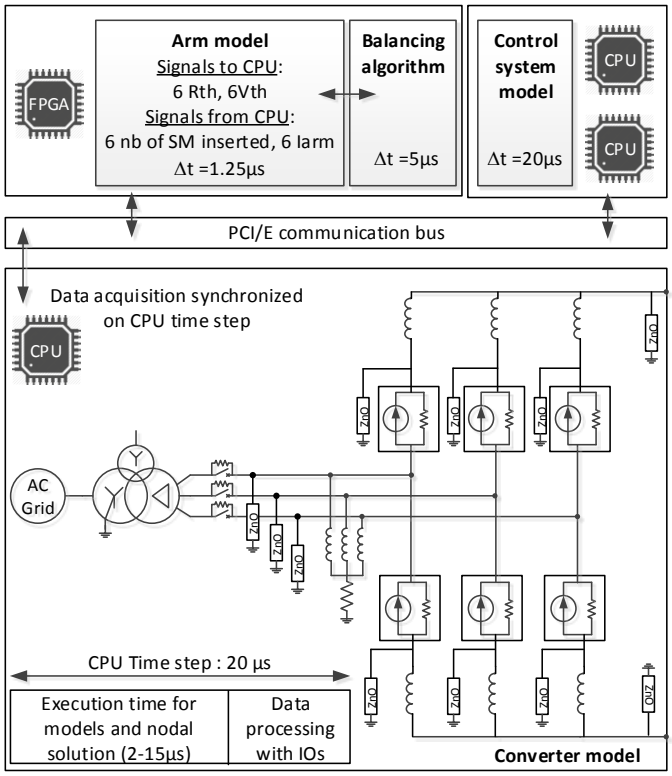

Fig. 9 - Converter station model implemented in Hypersim (CPU and FPGA)

A. Converter starting sequence

The start-up process of the MMC consists in charging equally all the capacitors before being able to operate. Moreover, current and voltage stresses in the power switches and on the ac grid have to be limited during start-up [23]. The first step of the starting sequence is the passive energization of the converter station and the dc cables. The sum of capacitor voltages in upper arm phase-a is presented in Fig. 10 :

1. ac circuit breaker (M1A) closing at t=0.1s
2. insertion of resistor RA1 bypass at t= 0.5s.
3. ac circuit breaker M1B closing at t=2s.
4. insertion of resistor RB1 bypass at t=4s.
5. converter de-blocking, send pulses to control dc voltage and start full power transmission at t=3s.

The start-up sequence is a relevant test case to validate the arm model and especially the blocked state condition. The upper arm current in phase-a of converter Side A is presented in Fig. 12. Simulation results are similar between the proposed model (without iterations) and the offline model (with iterations). The impact of the proposed arm model simplification during current zero crossing is negligible during the start-up sequence. The differences between real-time and offline results are identified with the letter ε (relative error).

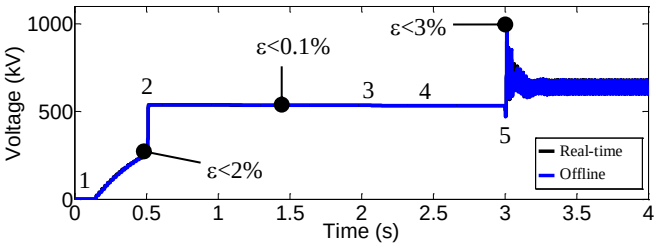

Fig. 10 Sum of capacitor voltage in upper arm during starting sequence

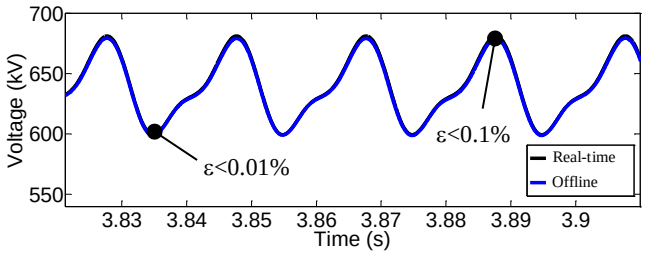

Fig. 11 Sum of capacitor voltage in upper arm during starting sequence (Zoom)

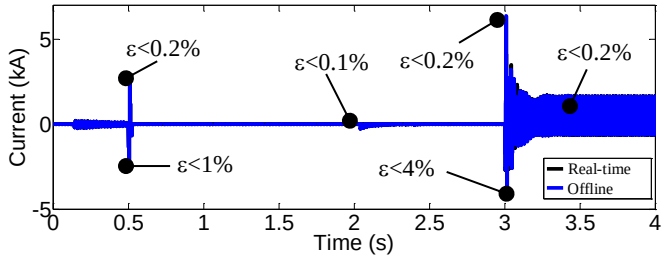

Fig. 12 Lower arm phase-a current during start-up sequence

B. DC bus faults

The objective of this section is to analyse DC pole to ground fault with converter blocking and surge arresters.

The pole to ground fault presented in Fig. 8 is simulated with surge arresters included and the converter is blocked when the dc fault is detected. The MMC Side-A converter is blocked 6.18 ms after fault ignition (over-current protection) and ac circuit breakers are opened 2 cycles later. The system presented in Fig. 9 is configured in the STATCOM mode (i.e. dc cable disconnected – only Side A simulated) in order to get faster decrease in the non-faulty pole-to-ground voltage. This is the worst case in terms of rate of change for overvoltages. This configuration in STATCOM mode has no impact on simulation performance because both sides are simulated on separated hardware (CPU and FPGA).

This test case is implemented in real-time and in offline with controls in the simulation loop. The controls are identical in both simulation tools. The following results are compared: EMTP results with arm and surge arrester models solved with iterations Hypersim results with only surge arrester solved with iterations (Norton equivalent for each arm is kept constant for each iteration, only surge arrester segments are changed); Hypersim results without any iteration. The voltages on the healthy pole are presented in Fig. 13 and Fig. 14.

The iterative solution of nonlinear characteristics necessitates increased computing efforts. For the test system presented in the paper (link or STATCOM configuration) the iterative process requires 3 times more computing time than a solution without iterations. The execution time of the test case with the starting sequence followed by a pole-to ground fault is presented in Fig. 15.

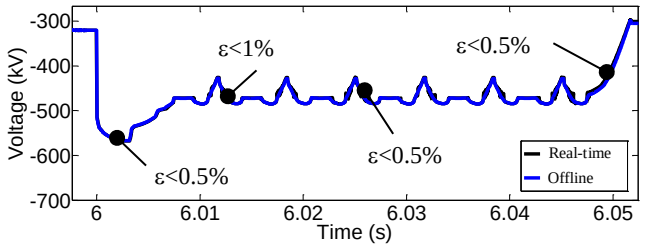

Fig. 13 DC voltage at converter terminals (healthy pole) during pole-to-ground fault – Comparison offline vs real-time with iterations

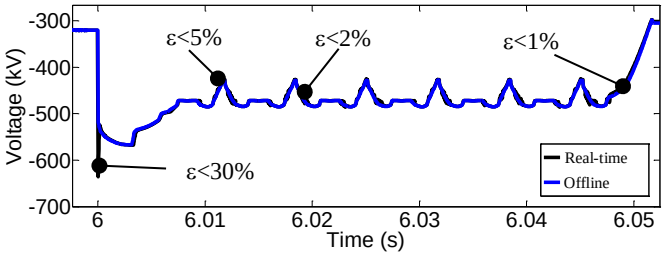

Fig. 14 DC voltage at converter terminals (healthy pole) during pole-to-ground fault – Comparison offline vs real-time without iterations

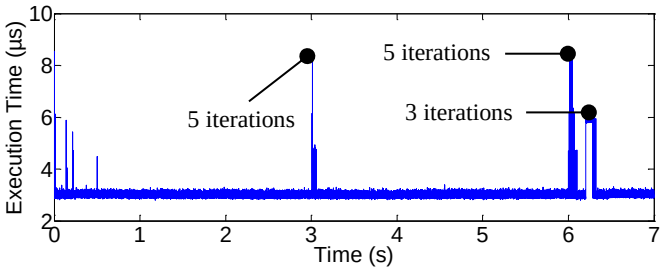

Fig. 15 Execution time in Hypersim with iterations

It is shown that without iterations, the overvoltage is over estimated by 30%, but the iterative solution requires more computing time. In the proposed test case, it is increased by a factor of 3 without leading to over-run in real-time simulation. There is a tradeoff between accuracy and computing time. In the proposed case, even if the simulation results are less accurate without iterations, they can be considered acceptable for many HIL applications. The inaccurate computation of overvoltages may, however, impact on the overvoltage protection system and produce erroneous results.

V. Conclusions

Study of MMC modeling including the nonlinear characteristics of components has been addressed in this paper. This paper describes and investigate the nonlinearities that must be taken into account in MMC station modeling. The proposed benchmark with its generic data is based on a real HVDC-VSC project.

This paper proposes and tests converter arm model simplifications (compromises) to accurately solve MMCs in real-time simulation tools. These compromises are mandatory to avoid iterations on mixed CPU-FPGA platforms within the required time-step limitations. The provided practical test cases

show that it is feasible to get sufficiently accurate results without iterations on the arm model.

It is shown that in the case of dc faults in converters, the iterative solution provides more accurate results. In the proposed test case, the overvoltage is over estimated by 30% when the iterative solution is not activated.

The accuracy analysis presented in this paper is part of an upstream research to ensure that real-time simulation platforms are suitable for modeling actual converter station installations and for interfacing with actual controller systems.

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