Effect of the Surge Arrester Configuration in MMC-HVDC Systems under DC and Converter Fault Conditions

Nicolas Manduley, Sellé Touré, Alain Xémard, Bertrand Raison, Serge Poullain

***Abstract*--Different surge arrester configurations are studied for a modular multilevel converter (MMC) in a symmetrical monopole configuration. Each configuration is analyzed under fault conditions including DC side faults and faults inside the converter station. The configurations considered are compared in terms of overvoltages, current levels and energy dissipation. It is found that the selection of the surge arrester parameters does not only depend on the overvoltage levels of the equipment, but also on the surge arrester configuration considered. The action of the surge arresters could result in higher longitudinal withstand voltage requirements of the arm reactors. Furthermore, special attention shall also be given to the possible low inductance loops created by the conduction of the arresters during a transient event.**

***Keywords*: Insulation coordination, HVDC, EMTP, VSC, MMC, symmetrical monopole, surge arresters, switching transients, temporary overvoltages**

I. Introduction

THE application of Voltage Source Converters (VSC) on High Voltage Direct Current (HVDC) systems generates more and more interest, especially with Modular Multilevel Converter (MMC) based technologies. This is mainly due to their multiple advantages [1], mostly in terms of performance, controllability and potentiality of developing large HVDC grids in the future.

Insulation coordination is a fundamental part of the studies of any electrical system. It ensures that the system and all equipment connected to it will be able to withstand, with an acceptable risk of failure, the different overvoltages they could be subjected to [2–4]. In the absence of overvoltage limiting devices the overvoltage levels, combined with the accepted risk of failure, result in high insulation requirements, which may lead to design complexity and significant increase on the total costs.

The installation of surge arresters is an effective way to limit the severest overvoltages of the system and reduce the insulation requirements of the equipment while ensuring that the risk of failure will remain within the acceptable limits. It is thus fundamental to understand the impact that surge arresters can have on the electromagnetic transients which can possibly occur on the system in order to adequately choose the arresters' characteristics and configurations that will have the most optimal performance protecting the system during transient events. In addition, it should be recalled that existing IEC insulation coordination standards cover exclusively AC [2], [3] and Line Commutated Converters (LCC-HVDC) [4] systems. There are no standardized procedures for MMC-HVDC systems.

Studies on transient voltage stresses in MMC-HVDC systems are presented in [5], [6] for DC pole-to-ground faults for configurations including DC pole and transformer arresters. In [7], several faults on the AC and DC side (including internal converter faults) are studied considering the DC pole surge arrester and a configuration including arresters inside the converter. In [8], a case with a particular surge arrester configuration based on the Transbay project is studied.

To go further, in the study presented in this paper, different surge arrester configurations are analyzed for a point-to-point symmetric monopolar MMC-HVDC station. Diverse fault conditions are considered to account for the slow-front and temporary overvoltages that could appear for each case, and thus analyze the impact that each configuration has on the system dynamics. Section II provides with the detailed description and the setup of the study cases. Section III analyzes the results in terms of the overvoltage, current and energy absorption levels obtained. The results are further discussed in section IV and in section V the main conclusions resulting from the analysis are presented.

II. Study Case Description and Setup

A. MMC-HVDC Architecture and Topology

For this study, a 401-level modular multilevel converter (MMC) in a symmetrical monopole and point-to-point configuration is considered and illustrated in Fig. 1.

An XLPE type cable is used for the link between the two stations and it is rated ±320 kV. One station is in power control mode, while the other is in DC voltage control mode. The

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Paper submitted to the International Conference on Power Systems Transients (IPST2019) in Perpignan, France June 17-20, 2019.

complete setup details are displayed in TABLE I.

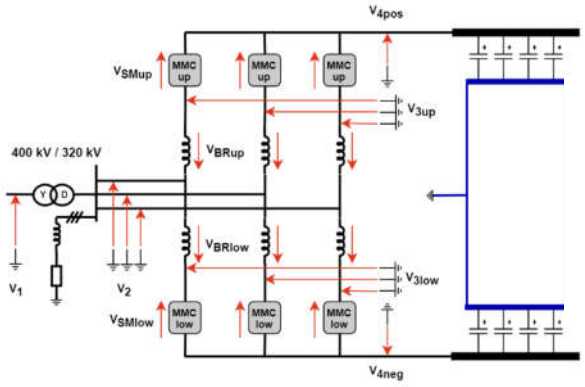


Fig. 1. Symmetrical monopole MMC-HVDC half-scheme with the different components for which the overvoltage levels are determined.

TABLE I
MMC MODEL SETUP AND PARAMETER CONFIGURATION

Parameter	Value
Rated power	1000 MVA
Primary AC voltage	400 kV (p-p rms)
Secondary AC voltage	320 kV (p-p rms)
DC pole to pole voltage	640 kV
Transformer reactance	0.18 p.u.
Arm reactor	0.15 p.u.
Capacitor energy	40 kJ/MVA (per submodule)
# of submodules per arm	400
Cable length	100 km (WB model)
Overcurrent protection	2 p.u.
MMC blocking delay	40 µs (EMTP native value)
AC breaker opening time	40 ms
Simulation step	1 µs

B. Fault Scenarios

The fault scenarios considered correspond to all the possible DC faults, and the faults inside the converter that could be more critical for the system. AC faults –outside the converter– are not considered in this study, and shall be considered in future work. See TABLE II and Fig. 2 for the detail of each fault considered.

TABLE II
FAULT SCENARIOS CONSIDERED

Name	Description
Fault I	Valve short-circuit
Fault J	Arm-to-ground fault
Fault K	DC bus-to-ground fault
Fault L	DC pole-to-ground fault at half cable length
Fault N	DC bus-to-bus fault
Fault N2	DC pole-to-pole fault at half cable length

C. Surge Arresters

The surge arresters considered for the different configurations studied in this work are also shown in Fig. 2. The locations have been chosen according to the fundamental insulation coordination rules and principles given in IEC standards for AC and LCC-HVDC systems [2–4] applied to MMC-HVDC systems. Though many other arresters could also be considered following these principles, such as those shown in [8], the arresters considered in this work have been chosen for being the ones that provide direct protection to the most critical points in terms of overvoltage, according to transient analysis, and without considering the longitudinal protection of the components. This way, it is possible to compare different combinations of these surge arresters and study their respective impact on the electromagnetic transients and their interactions.

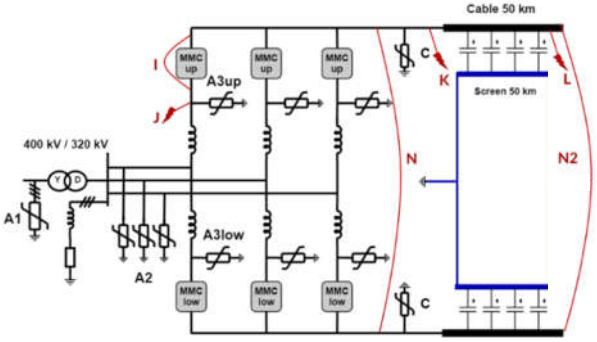


Fig. 2. MMC-HVDC scheme used for the simulations with the faults considered

IEC standards [2–4] state that overvoltages generated on the AC side shall be limited by arresters on the AC side, and idem for overvoltages generated on the DC side. Following this principle, arresters A1 and A2 are designed to play a more active role during AC faults on the primary and secondary side of the converter transformer, respectively. Similarly, arresters A3 and C are expected to play a major role in the overvoltage protection and energy dissipation in case of DC and converter faults, which are the faults considered in this work.

The surge arrester configurations considered are thus combinations of arresters A3 and C while arresters A1-A2 will be present in all configurations, as shown in TABLE III.

TABLE III
SURGE ARRESTER CONFIGURATIONS CONSIDERED

Name	Description
NS	No surge arresters
A1-A2	Transformer arresters
A1-A2-A3	Transformer and arm-to-ground arresters
A1-A2-C	Transformer and DC pole arresters
A1-A2-A3-C	All arresters considered

The initial parameters of the surge arresters have been determined differently for AC and DC side arresters, and are presented in TABLE IV for both the maximum continuous operating voltage (U_c) and rated voltage (U_r) of the arresters in their equivalent RMS value. The V-I matrix used is shown in Fig. 3 (obtained from [9]), and has been scaled to match the required rated voltage of the arresters.

All scenarios have been simulated in EMTP-RV [10] for each surge arrester configuration, giving a total of 30 study cases.

TABLE IV
RATINGS OF THE SURGE ARRESTERS USED FOR THIS STUDY

Arrester	**A_1**	**A_2**	**A_3**	**C**
Uc rms	288 kV	231 kV	248 kV	280 kV
Ur rms	360 kV	288 kV	310 kV	350 kV

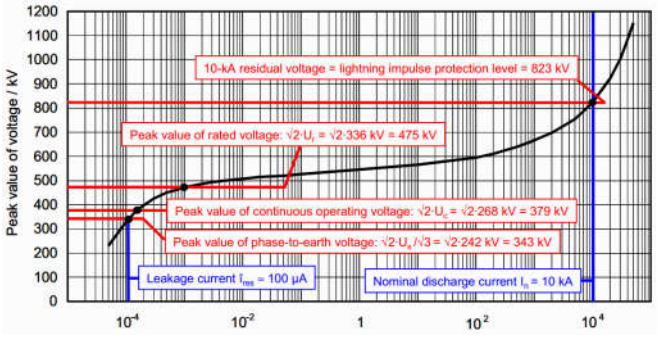


Fig. 3. V-I characteristic from which the base V-I matrix was obtained and scaled for each surge arrester used in this work (obtained from [9])

III. Results

The results of the simulations have been analyzed to determine the maximum slow-front and temporary overvoltages (SFO and TOV, respectively) for each component (see Fig. 1) and considering all studied faults (see Fig. 2 and TABLE II). The following paragraphs will present the results regarding overvoltage levels observed at each component, as well as the current levels generated and the energy absorption of the surge arresters.

A. Overvoltage Levels

For comparison purposes, the voltage levels obtained at each point and electrical component under normal operating conditions are summarized in TABLE V. All low frequency or transient voltages with higher amplitudes than these values were considered overvoltages and classified according to Table 1 in IEC 60071-1 [2]. The comparison of the maximum levels obtained for each component is illustrated in Fig. 4 for the SFO levels and in Fig. 5 for the TOV levels. The values are expressed in p.u., with 320 kV equal to 1 p.u.

TABLE V
Voltages measured for each component under normal operating conditions in per unit (1 p.u. = 320 kV)

Point	V1	V2	V3	V4	V_{SM}	V_{BR}
Voltage (p.u.)	1.04	0.88	0.90	1.01	1.90	0.08

It is observed that the SFO levels on the primary side of the transformer (voltage V1) are close to its normal operating voltage (i.e. around 1.04 p.u., see TABLE V), which means that the AC side is not significantly affected by the faults on the DC and converter side, as expected according to the insulation coordination principles previously mentioned. Also, no TOVs are transferred to the primary side of the converter transformer (Fig. 5).

It can be also seen that configurations A1-A2 and A1-A2-C are almost equivalent in terms of overvoltage limitation for both SFOs and TOVs, except at point 4 where the arrester C effectively limits the overvoltage levels on the DC pole. The same is observed for configurations A1-A2-A3 and A1-A2-A3-C, except that in this case the effect of arrester C is less important than in configuration A1-A2-C. This suggests that arrester A3 is more active in the overvoltage limitation, and/or that the protective level of arrester C is too high and could be lowered, if the minimum withstand voltage of the protected equipment allows it. Current levels under normal conditions and energy absorption levels will determine the feasibility of this possibility, along with the withstand levels of the DC cable.

Furthermore, it is observed that the SFO levels are higher for all points and equipment in the configuration without surge arresters (NS configuration), except for the arm reactors (Vbr in Fig. 4). In this case, the SFO levels are higher in all surge arrester configurations than in the base case without surge arresters. This is because when a surge arrester starts conducting, a new current path is created within the system. Consequently, the voltage distribution changes within the converter, as well as the voltage levels attained which could be different at each point, compared to the case without surge arresters. This concerns particularly the arm inductances, since they are the only components that are able to balance the voltage variation during the first instants after the fault.

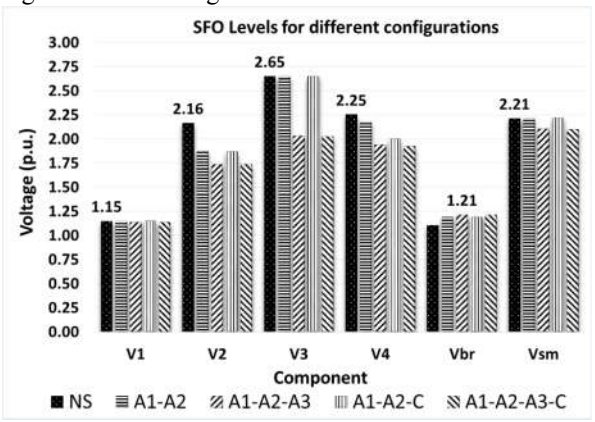


Fig. 4. Slow-front overvoltages (SFO) found for each considered component. The maximum value is indicated above the corresponding configuration.

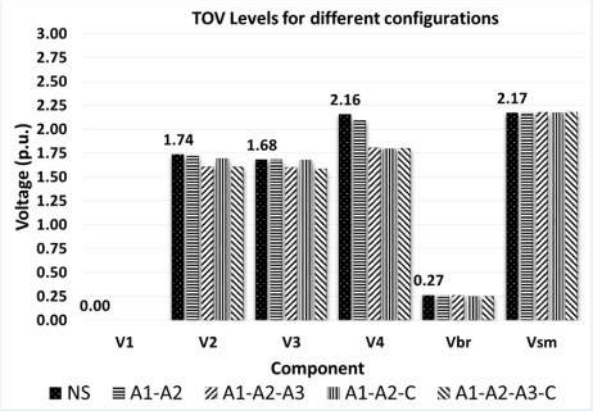


Fig. 5. Temporary overvoltages (TOV) found for each considered component. The maximum value is indicated above the corresponding configuration.

Special care shall be then taken to the possible loops created by the conduction of the surge arresters, as it could even create paths without limiting inductors, potentially resulting in very high currents through the IGBT valves and other equipment (an example of this is shown in the following section).

B. Fault Scenarios

TABLE VI and TABLE VII summarize the highest overvoltages obtained for each component for the configuration

without and with surge arresters, respectively, and the fault during which it was produced. When surge arresters are included, the overvoltage levels are significantly reduced, but the most critical faults are similar to the case without surge arresters.

It is observed in TABLE VI that fault I (MMC valve short-circuit) can generate significant overvoltages on the other valves (V_{SM}) and the arm reactors (V_{BR}). This is explained by the fact that, during such event, all the inserted capacitors inside the valve at the instant of the fault inception are abruptly discharged, resulting in a very high current (~100-200 kA) and voltage drop which will need to be taken by the arm reactors.

TABLE VI
MAXIMUM SFO AND TOV LEVELS WITHOUT SURGE ARRESTERS. SECOND HIGHEST VALUES INDICATED BETWEEN PARENTHESES

Component	SFO_{max}	Fault	TOV_{max}	Fault
V1	1.15	J	0	-
V2	2.16	L	1.74	J
V3	2.65	L	1.68	J
V4	2.25	K	2.16	K
V_{SM}	2.66 (2.21)	I (J)	2.17	J
V_{BR}	1.11 (1.10)	I (L)	0.30 (0.27)	I (J)

TABLE VII
MAXIMUM SFO AND TOV LEVELS IN CONFIGURATION A1-A2-A3-C

Component	SFO_{max}	Fault	TOV_{max}	Fault
V1	1.14	J	0	-
V2	1.73	L	1.61	J
V3	2.02	L	1.59	J
V4	1.92	K	1.80	K
V_{SM}	2.10	J	2.18	J
V_{BR}	1.21	N2	0.25	J

The submodule capacitors are designed to withstand such currents [11]. However, the loop formed by this fault will force most of the current to pass either through the IGBTs of the cascaded submodules when IGBTs are in the on-state (red path in Fig. 6) or through the antiparallel diodes during the off-state of the IGBTs (blue path in Fig. 6), which are not designed to withstand these current levels. Hence, all precautions have to be taken from the design of the MMC station to completely avoid, within the measure of the possibilities, the occurrence of this fault, since it would imply the loss of the whole arm valve.

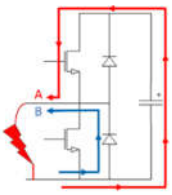


Fig. 6. Current paths during fault I (valve short-circuit) inside each submodule when IGBTs are in on-state (path A, red) and off-state (path B, blue)

If fault I is not considered for the overvoltage profile, because of the reasons explained in the previous paragraph, the next most critical overvoltages obtained are those indicated between parentheses in TABLE VI. The most critical faults are then the DC pole-to-ground, DC bus-to-ground and arm-to-ground faults (L, K and J, respectively), which is consistent with what is found in the current literature [7], [8].

C. Current Levels and Distribution

The currents of the surge arresters under normal operating conditions must remain below the level corresponding to the continuous voltage of the arrester, U_c. TABLE VIII summarizes the discharge currents of the surge arresters in steady state. They are within the typical values expected, though the discharge current at the maximum continuous voltage (U_c) of the arrester can vary between different models and manufacturers (more information on [8], [9], [12–15]).

TABLE VIII
DISCHARGE CURRENTS OF THE ARRESTERS UNDER NORMAL CONDITIONS

Arrester	A1	A2	A3	C
I_{max} (peak)	0.11 mA	0.90 mA	0.38 mA	0.28 mA
I_{rms}	78 µA	0.64 mA	0.27 mA	N/A

When an overvoltage is applied to a point directly protected by an arrester, current will start flowing through it according to the V-I characteristic of the arrester. As previously explained, this event can introduce new current paths to the system.

One of the most critical scenarios found is depicted in Fig. 7 and corresponds to the current path created during fault L through arrester A3. When the propagating wave reaches the station, current starts flowing through the arrester according to its V-I characteristic due to the overvoltage that appears between its terminals. Since no inductance is present in the loop created (red path in Fig. 7), this current will continue to increase for at least 40 µs (Fig. 8 left, green) and most of it will flow directly into the valve (Fig. 8 left, blue). Longer MMC blocking delays imply even higher current levels. This represents a potentially dangerous condition for the IGBTs inside the submodules. This supports the fact that the installation of a smoothing reactor in installations with the arm reactor on the AC side is considered mandatory. This way, no loops without inductive elements can be created through the IGBT valve.

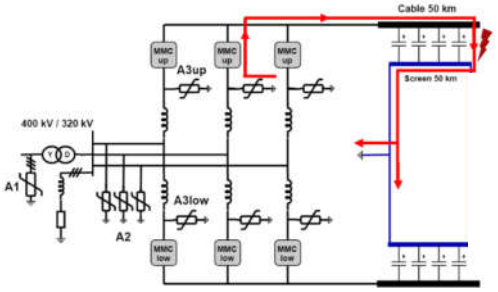


Fig. 7. Current path through arrester A3 on phase b of the upper arm where the maximum current is measured for DC pole to ground fault.

D. Energy Levels

The maximum energy absorption levels of arresters A2, A3 and C are illustrated in Fig. 9 for each configuration. Energy absorption levels for arrester A1 were negligible in all cases, hence it is not represented in the graphs.

It can be observed that arrester C absorbs the most energy when A3 is not present (Fig. 9b). When arrester A3 is present, the incorporation of arrester C does not produce major variations on the energy absorption levels (Fig. 9c and Fig. 9d).

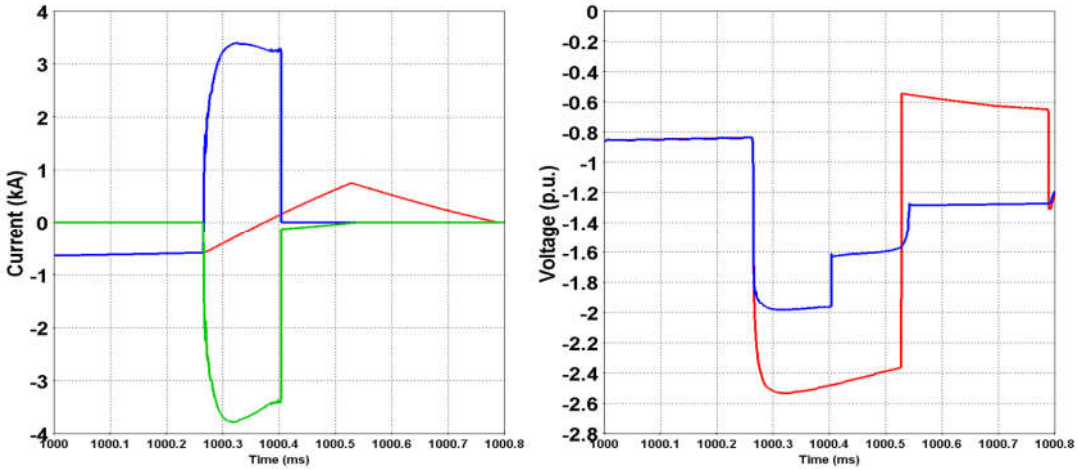
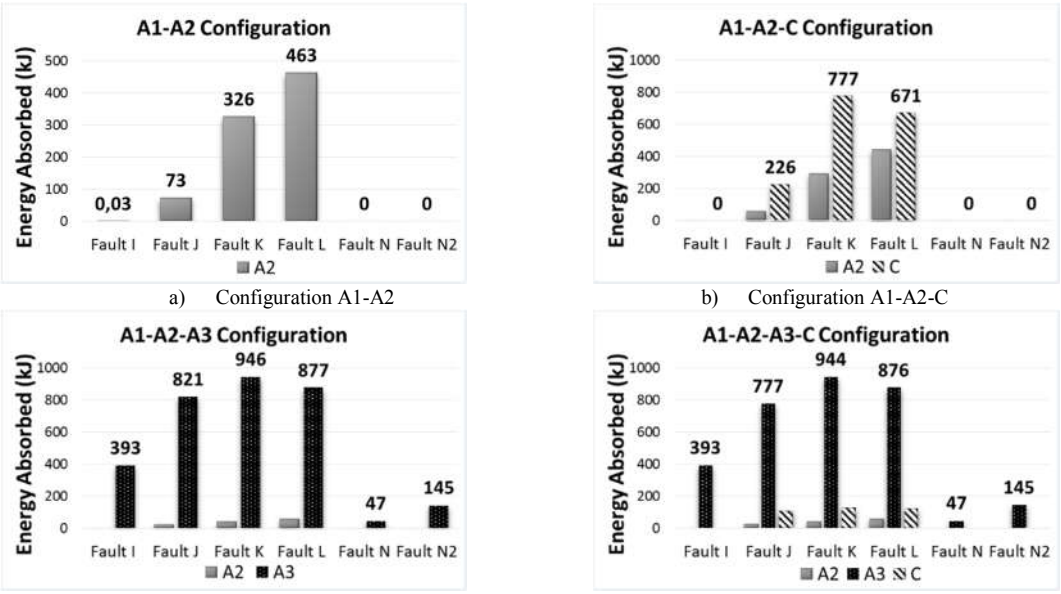


Fig. 8. Comparison between the case without surge arresters (NS, red) and the A1-A2-A3 configuration (blue) for DC pole to ground fault. On the left, the currents flowing through the IGBT valves (phase B), including the current of the corresponding upper surge arrester A3 (green). On the right, the voltage levels at the point protected by arrester A3 (bottom valve). It is seen how the overvoltage levels are effectively limited by the surge arrester.



a) Configuration A1-A2

b) Configuration A1-A2-C

c) Configuration A1-A2-A3

d) Configuration A1-A2-A3-C

Fig. 9. Energy absorption levels of each surge arrester for each configuration

Arrester energy absorption capability is frequently specified in kJ/kV of their rated voltage (U_r) [12] and it typically ranges between 4 and 16 kJ/kV of U_r [16], depending on the energy class. For the arrester ratings used in this work (see TABLE IV), this represents a minimum between 1.15-1.44 MJ, up to a maximum between 4.61-5.76 MJ of total energy handling capability. It is thus concluded that for the specific scheme studied in this work, and for any configuration considered, a single-column arrester is likely to be enough to guarantee the safe operation of the surge arresters, resulting in the overvoltage profiles presented in Fig. 4 and Fig. 5.

The analysis of the general energy absorption profile confirms, along with the overvoltage analysis, that the most critical faults for the system are fault J, K and L for all the studied configurations. Therefore, these faults are considered critical scenarios for the selection of the surge arrester characteristics and configuration.

IV. Discussion

In general terms, the absolute energy levels absorbed by the arresters in this study were relatively low. Additionally, the overvoltage levels obtained for the DC pole may be too high even in the configurations including arrester C (around 1.94 p.u. and 1.81 for SFOs and TOVs, respectively). It is stated in [7], based on the guidelines and recommendations for transmission cable tests provided in [17], that a typical value the XLPE cable insulation can withstand is in the range of 1.8 p.u.

Considering that the surge arresters can effectively withstand much higher energy levels than those obtained in this work, it would be possible –and necessary– to lower the protective levels of the arresters for better overvoltage protection. Furthermore, it is stated in [4], [14] that in DC systems it is possible to include multiple columns of arresters in parallel for better energy dissipation.

Based on these results, it can be concluded that surge arresters for this study were chosen based on very conservative criteria regarding energy absorption levels, while the overvoltage levels observed for the DC pole exceeded its recommended insulation withstand level limits. Protective levels shall be thus lowered, considering that:

1) Arrester current under normal operating conditions shall not result in overheating of the arrester in steady-state.
2) Energy absorbed shall remain within the energy handling capability of the arrester.
3) Current paths created by the sudden conduction of the arresters do not result in an undesired overcurrent for critical or sensitive equipment.

V. Conclusions and Perspectives

The effect of the surge arresters on the electromagnetic transients occurring in case of fault on a DC system depends on the surge arrester scheme considered. This implies that the selection of the surge arrester configuration and their individual parameters may not only depend on the overvoltage levels of the component to be protected, but also on the other arresters and their effect on the system dynamics.

The operating principle of the surge arresters involves the formation of temporary current paths during the transient state. Whenever a new surge arrester configuration is studied, special care shall be taken to the possible loops created by the possible conduction of the surge arresters.

For MMC-HVDC systems presenting the arm reactor on the AC side, the smoothing reactor will also play a role in limiting the fault current through the MMC valve when the arm-to-ground arrester starts conducting. Its installation is thus considered mandatory on MMC-HVDC systems with the arm reactor on the AC side.

The installation of surge arresters could effectively increase the longitudinal withstand voltage requirements of the inductances present in the system, as seen in the case of the arm reactors. This effect, though relatively small, shall be thus taken into account for the design of the clearances and insulation of the reactors, and can be considered as a key factor to decide whether the inductances will require a dedicated overvoltage protection (i.e. a surge arrester in parallel).

The most critical faults found in terms of both overvoltages and energy dissipation levels associated are the pole-to-ground, bus-to-ground and arm-to-ground fault (faults L, K and J, respectively), which is consistent with what has been found in the existing literature. Also, the short-circuiting of the MMC valve (fault I) is a critical scenario that leads to the loss of the whole arm valve. It is thus a fault to be avoided from the design of the station.

Future work shall consider the optimization of the surge arrester parameters and the inclusion of the AC faults on both the converter and AC side of the transformer. Additionally, architectures with the arm reactor on the DC side shall also be investigated.

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