Half-Bridge and H-Bridge Equivalent MMC Models for EMT Simulation

Juan Carlos Garcia Alonso, Steven Howell, Karim Abdel-Hadi

***Abstract*—This paper builds upon the detailed equivalent model for modular multilevel converters to present a novel and computationally efficient technique that accurately models half- and H-bridge configurations for EMT interpolation based algorithms. This modified detailed equivalent model is then extended to accurately model state transitions, which improves simulation accuracy by eliminating the spurious overvoltages and false capacitor cell collapses that conventional techniques may produce. It also properly models transition states within an MMC submodule that occur between one IGBT turning off and another turning on. The proposed techniques yield results that compare favorably to those produced through detailed representations of the MMC arms. Although this paper focuses on half-bridge and H-bridge cell structures, these methods can be further applied to other cell configurations.**

***Index Terms*—Modular Multilevel Converters, MMC, Voltage Source Converters, VSC, modeling, detailed equivalent model, DEM, half-bridge, H-bridge, dead-time.**

I. Introduction

MODULAR multilevel converters (MMCs) comprise large numbers of submodules (SMs), and these SMs contain switching elements consisting of complementary diode/IGBT pairs (Fig. 1). Modeling these switches has traditionally taxed electromagnetic transient (EMT) simulation programs because each switching element increases the size of the network subsystem's admittance matrix, which must be inverted every time a switch operates.

A technique commonly referred to as the detailed equivalent model (DEM) improves computational efficiency by representing SMs by their Thévenin equivalents as outlined in [1] and shown in Fig. 2.

Because MMC SMs are series-connected, their Thévenin equivalents (Fig. 2) can then be combined into single-arm Thévenin equivalents (Fig. 3), thus facilitating EMT modeling by reducing the number of nodes and therefore the size of the corresponding admittance matrix.

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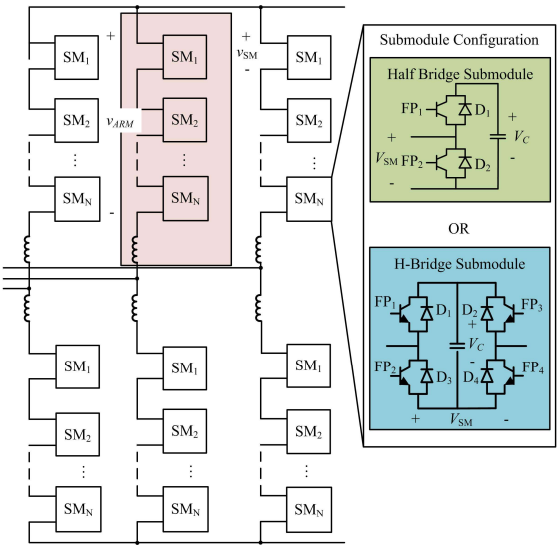

Fig. 1 Modular multilevel converter

However, simulating physical events with discrete time steps inevitably produces inaccuracies because SM switches (and therefore voltages) can physically transition between the ON and OFF states between the simulation's time steps. DEM simply ignores this time discrepancy and updates these transitions at the following time step. This strategy is computationally expedient, but it may produce inaccuracies such as spurious voltages and false capacitor SM collapses.

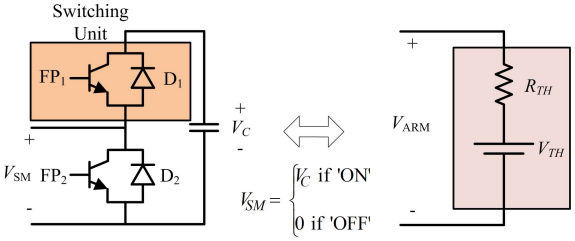

Fig. 2 Thévenin equivalent of a single half-bridge submodule

Other techniques have therefore been developed to better compensate for switching transitions. For example, smaller simulation time steps improve output accuracy by reducing the maximum possible error between the actual and simulated switching times at the expense of significantly increasing simulation time. Other methods include employing backward-Euler integration in conjunction with iterative processes [2] or interpolating each switching instant in the detailed model to the correct switching time. Modifying DEM to indiscriminately

incorporate interpolation for every SM within an MMC arm would be computationally onerous.

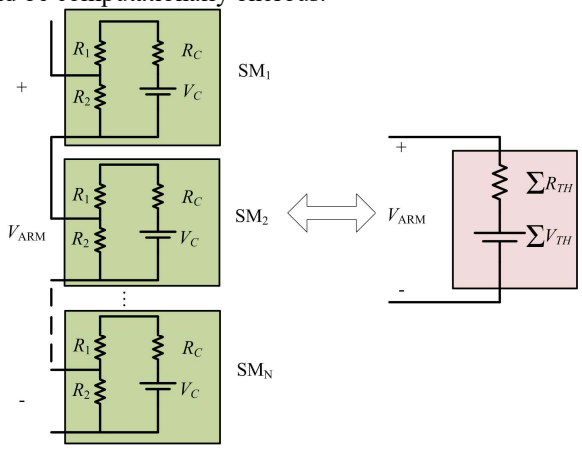

Fig. 3 Thévenin equivalent of an MMC converter arm

The method proposed in [2] modifies the existing DEM model by employing an alternative numerical integration technique to prevent numerical oscillations in conjunction with an iterative method to determine the instant the conduction path changes in a SM while it is in the blocked state. This paper proposes an alternative modification to the DEM model in order to determine the instant diode conductions change without requiring iterative processes and without needing to change numerical integration techniques throughout the duration of the simulation.

II. Extended-DEM for Half-Bridge Configurations

This paper extends DEM to render interpolation tractable for equivalent half- and H-bridge models by selectively choosing which state transitions to simulate. This extended-DEM technique is valid both when every SM within a converter arm is simultaneously operational and when they are all 'blocked', meaning that the firing pulses to every switch within the submodules are zero. This blocking condition occurs at startup and during certain faults for protection purposes.

The state transitions within a SM that are important enough to warrant interpolation can be determined by analyzing the impact that the lack of interpolation has on the overall simulation accuracy.

The models developed in this paper represent power electronics switches, diodes, and IGBTs as two-state devices with ~0.1 MΩ – 1.0 MΩ resistances in the 'OFF' state and ~0.1 mΩ – 1.0 mΩ resistances in the conducting, or 'ON', state.

Of all possible switching state transitions that can occur between time steps, two transitions are of particular interest.

A. Changing current direction when a SM firing order remains unchanged

These cases are illustrated in Fig. 4. The equivalent resistance R_{eq} of the conducting switching unit shown in Fig. 2 before and after the state transition for the case illustrated in Fig. 4a are described by

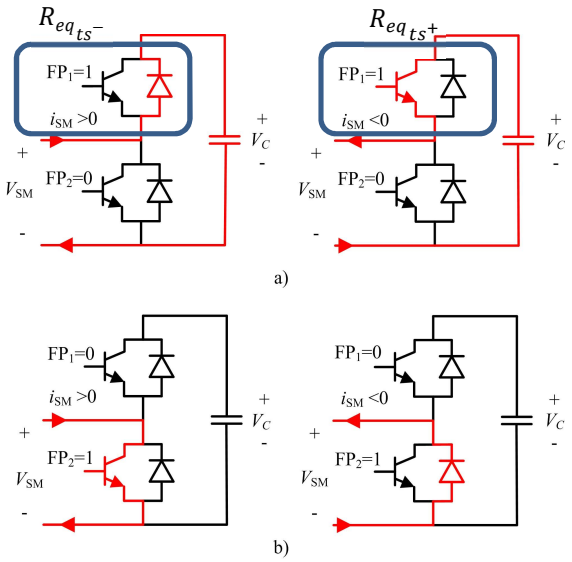

Fig. 4 Current paths for a) inserted and b) bypassed capacitor

$$R_{eq_{ts^-}} = \frac{R_{IGBT_{OFF}} \cdot R_{Diode_{ON}}}{R_{IGBT_{OFF}} + R_{Diode_{ON}}} \tag{1}$$

and

$$R_{eq_{ts^+}} = \frac{R_{IGBT_{ON}} \cdot R_{Diode_{OFF}}}{R_{IGBT_{ON}} + R_{Diode_{OFF}}} \tag{2}$$

In most practical cases, $R_{IGBT_{ON}}$ and $R_{Diode_{ON}}$ are equal or similar in magnitude, and $R_{IGBT_{OFF}}$ and $R_{Diode_{OFF}}$ are also equal or similar in magnitude. The equivalent resistance before and after the transition are therefore also similar:

$$R_{eq_{ts^-}} \approx R_{eq_{ts^+}} \tag{3}$$

Because the resistance remains approximately the same and the current continues flowing through the same switching unit independently of the current direction, the capacitor remains in its original inserted or bypassed state. System studies that do not interpolate for SM switching will therefore produce negligible error, and DEM can be used in its original form.

B. Changing current direction when the SM is blocked

When the SM is blocked, both IGBT firing orders are zero. A change in current direction from either positive to negative or from negative to positive leads the cell capacitor to transition from inserted to bypassed or vice versa. In the event that there is no current flowing within a sub-module, the sub-module would be in a high impedance state in which both diodes would not be conducting.

Fig. 5 illustrates one of the two possible cases, when the current transitions from positive to negative. The calculation of the equivalent resistance for the upper switching unit before and after the switching time t_s is

$$R_{eq_{ts^-}} = \frac{R_{IGBT_{OFF}} \cdot R_{Diode_{ON}}}{R_{IGBT_{OFF}} + R_{Diode_{ON}}} \quad (4)$$

and

$$R_{eq_{ts^+}} = \frac{R_{IGBT_{OFF}} \cdot R_{Diode_{OFF}}}{R_{IGBT_{OFF}} + R_{Diode_{OFF}}} \quad (5)$$

Where $R_{eq_{ts^-}} << R_{eq_{ts^+}}$.

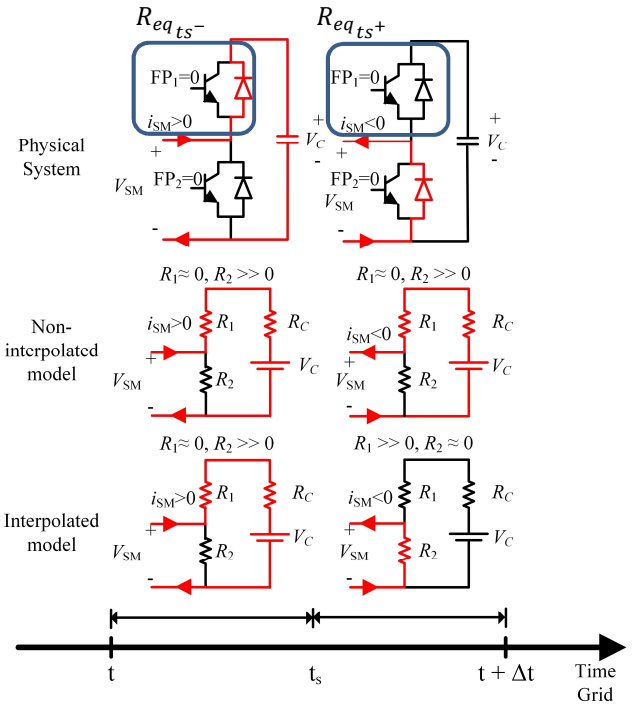

Fig. 5 Blocked state (FP_1=0, FP_2=0) current paths with and without interpolation at t+Δt

Neglecting to update the switching pair values at time t_s causes the simulation to continue computing the current as flowing through the wrong path from time t_s to the next time step t+Δt in the discretized time grid. This is especially significant when the SM is blocked (FP_1=0 & FP_2=0), because the current changes path through the SM depending on the current direction entering the SM (see Fig. 5). If the current path remains uncorrected, negative current continues flowing through the capacitor between t_s and t+Δt. This discharges the capacitor, possibly producing false capacitor collapses and in some cases numerical spurious overvoltages. Fig. 12 and Fig. 13 show some of these results. Interpolating to time t_s and therefore correcting the resistances at t_s eliminates this problem and produces correct results, as is also illustrated in Fig. 12 and Fig. 13.

This problem can be solved for the half-bridge by adding interpolation ready IGBT and diode components in series and parallel with the equivalent Thévenin model (see Fig. 6). In this configuration during normal operation, the series IGBT ($IGBT_{SE}$) is set to conduct, enabling bi-directional currents to flow through the capacitors represented by the Thévenin equivalent V_{TH}. The added IGBT and diode components employ the linear interpolation method shown in [3] to ensure the proper transition states. Essentially, when a transition state is detected, the interpolation algorithm assumes a linear relationship between the solution at time t and time $t+\Delta t$, which is reasonable due to the time step's duration. If a transition state is detected, the interpolation algorithm interpolates the current to when it switched directions (i=0) and updates all of the variables at time t_s. Next, a solution step is computed at time t_s+Δt. All variables are then interpolated back to the time grid at t+Δt such that the simulation continues normally from that point onward.

During the blocked state, Thévenin voltage and resistance V_{TH} and R_{TH} are calculated by artificially setting FP_1=1 and FP_2=0 in all of an MMC arm's SMs. The series IGBT ($IGBT_{SE}$) firing pulse is set to 0 so that the current flows through d_1 and the capacitors (represented by the equivalent V_{TH}) if the total current, i, is positive, and flows through the parallel diode d_2 if the current is negative. Diodes d_1 and d_2 take care of the interpolation and prevent false negative currents from flowing through the capacitors, thus eliminating the false capacitor voltage collapses produced by the original model [1] during blocked state. Diode d_1 and series $IGBT_{SE}$ conduction resistances (R_{ON}) are set to negligible values to minimize their effects while diode d_2 conduction resistance is set to $R_{d2_{ON}} = R_{Diode_{ON}} \times n_{cells}$ in order to represent the full chain of conducting diodes when current i is negative.

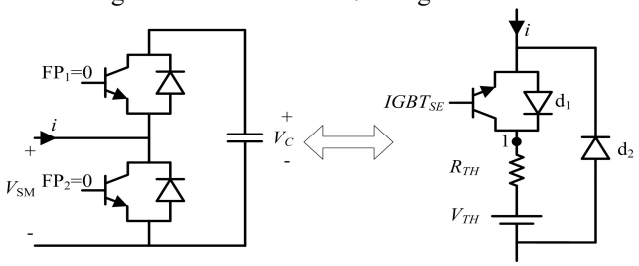

Fig. 6 Half-bridge model proposed for blocked state (FP_1=0 & FP_2=0) – general use

III. Extended-DEM for H-Bridge Configurations

An interpolated model that eliminates false capacitor voltage collapses and spurious overvoltages during blocked states in H-bridge configurations (Fig. 7) can be constructed using the same technique used to build the half-bridge model. The proposed H-bridge model is shown in Fig. 8.

During normal operation, both series $IGBT_{SE1}$ are set to ON while both parallel $IGBT_{Pr1}$ are set to OFF, and current flows freely through the SMs' Thévenin equivalent V_{TH} and R_{TH}. During a blocked state, series $IGBT_{SE1}$ are set to OFF, parallel $IGBT_{Pr1}$ are set to ON, and both positive or negative current entering the SMs are always directed in the positive (charging) direction through the Thévenin equivalent V_{TH} and R_{TH}. For blocked states, the Thévenin equivalent is calculated by artificially setting FP_1=1, FP_4=1 (see Fig. 7) on all SMs within the arm to allow the charging currents to flow freely through the capacitors.

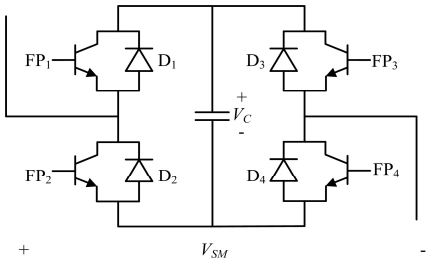

Fig. 7 H-bridge submodule

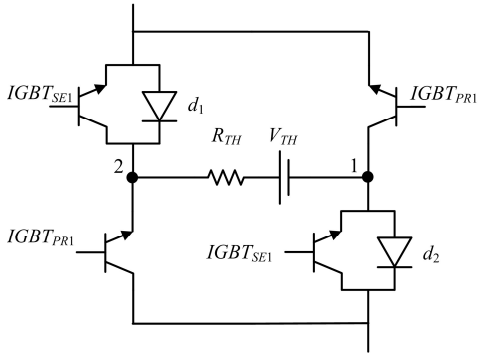

Fig. 8 H-bridge model with blocked state capability - general use

Fig. 9 illustrates the current flows through the proposed H-bridge model during blocked state.

IV. Practical Limitations to the Proposed Model

The modified models proposed here introduce additional electrical nodes compared to the models proposed in [1]. One additional node is required for the half-bridge model in Fig. 6 versus the original DEM [1], and two additional nodes are needed for the H-bridge model in Fig. 8. The nodes are denoted by bold dots. The additional nodes required by the extended DEM will make the simulation slightly slower than the original model proposed in [1].

V. Simulation Results

The following subsections illustrate scenarios where ignoring the interpolated diode current path transitions produce inaccurate results. The system studied along with its relevant parameters and control modes is shown in Fig. 11. These simulations compare results from applying the Detailed Model, which CIGRE B4-57 refers to as model Type-3 [4], to the traditional and extended-DEM methods. Ref [2] does not describe the actual algorithmic implementation of its iterative method, so it is impossible to state how it was implemented and determine its computational burden compared to these other methods. Extended-DEM therefore cannot be used to provide a direct comparison against the method proposed in ref [2].

A. DC fault applied to a two-terminal half-bridge system

In this case, the converter valves are blocked to protect the IGBTs as part of the DC fault clearing procedure (Fig. 10). Fig. 12 and Fig. 13 use a 50 µs time step to simulate the same system using a detailed model, traditional DEM, and the extended-DEM technique. Although both DEM techniques provide good results during system start-up, traditional DEM produces a spurious peak in the DC voltage when both converters are blocked upon inception of the DC fault. Moreover, the capacitor voltages in traditional DEM collapse once the converter blocks.

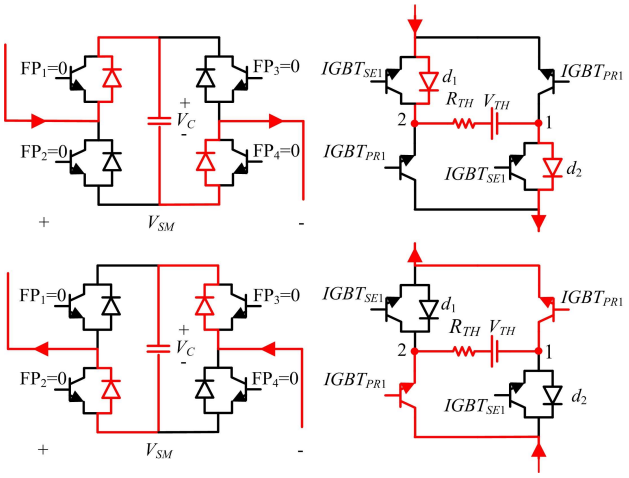

Fig. 9 Current flow during blocked states: H-bridge and equivalent model.

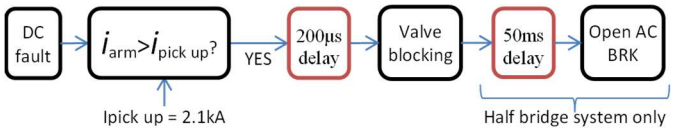

Fig. 10 DC fault detection and clearing strategy

Applying interpolation during the blocked state becomes less relevant as smaller time steps are used. For example, Fig. 14 shows that a 2.5 µs time step greatly improves the quality of results. The capacitor voltage no longer collapses. Instead of employing interpolation, real time tools such as RTDS produce accurate results by using smaller time steps combined with real time simulation techniques to correct for the lack of interpolation [5][6].

TABLE 1 compares the relative simulation times using the detailed model as the benchmark and shows that the extended-DEM presented in this paper is comparable in speed to that of the original DEM while producing much greater accuracy.

TABLE 1. Comparison of Half- and H-bridge simulation times

Model Type	Speed up factor	
	Half-bridge	H-bridge
Detailed Model	-	-
DEM	60.9	86.7
Extended-DEM	60.7	74.5

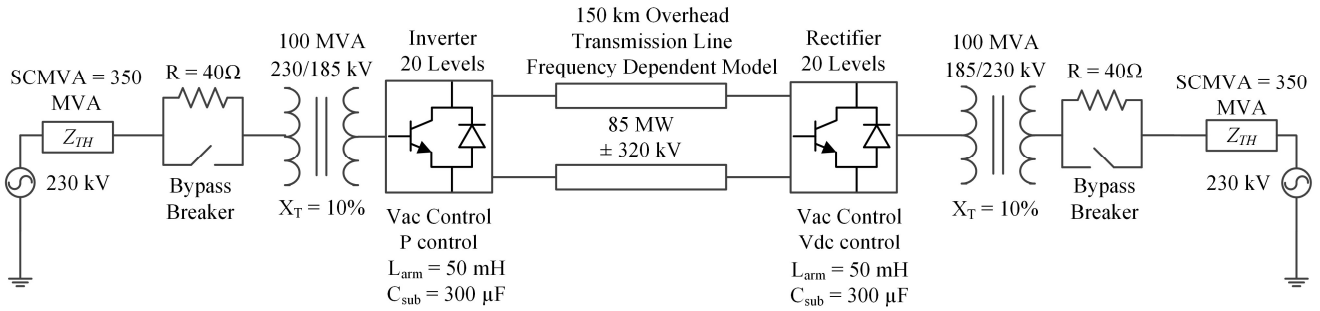

Fig. 11 Two-terminal MMC VSC-HVDC test system

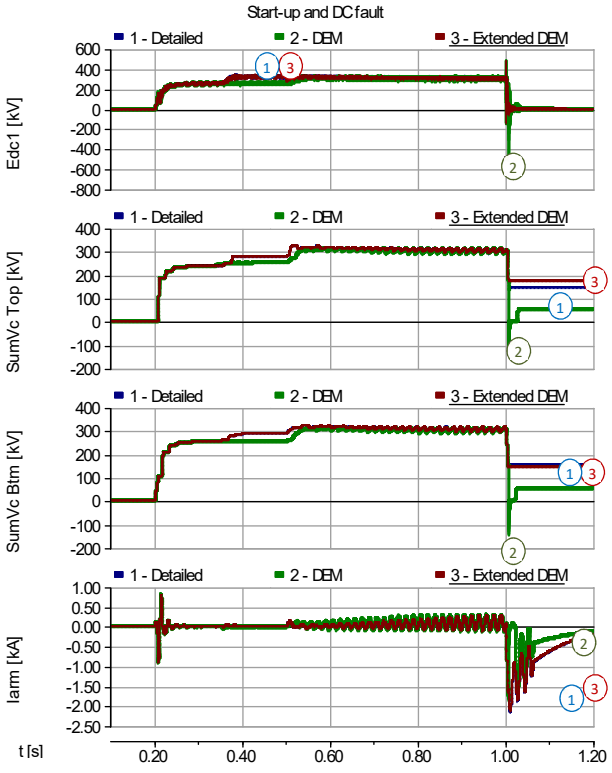

Fig. 12 Start-up and DC fault sequence of events for two-terminal half-bridge system: V_{DC}, ΣVcap for ph-A top and bottom arms (rectifier terminal), and ph-A top arm valve current (rectifier terminal). Events: AC breakers close at both terminals at t=0.2 s. Pre-insertion resistances bypassed at t=0.26 s. Rectifier de-blocks at t=0.35 s. Inverter de-blocks at t=0.5 s. Pole-to-pole DC fault applied at t=1.0 s. DC fault clearance sequence given in Fig. 10

B. DC fault applied to a two-terminal H-bridge system

The valves in the two-terminal system used in section V.A were replaced with H-bridges and re-simulated under otherwise identical conditions. Fig. 15 and Fig. 16 show that the extended-DEM yields very good results when compared with the detailed model. It also compares favorably to most simulations that use traditional DEM techniques. Once both sending and receiving end converters are blocked, the traditional DEM produces unrealistic oscillations in the DC voltage and inaccurate remnant voltages in the SM capacitors.

TABLE 1 compares the relative simulation times using the detailed model as the benchmark and shows that the H-bridge extended-DEM is comparable but slower than the half-bridge results (TABLE 1). This is expected because the H-bridge extended-DEM model (Fig. 8) uses twice as many interpolated elements as the analogous half-bridge model (Fig. 6). However, the results still greatly improve accuracy at a relatively large time step compared with the original DEM.

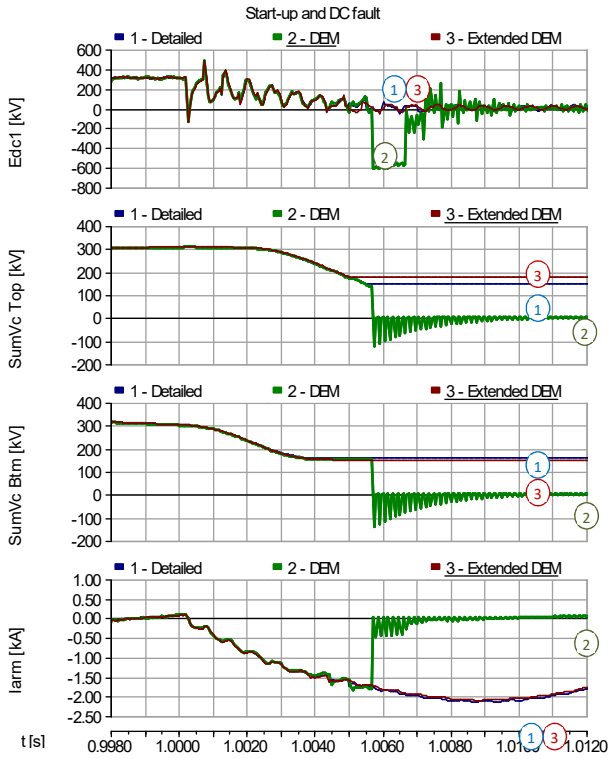

Fig. 13 Same simulation as shown in Fig. 12, magnified around the instant of applied DC fault and blocking of converters.

Two phenomena account for the minor discrepancy between the summed capacitor voltages as calculated by the detailed model and the extended-DEM in Fig. 12-Fig. 15. First, unlike the extended-DEM, which interpolates all components within all cells at the same time, the detailed model independently interpolates each diode and IGBT within each cell. Since the current flowing through these elements is the superposition of the arm current along with the current from each capacitor, the calculated switching time differs slightly for each cell depending upon the voltage of each cell capacitor.

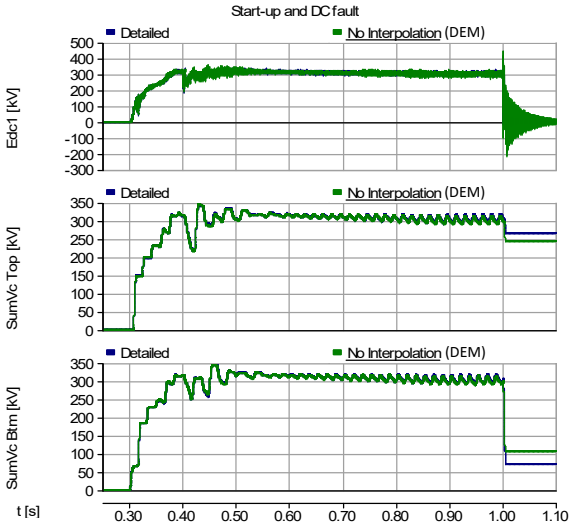

Fig. 14 Simulation of same system as shown in Fig. 12 with time-step shrunk from 50 µs to 2.5 µs to illustrate effect or smaller time step in results.

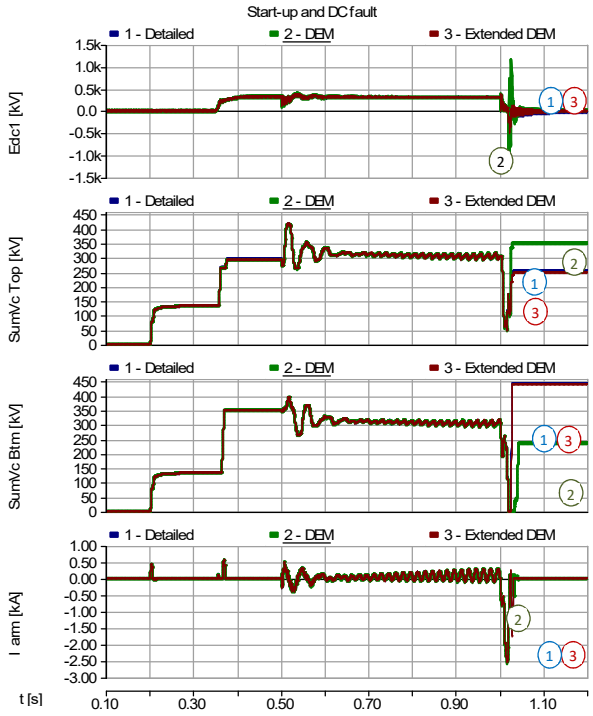

Fig. 15 Start-up and DC fault sequence of events for a two-terminal H-bridge system: V_{DC}, ΣVcap for ph-A top and bottom arms (rectifier terminal), and ph-A top arm valve current (rectifier terminal). Events: AC breakers close at both terminals at t=0.2 s. Pre-insertion resistances bypassed at t=0.26 s. Rectifier de-blocks at t=0.35 s. Inverter de-blocks at t=0.5 s. Pole-to-pole DC fault applied at t=1.0 s. DC fault cleared by valve blocking 200 µs after detection.

Secondly, the artificial series and parallel elements introduced in the extended-DEM to handle interpolation (see Fig. 6 and Fig. 8) also introduce parasitic impedances that do not exist in the Type-3 detailed model as defined in [4]. The inaccuracies introduced by these parasitic impedances are more than offset by the improved accuracy and numerical stability that the extended-DEM model provides by enabling interpolation.

VI. Conclusions

An efficient equivalent model with blocking capability is presented for general use in the simulation of chains of half- and H-bridge SMs. The models in this paper produce results that agree well with detailed representations of SM chains.

The techniques applied to half- and H-bridge SM in this paper can be adapted to other SM configurations in a straightforward manner if desired. These techniques can also be further extended to include parasitic inductances and capacitances that occur within each SM during severe fault conditions if desired.

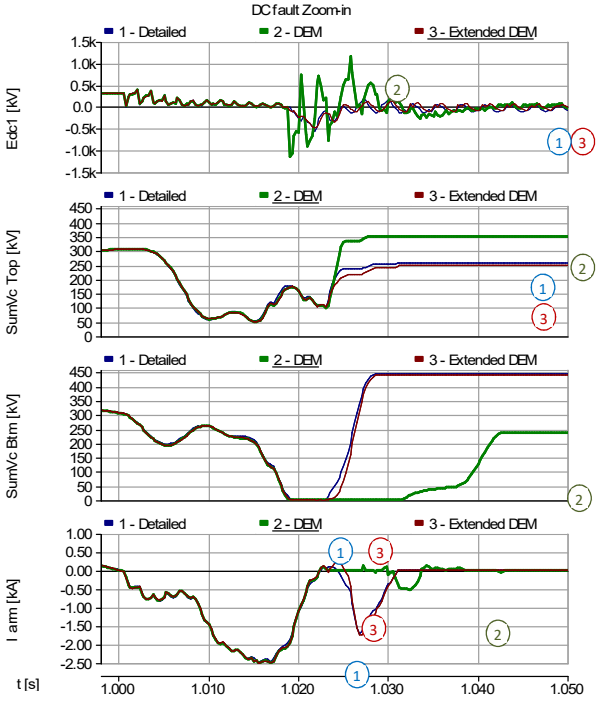

Fig. 16 Same simulation as shown in Fig. 15, magnified around the instant of applied DC fault and blocking of converters.

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