Voltage Compensation in Multi-Grounded Distribution Network with a Three-Phase Five-Wire DSTATCOM

S. N. Duarte, P. M. Almeida, P. G. Barbosa

***Abstract*—This paper presents a three-phase static synchronous compensator with five legs to be connected to a multi-grounded neutral distribution network. Several strategies are proposed in the literature to compensate for the imbalances in multi-grounded networks. Typically, three-phase static synchronous compensators with four legs can compensate for positive-, negative- and zero-sequence network voltages. However, they cannot compensate for the neutral voltage of multi-grounded network. Thus, the fifth-leg of the proposed compensator is controlled as a single-phase converter in order to compensate the neutral-voltage at the point of common coupling. Linearised mathematical models, in the synchronous reference frame, are developed and used to design the controllers used to compensate the network's neutral voltage and to regulate the current synthesized by the fifth-leg of the compensator. A multi-grounded network, derived from the IEEE NEV test feeder, is modelled in the PSCAD/EMTDC to investigate the performance of the proposed compensator. The results of the digital simulations demonstrate the effectiveness of the neutral voltage compensation strategy and validate the control loops designed for the three-phase static synchronous compensator with five legs.**

***Keywords*—DSTATCOM, Grid-Connected Converter, Control Algorithm**

I. Introduction

Modern distribution networks provide electricity for a wide variety of linear and non-linear loads connected to one, two and three phases of the mains [1]. The unbalanced currents absorbed by these loads, as well as the non-transposed structure of the feeders and the connection of single- and three-phase transformers, contribute to the propagation of unbalanced voltages in the electrical networks. In addition to the previous issues, the increase in the number of single-phase distributed generation systems (*e.g.* rooftop photovoltaic) may aggravate the problem of voltage imbalance in electrical networks in the near future [2].

A recently published work investigated the strategies proposed in the last two decades to mitigate imbalances in the distribution networks [3]. In addition to report the growing trend of imbalance mitigation research, the authors presented a summary of the imbalance recommendations made by some of the world's leading organizations. Historically, when the balancing of the loads connected to the distribution feeders cannot be performed, the voltage unbalance can be mitigated by connecting capacitors and/or inductors among the phases of the feeders [4], besides the use of variable-tap transformers to regulate the voltages of each phase independently [2].

On the other hand, there are several papers were the authors propose the use of static converters to improve the power quality of the electrical networks. For instance, a dynamic voltage restorer (DVR) is proposed in [5] to mitigate the voltage unbalance of the electric network. However, in case of a failure of the device, the electricity supply may be compromised once the DVR is connected in series with the feeder. Under other conditions, the authors in [6] and [7] shown that the inverters used as front-end circuits of distributed generators could also be used to compensate for negative-sequence voltage at the point of common coupling (PCC).

The distribution static synchronous compensator (DSTATCOM) is a power electronic converter designed to compensate reactive power at its ac terminals. This compensator can also be connected to distribution networks in order to compensate for power factor and to regulate the network voltage. A three-phase DSTATCOM can also compensate for the negative-sequence voltage in a three-wire network [8]. However, the manufacture of high-capacity self-commutated semiconductor switches has allowed the development of multilevel converter topologies that can be connected directly to medium voltage networks without the need for transformers or complex filter structures [9].

In [10], the authors used a three-phase DSTATCOM, with four legs, to regulate the positive-sequence voltage and to compensate the zero-sequence voltages in a three-phase four-wire network. However, multi-grounded electrical networks can present an additional imbalance issue when supplying electricity to single-, two- and three-phase loads. A current can flow through the neutral wires and grounding resistances, causing an elevation in neutral-to-ground voltage [11], [12]. In many time-domain studies involving the connection of power electronic converters, the neutral wire and the grounding resistances are neglected. In these examples, the results of the simulations may not adequately represent the behaviour of the distribution networks.

Duarte et al [13] proposed the use of a three-phase four-wire power conditioning to compensate imbalances in multi-grounded distribution networks. Although a $3\phi4w$–DSTATCOM compensates the voltage imbalance at the PCC the simulation results shown that the neutral-to-ground voltage was not fully compensated. In these types of networks, the paths formed by the grounding resistors act as a fifth-wire. Therefore, this paper will extend the work proposed in [13], but instead of using a $3\phi4w$–DSTATCOM, a new three-phase five-wire compensator will be used to compensate the neutral voltage at the PCC, in addition to compensate the positive-, negative- and zero-sequence voltages. Small-signal mathematical models will be used to design the current and voltage control loops used to control the fifth-leg of the static compensator as a single-phase converter. A simple multi-grounded neutral distribution network, based on the IEEE NEV test feeder [14], will be used to demonstrate the effectiveness of the proposed strategy.

II. Modelled System

Fig. 1 shows the topology of a multi-grounded neutral distribution network. This circuit was derived from the IEEE NEV test feeder [14]. The parameters R_f and L_f respectively represent the resistance and inductance of the feeders, while the parameters R_L and L_L are the resistance and inductance of the loads, respectively. The three-phase voltages v_{abc} are the secondary voltages of the distribution transformer. The voltages $v_{B1,n}$, $v_{B2,n}$ and v_n are the neutral-to-ground voltages across the grounding resistances R_{g1}, R_{g2} and R_g, respectively. The subindexes $(_{B1})$ and $(_{B2})$ denote the Bus 1 and Bus 2, respectively.

As mentioned earlier, in [9] and [10], $3\phi4w$–DSTATCOM was used to compensate the negative- and zero-sequence voltages at

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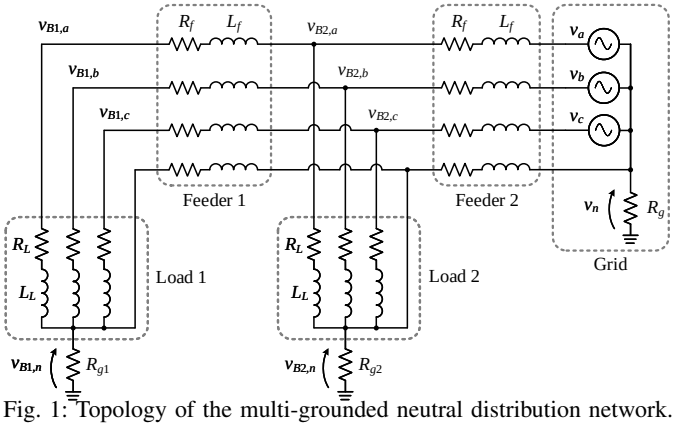


Fig. 1: Topology of the multi-grounded neutral distribution network.

the PCC. However, neutral-to-ground voltage compensation was not addressed in the works cited, since the paths formed by the grounding resistors act as a fifth-wire for the electrical network. Fig. 2 shows the topology of the $3\phi5w$–DSTATCOM with an equivalent capacitance C_{eq} connected to its DC terminals. It consists of voltage source converter with five legs, each with two IGBTs and two antiparallel diodes. The static compensator is connected to an equivalent distribution network by means of five sets of second-order passive filter composed of series inductor, represented by the inductance L_i and the resistance R_i, and a shunt capacitor C_i, connected to the neutral-wire. In this figure, the equivalent electric network is modelled by a three-phase voltage source $v_{s,abcn}$ series connected to the impedance $(R_s + \jmath\omega_s L_s)$, where $\omega_s = 2\pi f_s$ is the grid fundamental angular frequency.

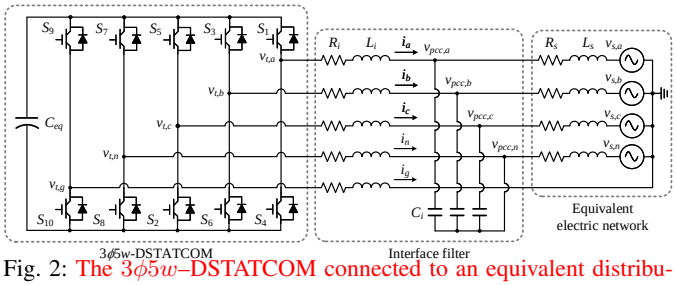


Fig. 2: The $3\phi5w$–DSTATCOM connected to an equivalent distribution network.

The first four legs of the DSTATCOM of Fig. 2 are connected to the phases "*a*", "*b*", "*c*", and neutral-wire. They are controlled to regulate the positive-sequence voltage and to compensate the negative- and zero-sequence voltages at the PCC in a similar way as proposed in [9]. On the other hand, the fifth-leg of the $3\phi5w$–DSTATCOM controls the neutral voltage at the PCC.

In the next section, mathematical models will be developed to control the fifth-leg of the $3\phi5w$–DSTATCOM as a single-phase converter to regulate the current i_g in order to compensate for the neutral voltage $v_{pcc,n}$ at the PCC.

III. Modelling and Control of the Fifth-Leg of The $3\phi5w$–DSTATCOM

The $3\phi5w$–DSTATCOM will be controlled in the synchronous reference frame. This choice is justified by the possibility to use proportional-integral (PI) controllers, simplifying the design of control loops for the static compensator [9].

However, it is not possible to apply the *dq*–transformation directly to the current i_g and the voltage $v_{pcc,n}$. Therefore, a fictitious β-axis must be used to allow these quantities be modelled in the $\alpha\beta$ coordinates. The second-order generalized integrator (SOGI) and a transport delay buffer will be used to generate 90-degrees shift-delay signals for the voltage $v_{pcc,n}$ and the current i_g, respectively.

Fig. 3 shows the block diagram for the algorithm used to convert the neutral voltage at the PCC into a fictitious $\alpha\beta$ reference frame. The output signal $v_{pcc,n\alpha}$ tracks the instantaneous neutral voltage $v_{pcc,n}$ while the voltage $v_{pcc,n\beta}$ is 90° lagged from $v_{pcc,n\alpha}$.

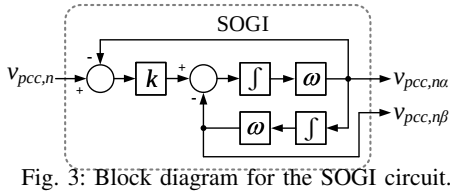


Fig. 3: Block diagram for the SOGI circuit.

Despite the good performance of the SOGI circuit for the PCC voltages, the current i_g synthesized by the DSTATCOM presents a faster dynamic behaviour than the neutral voltage measured at the PCC. Thus, a transport delay buffer is used to generate the fictitious component $i_{g\beta}$ for the current $i_g = i_{g\alpha}$. Fig. 4 shows the block diagram for the transport delay buffer, where $T = (1/f)$ is the fundamental period of the current i_g.

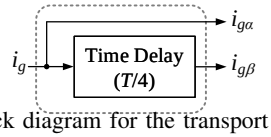


Fig. 4: Block diagram for the transport delay buffer.

A. The current control of the $3\phi5w$–DSTATCOM fifth-leg

Neglecting the switching harmonics, and assuming $v_{pcc,g} = 0$ since the fifth-leg of the DSTATCOM was connected directly to the earth through the interface filter, the following dynamic equations can be written, in the $\alpha\beta$ coordinates, for the fifth-leg of the $3\phi5w$–DSTATCOM of Fig. 2:

$$L_i \frac{di_{g\alpha}}{dt} = -R_{eq} i_{g\alpha} + v_{t,g\alpha}, \tag{1}$$

$$L_i \frac{di_{g\beta}}{dt} = -R_{eq} i_{g\beta} + v_{t,g\beta}, \tag{2}$$

where $i_{g\alpha}$ and $i_{g\beta}$ are the instantaneous currents synthesized by the fifth-leg of $3\phi5w$–DSTATCOM; $v_{t,g\alpha}$ and $v_{t,g\beta}$ are the instantaneous terminal voltages of the fifth-leg of $3\phi5w$–DSTATCOM; $R_{eq} = (R_i + R_{igbt})$ is the equivalent resistance and R_{igbt} is the resistance of the IGBTs.

As previously mentioned, $v_{t,g\beta}$ and $i_{g\beta}$ in (2) were artificially generated by the SOGI and the Transport Delay Buffer shown in Fig. 3 and Fig. 4, respectively. Then, applying the $\alpha\beta \rightarrow dq$ transformation in (1) and (2) yields:

$$L_i \frac{di_{gd}}{dt} = -R_{eq} i_{gd} + \omega L_i i_{gq} + v_{t,gd}, \tag{3}$$

$$L_i \frac{di_{gq}}{dt} = -R_{eq} i_{gq} - \omega L_i i_{gd} + v_{t,gq}, \tag{4}$$

where i_{gd} and i_{gq} are the d- and q-axis instantaneous currents synthesized by the fifth-leg of the $3\phi5w$–DSTATCOM, $v_{t,gd}$ and $v_{t,gq}$ are the d- and q-axis voltages synthesized by the fifth-leg of the $3\phi5w$–DSTATCOM, and ω is the angular frequency of the PCC voltages tracked by a second-order generalized integrator based phase-locked loop (DSOGI-PLL) [15].

Considering that a sinusoidal PWM strategy generates the pulse pattern for the $3\phi5w$–DSTATCOM, one can replace the terminal volt-

ages of the fifth-leg by $v_{t,gd} = m_{gd}(V_{dc}/2)$ and $v_{t,gq} = m_{gq}(V_{dc}/2)$ and to write the following control laws:

$$m_{gd} = \frac{2}{V_{dc}}\left(-\omega L_i i_{gq} + u_{gd}\right), \tag{5}$$

$$m_{gq} = \frac{2}{V_{dc}}\left(+\omega L_i i_{gd} + u_{gq}\right), \tag{6}$$

where m_{gd} and m_{gq} are the modulation indexes for the sinusoidal PWM strategy, u_{gd} and u_{gq} are the new d- and q-axis control variables and V_{dc} is the DC terminal voltage of the static converter.

Replacing (5) and (6) into (3) and (4), the cross-coupling between the d- and q-axis currents are eliminated, resulting in the following first-order dynamic system:

$$L_i \frac{di_{gd}}{dt} = -R_{eq} i_{gd} + u_{gd}, \tag{7}$$

$$L_i \frac{di_{gq}}{dt} = -R_{eq} i_{gq} + u_{gq}. \tag{8}$$

Since the dynamic behaviour of the system given by (7) and (8) is decoupled, PI-controllers can be designed to regulate the currents i_{gd} and i_{gq}, as follows:

$$u_{gd} = k_{ig,p}\ \varepsilon_{gd} + k_{ig,i} \int_{-\infty}^{t} \varepsilon_{gd} d\lambda, \tag{9}$$

$$u_{gq} = k_{ig,p}\ \varepsilon_{gq} + k_{ig,i} \int_{-\infty}^{t} \varepsilon_{gq} d\lambda, \tag{10}$$

where $\varepsilon_{gd} = (i^*_{gd} - i_{gd})$ and $\varepsilon_{gq} = (i^*_{gq} - i_{gq})$ are the errors between the reference currents (i^*_{gd}, i^*_{gq}) and the DSTATCOM currents (i_{gd}, i_{gq}), respectively, $k_{ig,p}$ and $k_{ig,i}$ are the proportional and integral gains of the current regulator $K_{ig}(s) = k_{ig,p} + k_{ig,i}/s$, respectively, and λ is a dummy variable.

Fig. 5 shows the control block diagram to regulate the currents i_{gd} and i_{gq} synthesized by the fifth-leg of $3\phi 5w$–DSTATCOM. From (7)–(10), the gains of the controller $K_{ig}(s)$ can be chosen equal to $k_{ig,p} = (L_i/\tau_{ig})$ and $k_{ig,i} = (R_{eq}/\tau_{ig})$ to ensure a first-order response to the closed-loop transfer function, where τ_{ig} is the desired time constant [10], [16].

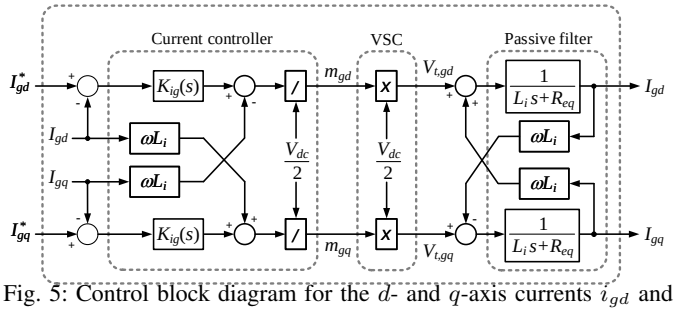


Fig. 5: Control block diagram for the d- and q-axis currents i_{gd} and i_{gq}.

The modulation index m_g for the fifth-leg of the DSTATCOM can be calculated as follows:

$$m_g = \cos(\rho) m_{gd} - \sin(\rho) m_{gq}, \tag{11}$$

where $\rho = (\omega t + \phi)$ is the angle of the positive-sequence PCC voltage tracked by the DSOGI-PLL, being ω and ϕ the angular frequency and the phase of ρ, respectively.

Therefore, it is possible to calculate the modulation index m_n for the terminal connected to the neutral-wire as follows:

$$m_n = -\underbrace{(m_a + m_b + m_c)}_{3m_0} - m_g, \tag{12}$$

where m_a, m_b and m_c are the modulation indexes of each phase of the DSTATCOM, given by the positive-, negative- and zero-sequence current controllers [10], [9].

The analysis of (12) shows that the fourth-leg modulation index depends on the value of m_0 and m_g. Then, the current i_0 can compensate the zero-sequence voltage $v_{pcc,0}$ at the PCC [10], while the current i_g can compensate the neutral voltage $v_{pcc,n}$ at the PCC. The design of the control loops for the positive-, negative- and zero-sequence voltages at the PCC are given in detail in [10] and [9].

In the next section, the steps to design the control loops to compensate for the neutral voltage at the PCC will be presented.

B. The control of the neutral voltage at the PCC

Starting from the network-side terminals of Fig. 2 and neglecting the harmonic currents through the capacitors of the interface filter, the following relations in the $\alpha\beta$-frame can be written for the neutral voltage at the PCC:

$$v_{pcc,n\alpha} = L_{sn} \frac{di_{n\alpha}}{dt} + R_{sn} i_{n\alpha} + v_{s,n\alpha}, \tag{13}$$

$$v_{pcc,n\beta} = L_{sn} \frac{di_{n\beta}}{dt} + R_{sn} i_{n\beta} + v_{s,n\beta}, \tag{14}$$

where $v_{s,n\alpha}$ and $v_{s,n\beta}$ are the network neutral voltages, $i_{n\alpha}$ and $i_{n\beta}$ are the neutral currents and, L_{sn} and R_{sn} are the inductance and resistance of the network neutral-wire, respectively.

Applying the $\alpha\beta \rightarrow dq$ transformation in (13) and (14) yields:

$$v_{pcc,nd} = L_{sn} \frac{di_{nd}}{dt} - \omega L_{sn} i_{nq} + R_{sn} i_{nd} + v_{s,nd}, \tag{15}$$

$$v_{pcc,nq} = L_{sn} \frac{di_{nq}}{dt} + \omega L_{sn} i_{nd} + R_{sn} i_{nq} + v_{s,nq}, \tag{16}$$

where $v_{pcc,nd}$ and $v_{pcc,nq}$ are the d- and q-axis neutral voltages at the PCC, respectively; i_{nd} and i_{nq} are the d- and q-axis neutral currents of the DSTATCOM, respectively; $v_{s,nd} = \widehat{V}_{sn}\cos(\omega_s t + \phi_{sn} - \rho)$ and $v_{s,nq} = \widehat{V}_{sn}\sin(\omega_s t + \phi_{sn} - \rho)$; $\widehat{V}_{sn}$, ω_s and ϕ_{sn} are the peak value, angular frequency and phase angle of the network neutral voltage, respectively.

The linearisation of (15) and (16) yields the following mathematical relationships:

$$\overline{V}_{pcc,nd} = -\overline{\omega} L_{sn} \overline{I}_{nq} + R_{sn} \overline{I}_{nd} + \widehat{V}_{sn}\cos\overline{\rho}_0, \tag{17}$$

$$\overline{V}_{pcc,nq} = +\overline{\omega} L_{sn} \overline{I}_{nd} + R_{sn} \overline{I}_{nq} - \widehat{V}_{sn}\sin\overline{\rho}_0, \tag{18}$$

and

$$\widetilde{v}_{pcc,nd} = L_{sn}\frac{d\widetilde{i}_{nd}}{dt} - \widetilde{\omega} L_{sn}\overline{I}_{nq} - \overline{\omega} L_{sn}\widetilde{i}_{nq} + \\ + R_{sn}\widetilde{i}_{nd} - (\widehat{V}_{sn}\sin\overline{\rho}_0)\widetilde{\rho}, \tag{19}$$

$$\widetilde{v}_{pcc,nq} = L_{sn}\frac{d\widetilde{i}_{nq}}{dt} + \widetilde{\omega} L_{sn}\overline{I}_{nd} + \overline{\omega} L_{sn}\widetilde{i}_{nd} + \\ + R_{sn}\widetilde{i}_{nq} - (\widehat{V}_{sn}\cos\overline{\rho}_0)\widetilde{\rho}, \tag{20}$$

where $\cos(\omega_s t + \phi_{sn} - \rho) \approx \cos(\overline{\rho}_0 + \widetilde{\rho}) \approx \cos\overline{\rho}_0 - (\sin\overline{\rho}_0)\widetilde{\rho}$ and $\sin(\omega_s t + \phi_{sn} - \rho) \approx -\sin(\overline{\rho}_0 + \widetilde{\rho}) \approx -\sin\overline{\rho}_0 - (\cos\overline{\rho}_0)\widetilde{\rho}$, considering $\widetilde{\rho} << 1$.

The voltages, currents and angles in (17)–(20) with the symbol $(\bar{})$ represent the steady-state variables while the variables with the symbol $(\tilde{})$ represent small disturbances around an operating point. Considering a zero steady-state error for the PLL [10], it is possible to write the following small-signal relation, in the frequency domain, for the d- and q-axis neutral voltages:

$$\widetilde{V}_{pcc,nd}(s) = G_{nd}(s)\widetilde{I}_{nd}(s) - G_{nq}(s)\widetilde{I}_{nq}(s), \tag{21}$$

$$\widetilde{V}_{pcc,nq}(s) = G_{nd}(s)\widetilde{I}_{nq}(s) + G_{nq}(s)\widetilde{I}_{nd}(s), \tag{22}$$

where $G_{nd}(s) = (R_{sn} + sL_{sn})$ and $G_{nq}(s) = \overline{\omega} L_{sn}$.

As the fourth-leg of the DSTATCOM, connected to the neutral-wire, is controlled to synthesize the currents $i_0 = (i_a + i_b + i_c)/3$ and i_g, the following relations can be written:

$$\widetilde{I}_{nd}(s) = -\widetilde{I}_{gd}(s) - 3\widetilde{I}_{d0}(s), \quad (23)$$

$$\widetilde{I}_{nq}(s) = -\widetilde{I}_{gq}(s) - 3\widetilde{I}_{q0}(s), \quad (24)$$

where $\widetilde{I}_{gd}$ and $\widetilde{I}_{gq}$ are the d- and q-axis currents synthesized by the fifth-leg of the DSTATCOM and $\widetilde{I}_{d0}$ and $\widetilde{I}_{q0}$ are the d- and q-axis zero-sequence currents synthesized by the three phases of the DSTATCOM.

Therefore, (21) and (22) can be rewritten as follows:

$$\widetilde{V}_{pcc,nd}(s) = -G_{nd}(s)\widetilde{I}_{gd}(s) + G_{nq}(s)\widetilde{I}_{gq}(s) - \\ -3G_{nd}(s)\widetilde{I}_{d0}(s) + 3G_{nq}(s)\widetilde{I}_{q0}(s), \quad (25)$$

$$\widetilde{V}_{pcc,nq}(s) = -G_{nd}(s)\widetilde{I}_{gq}(s) - G_{nq}(s)\widetilde{I}_{gd}(s) - \\ -3G_{nd}(s)\widetilde{I}_{q0}(s) - 3G_{nq}(s)\widetilde{I}_{d0}(s). \quad (26)$$

Since the currents $\widetilde{I}_{d0}$ and $\widetilde{I}_{q0}$ will be used to compensate the zero-sequence imbalance in the PCC phase voltages, as shown in [10], they cannot ensure a null neutral voltage at the PCC. Thus, both voltages $\widetilde{V}_{pcc,nd}$ and $\widetilde{V}_{pcc,nq}$ can be controlled by the currents $\widetilde{I}_{gd}$ and $\widetilde{I}_{gq}$. However, in multi-grounding neutral distribution networks, the resistance R_{sn} cannot be neglected compared to ωL_{sn}, depending on the values of the system's grounding resistances. Then, the neutral voltage $\widetilde{V}_{pcc,nd}$ will be controlled by the current $\widetilde{I}_{gd}$, while the voltage $\widetilde{V}_{pcc,nq}$ will be controlled by the current $\widetilde{I}_{gq}$.

Fig. 6 shows the block diagram for the d- and q-axis neutral voltage control loops, where the disturbances were not represented for simplicity sake. The block $K_{vn}(s)$ is the neutral voltage controller while $H_{ig}(s)$ represents the closed-loop transfer function for the current control loop of Fig. 5, when an inner loop regulates the currents I_{gd} and I_{gq} synthesized by the fifth-leg of the DSTATCOM. The block with the unitary negative gain compensates the signal of the plant.

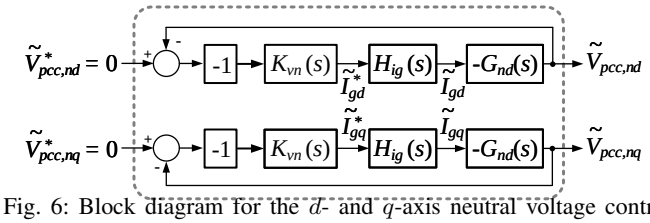


Fig. 6: Block diagram for the d- and q-axis neutral voltage control loops.

Based on the internal model principle, the controller $K_{vn}(s)$ can be chosen of the integral type to ensure null steady-state error. Thus, the following voltage closed-loop transfer function can be written for the block diagram of Fig. 6, assuming that the time constant of the closed-loop transfer function $H_{ig}(s)$ is much smaller than the voltage one:

$$H_{vn}(s) = \frac{1}{s\tau_{vn} + 1}, \quad (27)$$

where $\tau_{vn} = [(1/k_{vn}) + L_{sn}]/R_{sn}$ is the time constant of the neutral voltage closed-loop; k_{vn} is the gain of the integral controller $K_{vn}(s) = k_{vn}/s$ and $H_{ig}(s) = 1$. The gain k_{vn} can then be calculated by choosing $\tau_{vn} \geq (10\tau_{ig})$.

IV. Results of Digital Simulations

The multi-grounded neutral distribution network shown in Fig. 1 and the $3\phi5w$–DSTATCOM depicted in Fig. 2 were modelled in the electromagnetic transient program PSCAD/EMTDC to demonstrate the effectiveness of the voltage unbalance and neutral voltage compensation strategy proposed in this work. The parameters of the network are given in Table I, Table II and Table III while the parameters of the DSTATCOM and its voltage and current controllers are given in Table IV and Table V, respectively.

The DSTATCOM was connected to the Bus 1 of the multi-grounded network. The DSTATCOM controllers were discretized using the bilinear approximation and implemented digitally, considering a sampling frequency of 25 kHz. All digital simulation studies were carried out considering a time step of 4 µs.

A sinusoidal pulse-width modulation strategy was used to generate the switching pattern for each leg of the DSTATCOM [16]. A DSOGI-PLL synchronizes the voltages and currents at the DSTATCOM terminals with the PCC voltages [15]. A PI-controller forces the DSTATCOM to drain or supply positive-sequence current from the mains in order to regulate the DC terminal voltage, as shown in [9].

For comparison purposes, the results of three digital simulations will be presented and analysed: (*i*) the performance of the $3\phi5w$–DSTATCOM, compensating for the neutral voltage at the PCC, will be compared with that of the $3\phi4w$–DSTATCOM, (*ii*) the performance of $3\phi5w$–DSTATCOM to compensate for the neutral voltage at the PCC when the multi-grounded network faces a high-impedance single-phase fault to earth, and (*iii*) the effectiveness of the $3\phi5w$–DSTATCOM compensating the neutral-voltage at the PCC will be investigated when the multi-grounded network faces a single-phase fault to ground.

A. Neutral-voltage compensation with the $3\phi5w$–DSTATCOM

This section compares the performance of the $3\phi5w$–DSTATCOM, regulating the positive-sequence voltage and compensating for the negative-sequence, zero-sequence and neutral voltages at the PCC, with the $3\phi4w$–DSTATCOM.

Fig. 7 (a), (b), (c), (d) and (e) shows the PCC three-phase voltages, the instantaneous currents synthesized by the $3\phi5w$–DSTATCOM, the *rms* value of the PCC positive-sequence voltage, the *rms* value of the PCC negative-sequence, zero-sequence and neutral voltages, and the DC terminal voltage of the DSTATCOM, respectively. The current synthesized by the fifth-leg of the DSTATCOM is controlled as described in Section III-A in order to compensate the the PCC neutral voltage, as discussed in Section III-B. The other four-legs of the DSTATCOM are controlled by algorithms similar to those shown in [10] and [9]. Fig. 7 (c) shows that the *rms* value of the positive-sequence voltage is regulated to the setup value (dashed-line), while Fig. 7 (d) depicts that the *rms* value of negative-sequence, zero-sequence and neutral-voltages at the PCC go to zero for $t > 0.3$ s. Note that the instantaneous waveforms of the three-phase voltages at the PCC become balanced (Fig. 7 (a)) after the $3\phi5w$–DSTATCOM starts to operate.

Fig. 8 (a), (b), (c), (d) and (e) shows the PCC three-phase voltages, the instantaneous currents synthesized by the $3\phi4w$–DSTATCOM, the *rms* value of the PCC positive-sequence voltage, the *rms* value of the PCC negative-sequence, zero-sequence and neutral voltages and the DC terminal voltage of the DSTATCOM, respectively. In this simulation, the pulses sent to the IGBTs of the DSTATCOM's fifth-leg are blocked. Note that although the *rms* value of the positive-sequence voltage is set to the reference value (Fig. 8 (c)), and the *rms* value of negative- and zero-sequence voltages at the PCC are fully compensated, the neutral-voltage is not cancelled by the $3\phi4w$–DSTATCOM.

The comparison of Fig. 7 (d) and Fig. 8 (d) demonstrates the effectiveness of the $3\phi5w$–DSTATCOM to compensate for neutral-voltage in a multi-grounded network. Fig. 7 (e) and Fig. 8 (e) show that the DC voltage of both DSTATCOMs oscillates with twice the grid fundamental frequency. This behaviour is due to the synthesis of

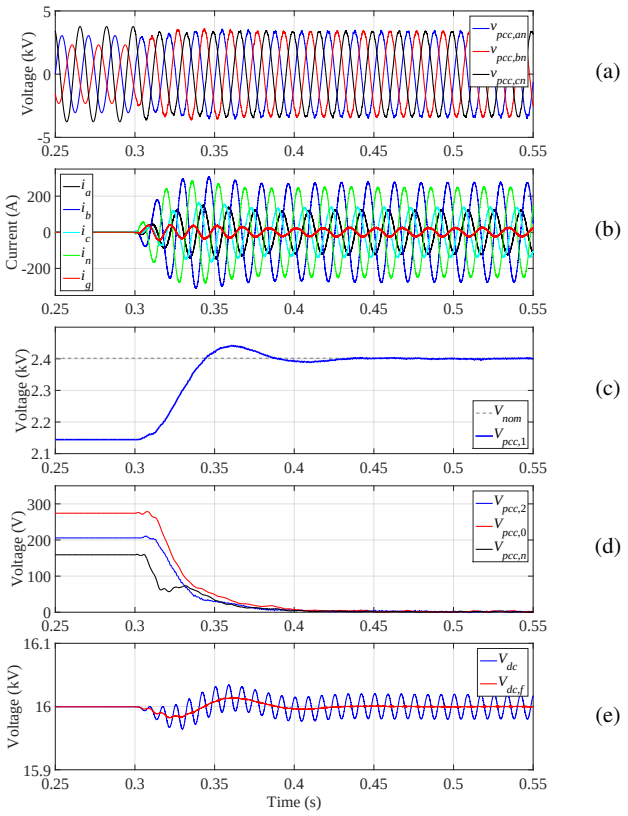


Fig. 7: Waveforms for $3\phi5w$–DSTATCOM: (a) three-phase PCC voltages, (b) DSTATCOM currents, (c) *rms* value of the PCC positive-sequence voltage, (d) *rms* value of the PCC negative-sequence, zero-sequence and neutral voltages and (e) DC terminal voltage of the DSTATCOM.

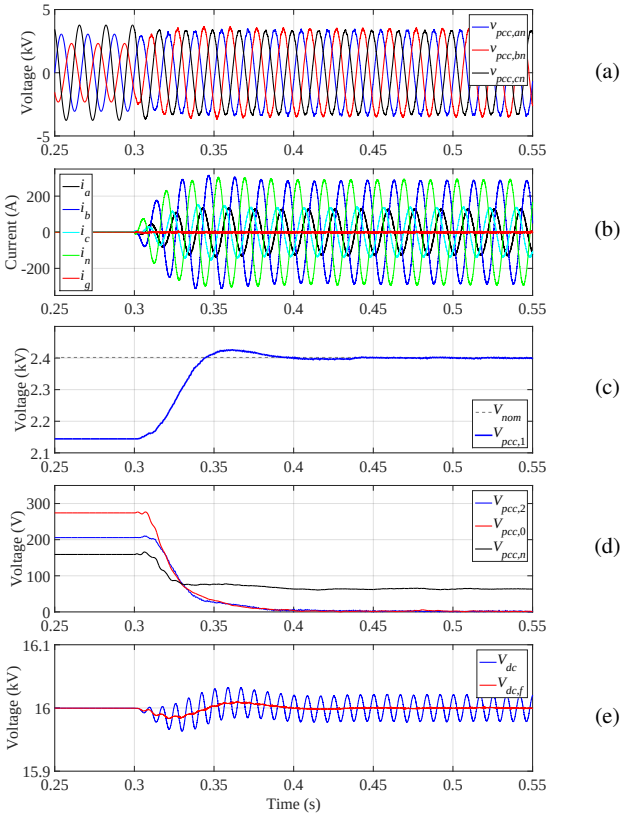


Fig. 8: Waveforms for $3\phi4w$–DSTATCOM: (a) three-phase PCC voltages, (b) DSTATCOM currents, (c) *rms* value of the PCC positive-sequence voltage, (d) *rms* value of the PCC negative-sequence, zero-sequence and neutral voltages and (e) DC terminal voltage of the DSTATCOM.

unbalanced currents by the DSTATCOM to compensate for voltage imbalances at the PCC. It can be minimized by carefully designing the capacitance of the DSTATCOM.

Fig. 9 (a), (b), (c) and (d) shows the waveforms of the currents that flow through Feeder 1 and Feeder 2, and the terminals of the Load 1 and Load 2, respectively. Fig. 10 (a) and (b) show the instantaneous active and reactive powers measured at the terminals of Load 1 and Load 2, respectively. The previous results were obtained considering the $3\phi5w$–DSTATCOM connected to Bus 1 of the multi-grounded network.

B. Performance of $3\phi5w$–DSTATCOM during phase-to-ground high-impedance fault

This section investigates the performance of the $3\phi5w$–DSTATCOM when occurs a phase-to-ground high-impedance fault in the multi-grounded network of Fig. 1. This type of fault is very common and it is difficult to detect due to the low value of the short-circuit currents.

Fig. 11 (a), (b), (c), (d) and (e) show the three-phase instantaneous voltages at the PCC, the currents synthesized by the $3\phi5w$–DSTATCOM, the *rms* value of the PCC neutral voltage, the *rms* values of the PCC phase voltages and the DC terminal voltage of the DSTATCOM, respectively. The failure was emulated by connecting an impedance of 10 Ω between the phase "*b*" of Bus 2 and the ground in $t = 0.3$ s. Fig. 11 (a) shows that the network neutral voltage increases after the fault occurs. However, the loads are kept connected to the grid. In $t = 0.4$ s, the $3\phi5w$–DSTATCOM starts to regulate the positive-sequence voltage and compensate the negative-

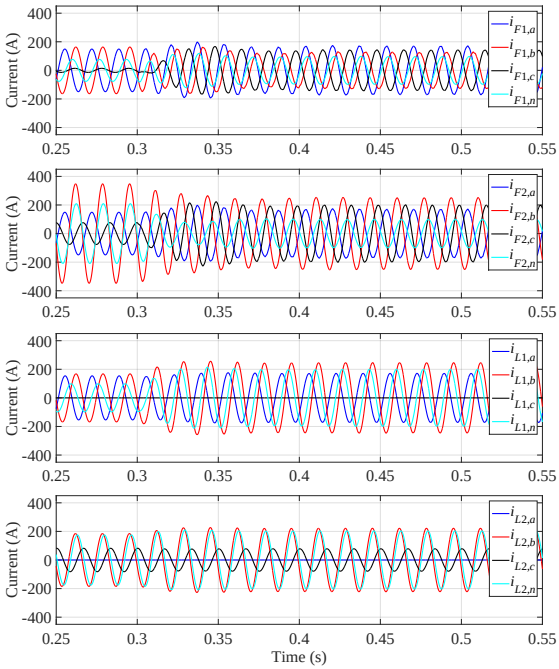
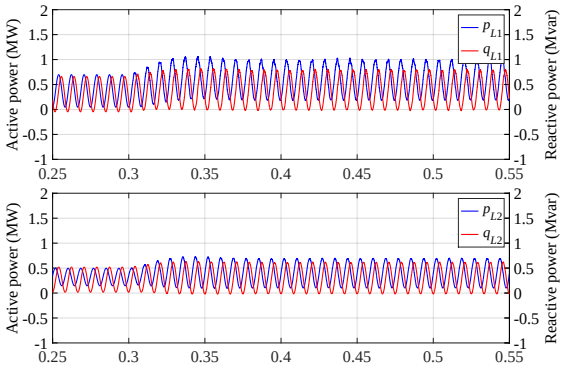


Fig. 9: Currents waveforms of $3\phi5w$–DSTATCOM: (a) Feeder 1, (b) Feeder 2, (c) Load 1 and (d) Load 2.

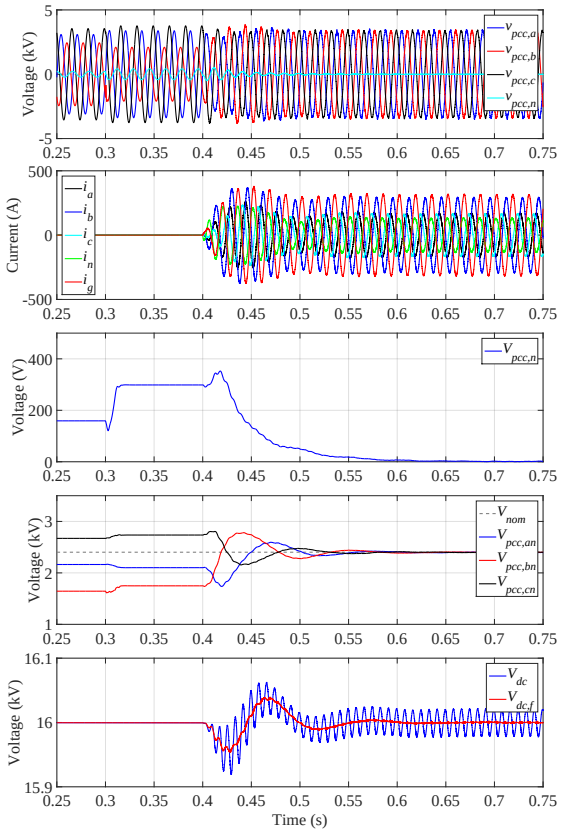


(a)

(b)

Fig. 10: Active and reactive powers: (a) Load 1 and (b) Load 2.

sequence, zero-sequence and neutral voltages at the PCC. Fig. 12 (a), (b), (c), and (d) shows the waveforms of the currents that flow through Feeder 1 and Feeder 2, and the terminals of the Load 1 and Load 2, respectively.



(a)

(b)

(c)

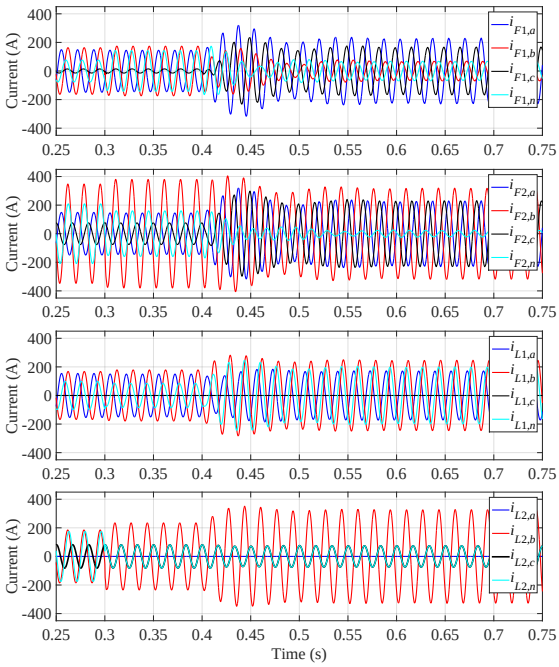
(d)

(e)

Fig. 11: Waveforms during high-impedance fault to ground: (a) three-phase voltages at the PCC, (b) currents synthesized by the DSTATCOM, (c) *rms* value of the PCC neutral voltage, (d) *rms* value of the PCC phase voltages and (e) DC terminal voltage of the DSTATCOM.

C. Performance of 3ϕ5w–DSTATCOM during phase-to-ground low-impedance fault

This section will investigate the effectiveness of the 3ϕ5w–DSTATCOM when the multi-grounded network faces phase-to-ground low-impedance fault. During this event, the static compensator must synthesize high currents to compensate for the network imbalance caused by the single-phase fault.



(a)

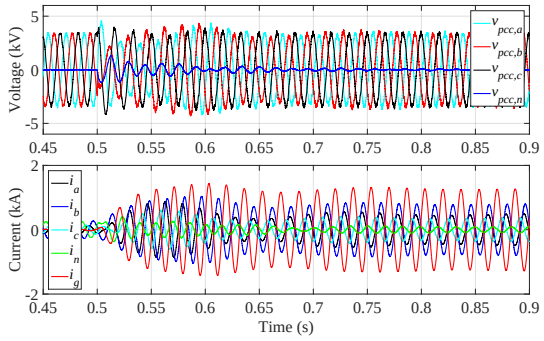
(b)

(c)

(d)

Fig. 12: Currents waveforms for phase-to-ground high-impedance fault: (a) Feeder 1, (b) Feeder 2, (c) Load 1 and (d) Load 2.

Fig. 13 (a) and (b) shows the three-phase instantaneous voltages at the PCC and the currents synthesized by the 3ϕ5w–DSTATCOM, respectively. The low-impedance fault was emulated by connecting an impedance of 2 Ω between the phase "b" of Bus 2 and the ground in $t = 0.5$ s. Then, the 3ϕ5w–DSTATCOM increases its terminal currents to regulate the positive-sequence voltage and compensate the negative-sequence, zero-sequence and neutral voltages at the PCC. The comparison of Fig. 11 (b) and Fig. 13 (b) shows that the currents synthesized during the low-impedance fault are higher than those shown in the previous section. In this case, the 3ϕ5w–DSTATCOM must be carefully redesigned so that the semiconductor switches can process these high currents. Despite this drawback, the neutral voltage goes to zero in approximately 0.25 s after the DSTATCOM starts to operate.



(a)

(b)

Fig. 13: Waveforms for phase-to-ground low-impedance fault: (a) instantaneous three-phase voltages at the PCC and (b) currents synthesized by the DSTATCOM.

V. Conclusions

This paper presented a new three-phase five-wire DSTATCOM topology to be connected in multi-grounded neutral distribution net-

works. Besides regulating the DC terminal voltage, the PCC positive-sequence voltage and compensating the negative- and zero-sequence voltage at the PCC, the static compensator could also compensate the PCC neutral voltage. Mathematical modellings were developed in order to derive the current and voltage control loops to control the fifth-leg of the DSTATCOM as a single-phase converter. In this way, a second-order generalized integrator (SOGI) and a transport delay buffer were used to generate quadrature components for the neutral-voltage and the current synthesized by the $3\phi5w$–DSTATCOM's fifth-leg, respectively. Results of digital simulations, in the time-domain, were also presented in order to demonstrate the voltage unbalance and neutral voltage compensation in the multi-grounded distribution network and to validate the control loops developed for $3\phi5w$–DSTATCOM. Although the results of the $3\phi4w$–DSTATCOM and $3\phi5w$–DSTATCOM simulations demonstrated that both topologies control the positive-, negative- and zero-sequence voltages, only the $3\phi5w$–DSTATCOM can compensate for the neutral voltage. In addition, the $3\phi5w$–DSTATCOM improved the network voltage profile even during phase-to-ground high- and low-impedance faults. Nevertheless, compensation for imbalances during low-impedance faults will require DSTATCOM to be redesigned to handle high amplitude currents.

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APPENDIX

Parameters of the multi-grounded electrical network and DSTATCOM.

TABLE I: Network parameters

Parameter	Value
Line rms voltage (V_s)	4.16 kV
Fundamental frequency (f_s)	60 Hz
Grounding resistance (R_g)	5 Ω
Grounding resistance of load 1 (R_{g1})	7 Ω
Grounding resistance of load 2 (R_{g2})	7 Ω

TABLE II: Impedances of the feeders

Phase	Value
a	$0.38 + j1.7342\ \Omega$
b	$0.38 + j1.7342\ \Omega$
c	$0.38 + j1.7342\ \Omega$
n	$0.38 + j1.7342\ \Omega$

TABLE III: Impedances of the loads

Bus	Phase	Value
1	a	$17.22 + j9.74\ \Omega$
1	b	$11.15 + j8.12\ \Omega$
2	b	$11.15 + j8.12\ \Omega$
2	c	$38.24 + j21.93\ \Omega$

TABLE IV: Parameters of the DSTATCOM

Parameter	Value
Equivalent capacitance (C_{eq})	3 mF
DC voltage (V_{dc}^*)	16 kV
Inductance of the interface filter (L_i)	24 mH
Resistance of the interface filter (R_i)	90 mΩ
Capacitance of the interface filter (C_i)	10 μF
Resistance of the capacitor (R_{Ci})	5 Ω
Resistance of the IGBTs (R_{igbt})	13 mΩ
Switching frequency (f_{sw})	9 kHz
Gain of the SOGI (k)	4.2

TABLE V: Controller gains of the DSTATCOM

Controller	Gain	Value
K_{i1}, K_{i2}, K_{i0} and K_{ig}	Proportional	48 V/A
	Integral	206 V/As
K_{vdc}	Proportional	39.2 μA/V^2
	Integral	1.3 mA/V^{2}s
$K_{v1}(s)$ and $K_{v2}(s)$	Integral	22 A/Vs
$K_{v0}(s)$	Integral	12.4 A/Vs
$K_{vn}(s)$	Integral	28.3 A/Vs

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