PERFORMANCE ASSESSMENT USING EMTP OF TWO GATE FIRING UNITS FOR HVDC CONVERTERS OPERATING WITH WEAK AC SYSTEMS

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Abstract: The firing pulse generation unit of a static converter has a significant impact on the transient performance of the converter. For HVDC applications, a voltage controlled oscillator in conjunction with a phase locked loop are used to generate equi-distant firing pulses so that a satisfactory transient performance can be achieved even with relatively weak ac systems. In this paper, the design and dynamic performance of two gate firing control units, both based on pulse frequency control, are assessed using EMTP.

Keywords: gate firing unit, PLL, VCO

INTRODUCTION

EMTP based simulators are being used in utilities for HVDC transmission system studies. One of the key elements in a HVDC control system is the gate firing unit of a static converter. Some of the work previously reported on the modelling of HVDC control systems [1,2] assume infinite ac systems and are found not suitable for modelling realistic HVDC systems with weak ac systems. Modelling of HVDC systems with weak ac systems using EMTP based packages has been documented in [3,4]. In these reports, however, very limited information is provided regarding analysis and design of a practical gate firing unit. Therefore, a description of a basic design procedure for a gate firing unit is still necessary so that it can be readily adopted for HVDC system studies in EMTP.

The application of Voltage Controlled Oscillators (VCO) to HVDC converter firing control was first described in [5]. This method derived equi-distant firing pulses for the converter valves and, to a large extent, decoupled the impact of any commutation ac voltage distortion on the valve triggering [6]. This made it feasible for the successful operation of converters with relatively weak ac systems having Short Circuit Ratios (SCRs) of less than 3. Increasingly, as economic pressures force utilities to consider still weaker ac systems (with SCRs of less than 2), problems of harmonic instability are being experienced.

One common type of gate firing unit, here after referred to as the conventional type, is based on a VCO in conjuction with a Phase Locked Loop (PLL) [7]. Another type of gate firing unit, referred to as the *Transvektor* type [8,9], has an ac to DQ transformation stage in the circuit. This DQ-type has been used in motor drive applications for many years. Its first application to an HVDC system was made at Chateauguay, Quebec in the middle 1980's.

The objective of this paper is to assess the design and performance of these two types of gate firing units under both steady state and dynamic conditions. The operational principles of these two circuits are briefly reviewed and the procedure of designing the circuits are described. The circuits are then tested under fault and harmonic distortion conditions. An HVDC rectifier system based on the CIGRE benchmark system [10] is studied using EMTP and results are provided for comparison.

REVIEW OF GATE FIRING UNITS

There are two types of gate firing units which have been widely used; one based on Individual Phase Control and the other on Equi-Distant Pulse control.

Individual Phase Control (IPC) Unit

In this type of gate firing unit, the firing pulses are directly derived from the zero crossover points of the commutation voltage. Consequently, the firing pulses are vulnerable to harmonic pollution on the waveform. Early attempts to use filtering techniques to alleviate some of these problems were not successful for operation with weak ac systems due to the introduction of phase shifts. Recent developments in tracking band-pass filters [11] which derive the fundamental frequency component of the commutation voltage with no phase shift may be useful in operation with weak ac systems. However, the main disadvantage of IPC systems, which eventually led to their demise, was the generation of non-characteristic harmonics which caused harmonic instability problems.

Equi-Distant Pulse Control (EPC) Unit

EPC systems generate only characteristic harmonics during steady state operation. Two gate firing units of this type have been described in the literature:

a) Pulse Frequency Control (PFC) Type.
To decouple the direct dependence of the pulse firing from the zero crossover points of the commutation voltage, a VCO followed by a ring counter is used [5,12]. The characteristic feature of this method is that a dc input control signal to the VCO results in a frequency change of the VCO. For this reason, this type of gate firing unit is referred to as of the PFC type [13].

The free running VCO generates a train of short pulses at a pulse repetition frequency directly proportional to the dc control voltage. For example, if the control voltage is adjusted such that the oscillator frequency is at 6 times the ac supply frequency, then the pulses will be exactly at 60° intervals (and hence the term equi-distant firing pulses). A ring counter is used to separate the pulse train into 6 sets of pulses for a 6-pulse converter.

An indirect method is used to synchronize the VCO output frequency to the ac supply frequency. An error signal is derived from either the converter dc current or extinction angle controller as a feedback signal. When the error signal is zero, the gate firing unit is in steady state (free running or at a centre frequency) and the VCO output frequency will be at supply frequency. When there is an error, the VCO will either speed up or slow down to cor-

rect for the error. Both [5] and [12] use the dc current controllers for synchronizing the VCO when the converter is a rectifier; however, when the converter is an inverter, the VCO synchronizing is based on an extinction angle controller, although the method used by [12] is based on a predictive estimation of extinction angle.

b) Pulse Phase Control (PPC) Type.
In a gate firing unit of this type [13], the dc control voltage resulted in a change to the phase of the VCO output rather than its frequency. The transfer function of this type of unit is therefore proportional rather than integral. To ensure the synchronizm of the VCO output frequency with the ac supply frequency, a slower acting frequency error feedback loop is used. This type of gate firing unit does not permit the modulation of firing pulses on an individual basis either.

GATE FIRING UNITS - DESIGN AND ANALYSIS

Conventional Gate Firing Unit.

The block diagram of a conventional gate firing unit is shown in Figure 1.

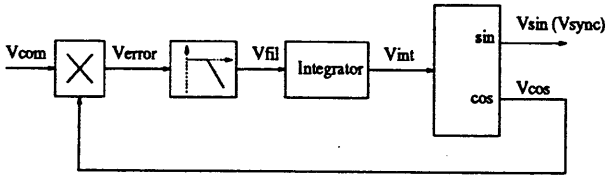

Figure 1: Block diagram of conventional gate firing unit

In this circuit, the commutation voltage, assumed to be Vcom = $1\sin(\omega_1 t + \theta_1)$, is multiplied by a feedback signal, Vcos = $1\cos(\omega_2 t + \theta_2)$. The output voltage Verror is obtained according to eq.(1)

$$V_{error} = 1\sin(\omega_1 t + \theta_1)\,1\cos(\omega_2 t + \theta_2)$$

$$V_{error} = 0.5\sin[(\omega_1 - \omega_2)t + (\theta_1 - \theta_2)] + 0.5\sin[(\omega_1 + \omega_2)t + (\theta_1 + \theta_2)] \quad (1)$$

The first term of eq.(1) represents the error between the synchronizing voltage and the commutation voltage due to the frequency and phase difference. Under steady state, the synchronizing voltage will be locked to the commutation voltage. In this case $\omega_1 \Rightarrow \omega_2$ and $\theta_1 \Rightarrow \theta_2$, and the first term of eq.(1) approaches zero. The second term is an unwanted ac component which has a frequency of $2\omega_1$ under steady state. In order to extract the dc error signal and filter out the unwanted ac component, a low-pass filter having the transfer function $\omega_c/(s+\omega_c)$ is used. The output is passed onto an integrator with a transfer function of $1/sT_i$. The integrator output, Vint, is used to modulate the phase and frequency of a free-running Sine-Cosine Oscillator to generate the output signal Vsync. Under steady state conditions, the feedback signal Vsync will be in phase and at the same frequency as the commutation voltage, Vcom. Thus Vsync can be used as a stable pollution-free signal to derive the zero-crossover points to provide the timing reference points for the gate firing unit..

Figure 2 shows the waveforms of the conventional gate firing unit shown in Figure 1. The error signal contains a dominant second harmonic ac component which is

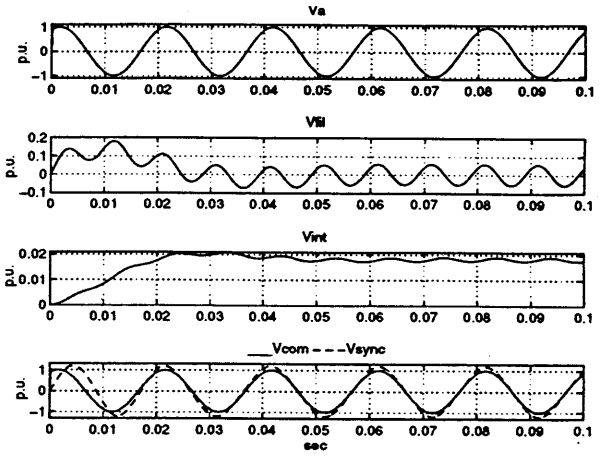

Figure 2: Waveforms of conventional gate firing unit

removed by a low-pass filter thus minimizing its impact on the overall system operation. The bottom superimposed signals in Figure 2 show the commutation voltage Vcom and the synchronizing voltage Vsync. Note that, in order to see clearly the phase difference of the two signals, the magnitude of Vsync has been deliberately increased by 20%

There are two parameters that need to be designed in the circuit of Figure 1. One is the cut-off frequency of the low-pass filter, and the other is the integrator time constant. The design objective is to achieve synchronization between Vsync and Vcom in the shortest time possible. One common design approach is to study the small signal model of the circuit and design the parameters in the frequency domain. Studies show [7] that the small signal model of the circuit in Figure 1 can be represented as shown in Figure 3 where H(s) is the low-pass filter transfer function and variables in hats represent small signal quantities. The loop transfer function is given in eq.(2).

$$T_{l1} = \left(\frac{\omega_c}{s+\omega_c}\right)\left(\frac{1}{sT_i}\right) \quad (2)$$

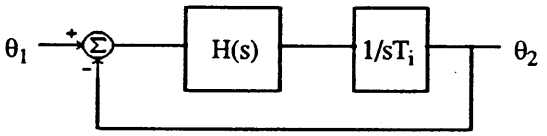

Figure 3: Small signal model of conventional gate firing unit

Figure 4 gives the Bode plot of the loop transfer function. In this figure, the solid line represents the response of the loop transfer function $T_{l1}(s)$, and the dotted lines are for the low-pass filter function H(s) and the integrator function $1/sT_i$. This figure shows that, in order to achieve the optimum phase margin of around 60°, the integrator time constant should be selected such that the value of $1/T_i$ is smaller than ω_c, the cut-off frequency of the low-pass filter.

Figure 4 also shows that the loop response speed, represented by the gain-crossover frequency, is to a large extent, limited by the cut-off frequency ω_c of the low-pass filter. There is a compromise in selecting ω_c. If ω_c is too high, the ac component remains large and it will interfere with the system operation. On the other hand, if ω_c is too low, the overall system response of the system will be very sluggish. Our simulation studies show that a

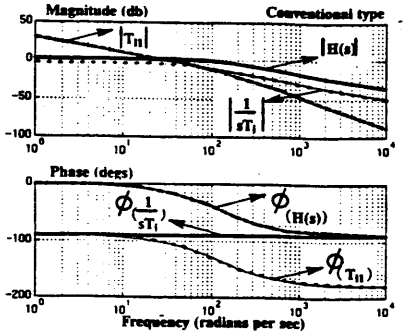

Figure 4: Bode plot for the loop transfer function of eq.(2)

cut-off frequency around one fifth of the ac component ($2\omega_c$) gives satisfactory results.

DQ-type Gate Firing Unit

The block diagram of the DQ-type gate firing unit and its corresponding signals are shown in Figure 5 and Figure 6 respectively.

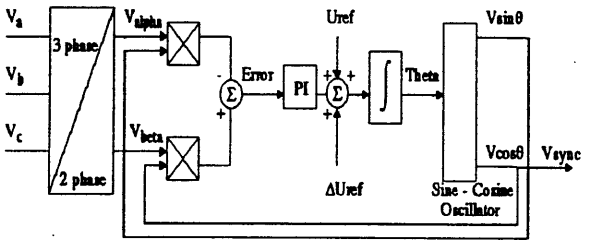

Figure 5: block diagram of DQ-type gate firing unit

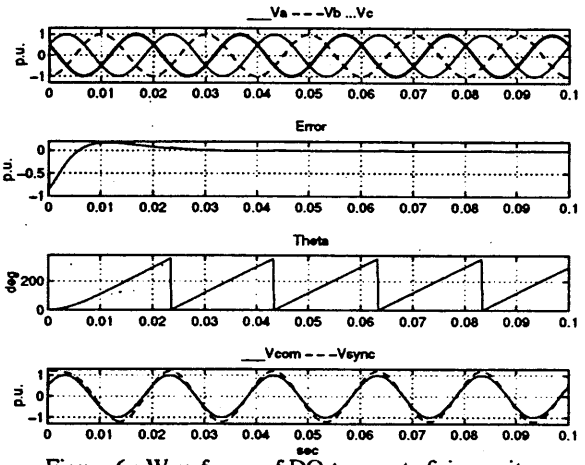

Figure 6 : Waveforms of DQ-type gate firing unit

The three phase commutation voltages Va, Vb and Vc are transformed into DQ axis voltages V-alpha and V-beta using eq.(3) and eq.(4) respectively.

$$Valpha = (\frac{2}{3})V_a - (\frac{1}{3})V_b - (\frac{1}{3})V_c \qquad (3)$$

$$V_{beta} = \left(\frac{1}{\sqrt{3}}\right)(V_b - V_c) \qquad (4)$$

$$Error = -V_{alpha}V\sin\theta + V_{beta}V\cos\theta \qquad (5)$$

An error signal, derived using eq.(5), is fed through a PI controller to generate a reference value for the VCO. This reference value can be modulated by a signal ΔUref, and it has a fixed voltage bias Uref which sets the center frequency of the VCO. The output of the VCO is a signal proportional to a sawtooth waveform (an angle Theta). This waveform is used to generate the Sine-Cosine waveforms which are fed back to the multipliers to generate the error signal. Under steady state, this error is reduced to zero and the output of the Sine-Cosine oscillator will be in synchronizm with the commutation voltages. In Figure 6, the outputs Vsync and Va are compared; note that the magnitude of Vsync has been deliberately increased by 20% to see clearly the phase relationship between these two signals.

The small signal block diagram of the DQ-type gate firing unit is shown in Figure 7,where $G(s) = K_{pi}(1+sT_{pi})/sT_{pi}$ representing the PI transfer function. The loop transfer function is given in eq.(6).

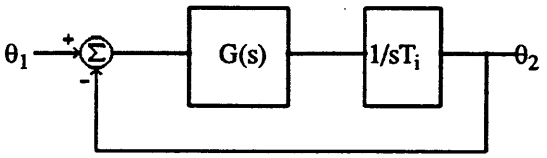

Figure 7: Small signal block diagram of DQ-type unit

$$T_{l2}(s) = K_{pi}\left(\frac{1+sT_{pi}}{sT_{pi}}\right)\left(\frac{1}{sT_i}\right) \qquad (6)$$

The Bode plot of $T_{l2}(s)$ is shown in Figure 8. The solid lines are for the loop transfer function $T_{l2}(s)$ and the dotted lines are for the PI controller and the integrator transfer functions. From Figure 8, it can be concluded that, in order to achieve the optimum phase margin of around 60°, the value of $1/T_i' = K_{pi} / T_i$ should be larger than $1/T_{pi}$. Also, since the phase lag approaches 90° as the frequency increases, theoretically the gain-crossover frequency can be chosen as high as one wishes. Practically, this frequency will be limited in a realistic system. One of the limiting factors is the existence of the low order harmonic component in the error signal when the three-phase ac source contains harmonics. For example, with a third harmonic injection at the ac bus, the error signal will contain a second harmonic ac component. Under such operating conditions, as the gain crossover frequency increases, the error between the synchronizing signal (Vsync) and the fundamental component of the commutation voltage (Vcom) increases as well. Our studies show that the gain crossover frequency of around 40 Hz provides a good compromise between a fast response and a small synchronizing error.

Comparison

The major difference between the operational behavior of the conventional and DQ-type gate firing units is the presence of the ac harmonic component in the error signal under normal operating conditions. In the conventional gate firing unit, a large second harmonic ac component exists and a low-pass filter is required in the loop. While in the DQ-type gate firing unit, there is no such ac component in the error signal. The absence of the low-pass filter allows the DQ-type circuit to achieve a much faster dynamic response than its conventional

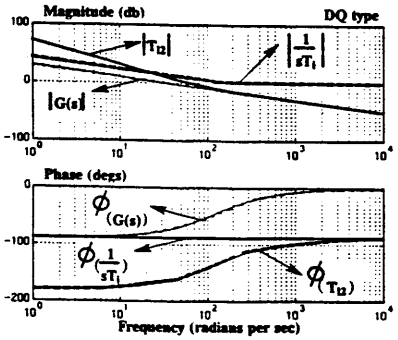

Figure 8: Bode plot for the loop transfer function of eq.(6)

counterpart. Experience also shows that the optimization of the low-pass filter requires additional effort when compared to the DQ-type circuit.

TESTS ON GATE FIRING UNITS

Loss of Synchronization Voltage

Figure 9a shows the internal signals from the conventional gate firing unit during a temporary loss of the commutation voltage caused by a fault on the ac commutation bus. The multiplier output Verror and the low-pass filter output Vfil are reduced to zero during the fault period. The Integrator output Vint shows only a small offset voltage during the fault period which is used to modulate the frequency and phase of the Sine-Cosine oscillator stage following it. The post-fault synchronization dynamics of the conventional gate firing unit show that the output voltage Vsync is able to synchronize with the commutation voltage Vcom within 1 cycle (20 ms at 50 Hz). The waveform of Vint also shows that the control loop is slightly underdamped and requires a settling time of about 3 cycles.

Figure 9b shows the internal signals from the DQ-type gate firing unit during a temporary loss of the commutation voltage caused by a three phase fault on the ac commutation bus. During the fault, the three phase commutation voltages Va, Vb and Vc are reduced to zero causing the Error input to the PI controller to drop to zero. This results in the output of the sawtooth waveform, Theta, to be at the centre frequency (50 Hz). After the fault, the error is reduced to zero within 1 cycle (20 ms).

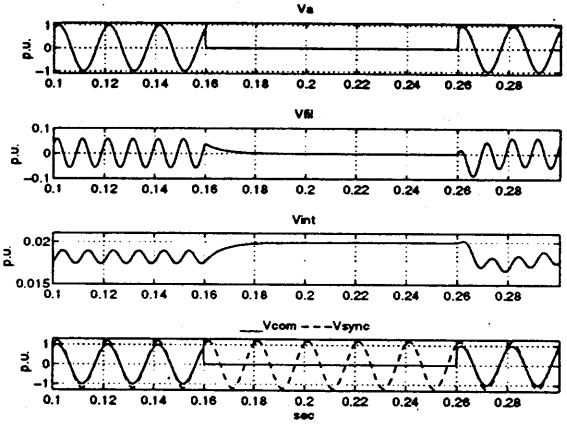

Figure 9a: Loss of synchronization voltage for conventional unit

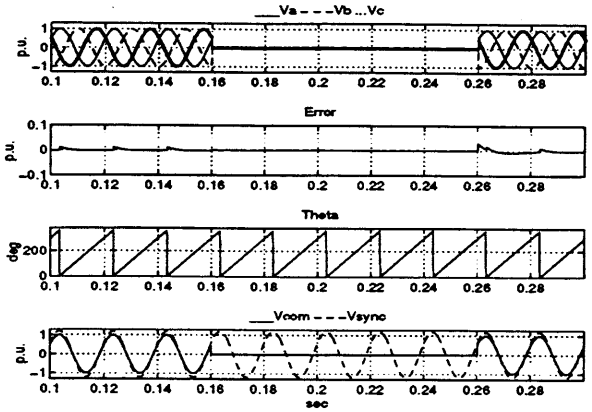

Figure 9b: Loss of synchronization voltages for DQ-type uni

Harmonic Distortion Test

Figure 10a shows the internal signals from the conventional gate firing unit with 30% injection of a third harmonic voltage on the commutation voltage. This harmonic level distorts the outputs of the multiplier and other stages in the gate firing unit. Never-the-less, the Vsync output voltage of the gird firing unit contains no harmonics and is synchronized to the fundamental component of the commutation voltage. Similarly Figure 10b shows the corresponding signals with the DQ-type gate firing unit. Although, the Verror signal contains a second harmonic component, the integrator output Theta smooths the impact of this ac component considerably. The Vsync output voltage of the DQ-type unit contains no harmonics and is synchronized to the fundamental component of the commutation voltage.

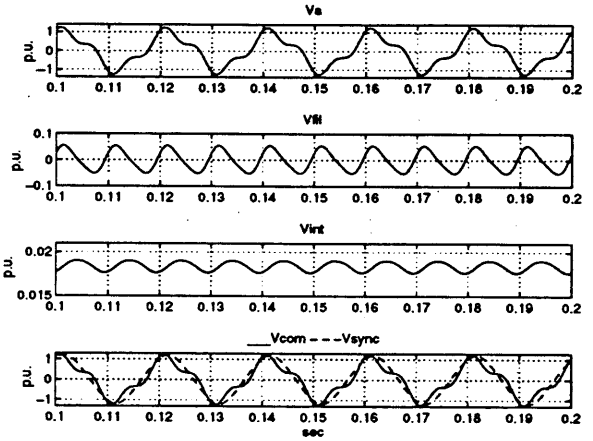

Figure 10a: Harmonic distortion test with conventional unit

EMTP SIMULATION OF A TEST SYSTEM

An HVDC rectifier system (Figure 11) based on the CIGRE Benchmark system [10] is used as the test system. Since a 6 pulse version of the converter system is modelled, it is necessary to add 5th and 7th harmonic ac filters. Only a 6 pulse model is used here to minimize the simulation time. However, the same design principles and the operational characteristics for the gate firing units can be extended to a 12 pulse unit.

The block diagram of the current controller used with this system is shown in Figure 12. The measured dc current Id is compared to a current order Iref, and a current error signal is generated. This current error is fed to a block,

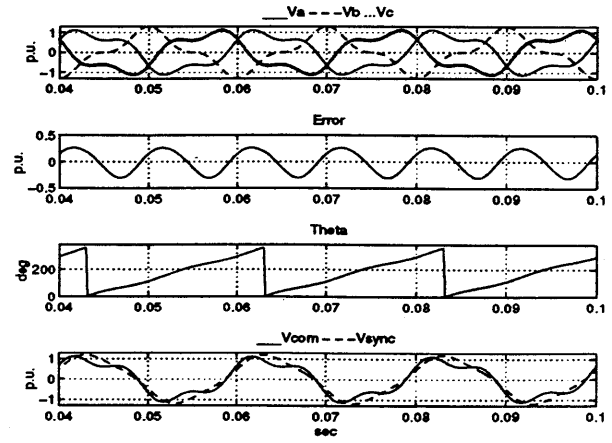

Figure 10b: Harmonic distortion test with DQ-type unit

other input of which is a delayed step input FORAND. The delayed step input keeps the input to the PI controller zero for 0.02s; this effect contributes in reducing the initialization time of the simulation.The PI controller generates an alpha order signal which is limited between 5° and 170°. This signal is fed to a gating unit which uses the synchronized voltage Vsync, to generate a firing pulse train. A ring counter is used to separate the firing ulses for the 6 thyristor valves of the converter.

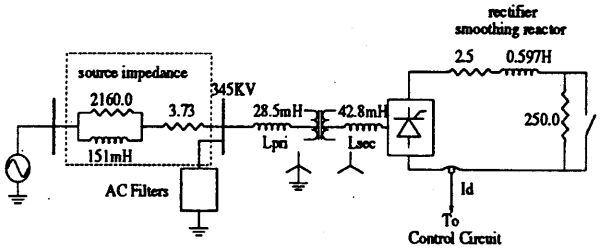

Figure 11: CIGRE benchmark rectifier system model.

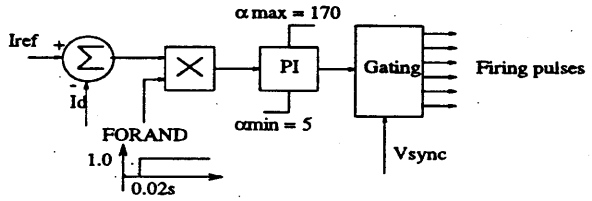

Figure 12: Block diagram of current controller

Start-up of System Model

Figures 13a and 13b show the start-up of the rectifier system with the conventional and DQ-type gate firing units, respectively. In both cases the start-up was achieved rapidly and the gate firing units are able to synchronize within 1 cycle. A detailed examination shows that the DQ-type unit is marginally faster

10% Step Change in Current Order

Figures 14a and 14b show the case of a 10% step change in current order for the rectifier system with the conventional and DQ-type gate firing units respectively. The signals shown are the dc current I_d, alpha order and the superimposed values of the synchronizing voltage (1.2*Vsync) and the commutation voltage Vcom. For the conventional unit, the step change is effected in 30ms, and the response is well controlled and stable. For the DQ-type unit, the step change is slower and takes about 50 ms. Both units are able to maintain synchronizm with the commutation voltage without any noticeable delays.

Single Phase Fault

Figures 15a and 15b show the case of a single phase fault for the rectifier system with the conventional and DQ-type gate firing units respectively. The signals shown are the dc current Id, alpha order and the superimposed values of the synchronizing voltage (1.2*Vsync) and the commutation voltage Vcom. In both tests the recoveries are well controlled and stable although the DQ-type unit is slightly faster. The presence of a large second harmonic component in the dc current (a characteristic of the unbalanced fault in the ac system and the modulation effect of the converter) does not effect the operation of the firing units noticeably and they maintain synchronizm through the fault period.

CONCLUSIONS

This paper has provided detailed information and performance results of two typical gate firing units used in practical HVDC systems. A performance comparison between the two gate firing units showed that they are equally capable of operation in a weak ac system having high levels of pollution and harmonic distortion in the commutation voltage. On the other hand, due to the absence of a low-pass filter in its control loop, the DQ-type gate firing unit is relatively easier to design and is faster than the conventional type. This design information will be useful to utility planners using EMTP based simulators for HVDC system studies

REFERENCES

1. N. Mohan, "Computer Exercises for Power Electronics Education ", University of Minnesota, 1990.
2. R. H. Lasseter et al,"EMTP Workbook Volume IV (TACS) - EL-4651", EPRI Research Project 2149, Final Report, June 1989.
3. D. A. Woodford, "Validation of Digital Simulation of DC Link", IEEE Trans. on Power Apparatus and Systems, PAS -104, No 9, Sept. 1985, pp 2588-2596.
6. D. Goldsworthy and J. Vithayathil, "EMTP model of an HVDC System", IEEE Montech 86, Conf. on HVDC Power Transmission, Sept 29 - Oct 1, 1986.
7. J. D. Ainsworth, "The Phase-Locked oscillator: A new control system for controlled static converters", IEEE Trans. Power App. System, Vol. PAS-87, 1968.
8. J. D. Ainsworth, "Harmonic instability between controlled static converter and ac networks", Paper 5321, Proc. IEEE May, 1967.
9. D. H. Wolaver,"Phase locked Loop Circuit Design" Prentice Hall, Inc 1991.
10. K. Bayer, H. Waldman and M. Weibelzahl, "Field Oriented Closed Loop Control of an Synchronous Machine with the New Transvektor Control System", Siemens Review XXXIX (1972), pp 220-223
11. A. Gole, V. K. Sood, "Performance Analysis of a DQO type Phase Locked Loop gate Control system for HVDC Converters", 4-7 June 1990, Sixth National Power Systems Conference, Bombay, India.
12. M. Szechtman et al, "First benchmark model for HVDC control studies", Electra, April 1991, No.135.
13. J. Jacques, F. P. Dawson and R. Bonert, "A tracking bandpass filter for the rejection of power system disturbances", 1993 EPE'93 5th European Conf. on

Power Electronics and Applications, IEE Conf. Publication No. 377, Vol. 4, 13-16 Sept. 1993, Brighton.
14. A. Ekstorm and G. Liss, "A refined HVDC control system", IEEE Trans. on PAS-89, No. 5/6, May/June 1970, pp 723-732.
15. E. Rumpf and S. Ranade, "Comparison of suitable control schemes for HVDC stations connected to weak ac systems, Part I: new control systems", IEEE Trans. Power App. Syst., Vol. PAS-91, pp. 555-564, 1972.

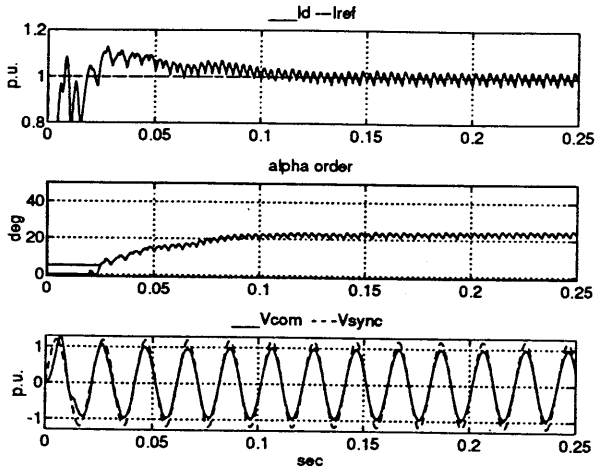

Figure 13a: Initialization with conventional gate firing unit

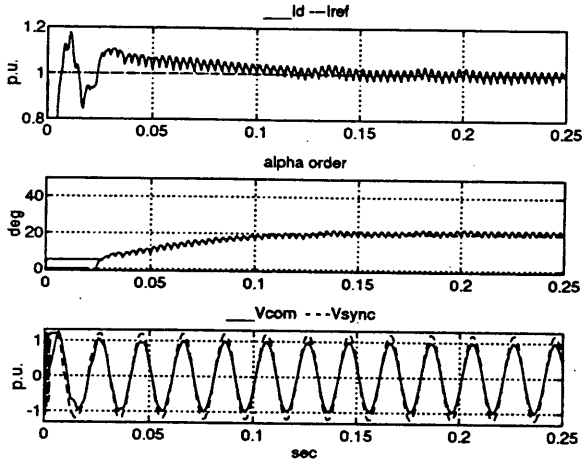

Figure 13b: Initialization with DQ-type gate firing unit

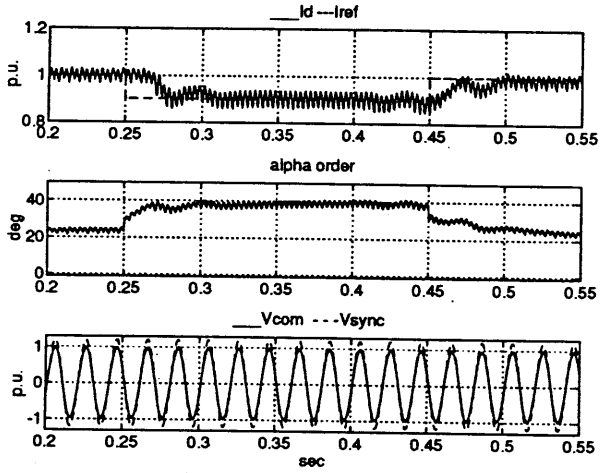

Figure 14a: 10% current step change with conventional gate firing unit

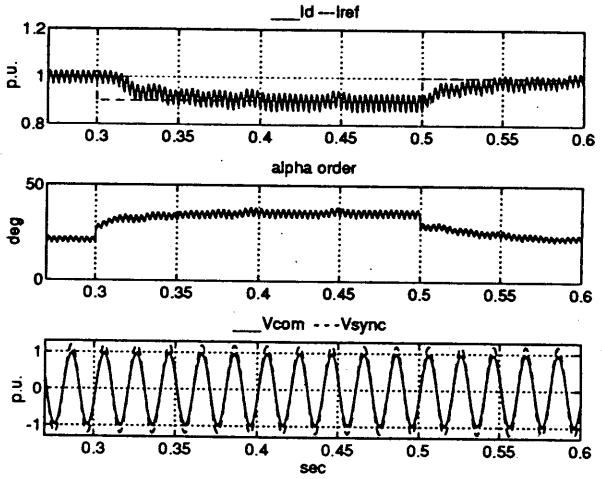

Figure 14b: 10% current step change with DQ-type gate firing

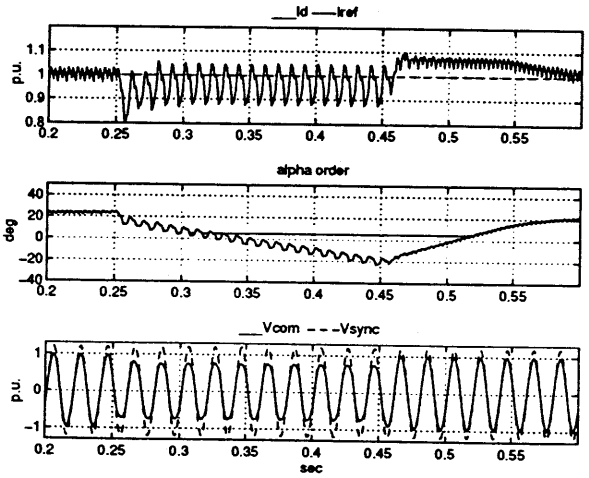

Figure 15a: Single phase fault with conventional gate firing unit

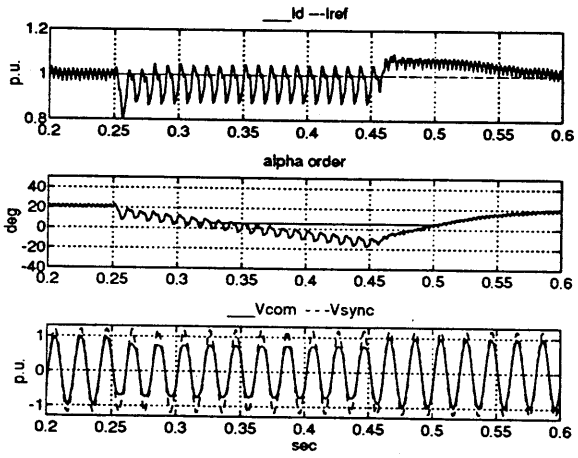

Figure 15b: Single phase fault with DQ-type gate firing unit.