Correct and fast Network Simulation using the new Calculation Method SDLV3 with advancing implied Euler Step

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Abstract

For present day real–time simulation it is important to use as large as possible step sizes. To integrate comprehensive differential equation systems, large programs for network simulation use the difference admittance method DLV. If the further developed synchronized difference admittance method SDLV3 is used instead, linear networks can be simulated by using space phasors with a step size as large as desired. Even when rotating machines are present in the network it is possible to substantially increase the step size without decreasing the accuracy of the model. The problem of determining the initial values for the difference admittance method can be solved by using an introductory implied euler step with a very small step size. Furthermore, by including the characteristic equations of equipment which cannot be described linearly, time consuming iterations can be avoided.

1 Introduction

By the simulation of transients in electrical power networks, the networks are either described with the state space theory or with the difference admittance method. The reproduction in state space has the disadvantage that a new system of linearly independent differential equations must be found whenever the network topology is altered. For difference admittance methods, on the other hand, it is only necessary to modify the matrixes. Because this is technically easier to execute, large program systems usually work with the difference admittance method.

2 Modal components for network computation

If instead of the usual abc–components the power–invariant hsz or space phasor components are used [3][7], the amount of work necessary for network computation is substantially decreased. The h–component represents here the zero–sequence system. Because the z–component is conjugated complexly to the s– component for abc–instantaneous values, the z–component is not necessary for further calculation. To reproduce the network, 2 instead of 3 component systems are sufficient. The s–component is called space phasor. Should the respective network frequency be used as transformation frequency by the transformation, the rotating part disappears and the space phasors become constant complex values in the steady state operation. After the decreasing of the transients, they can be integrated with a step size as large as desired. The angle between the rotor of the machine and the space phasor transformed with network frequency is the electrical rotor angle. If the voltage and current space phasors are then revolved back around the electrical rotor angle and divided into real and imaginary parts, the well–known rotor–fixed orthogonal dq or quadrature components can be obtained.

3 The difference admittance method

Large programs for simulation of power networks normally use the difference admittance method DLV, as was suggested for the first time by *Dommel* [1] in the 1960s. To integrate the differential equations of a network branch, the trapezoid rule is applied. This results in a slope error by the approximation of the integral. The slope error can be avoided by factorizing the eigenvalue in advance. If the eigenvalue factorized form of the differential equation is solved with the trapezoid rule, the synchronized difference admittance method SDLV1 according to *Inan* [2] is obtained. If, on the other hand, the product rule of the integral calculation is previously applied, the most highly developed solution of the original differential equation is obtained. This solution is still analytically exact. If one assumes that the slope of the value which is to be integrated in the interval remains constant, then the synchronized difference admittance method SDLV3 is obtained as the mathematically most highly developed difference admittance method [3].

Because the voltage and current space phasors by the transformation with the network frequency in steady state operation are constant complex values, they become, at the end of an indefinitely long integration step, the complex phasors of electrical engineering, which are only connected with each other as follows:

$$\underline{I} = \text{Admittance} \cdot \underline{U}$$

From these considerations three requirements for the step coefficients and the difference admittance can be derived, whereby the SDLV3 is the only difference admittance method which can fulfil all of them [3]. By DLV, on the other hand, numerical oscillations occur, which can be proved beyond a doubt with the help of the $\mathcal{Z}$–transformation [5]. Figure 1 shows as an exam-

ple of this the current by connecting a constant voltage source U to a one–phase RL–serial element for various values of the relative step size $\tau = \frac{R}{L} \cdot \frac{\Delta t}{2}$. The oscillations occur when $\tau > 1$. For not too large values of τ, they die away relatively quickly, as shown in figure 1a. For large values of τ, however, one obtains, as shown in figure 1b, an undamped oscillation around the steady state final value of the current. The results by SDLV3 are, in contrast to this, always exact.

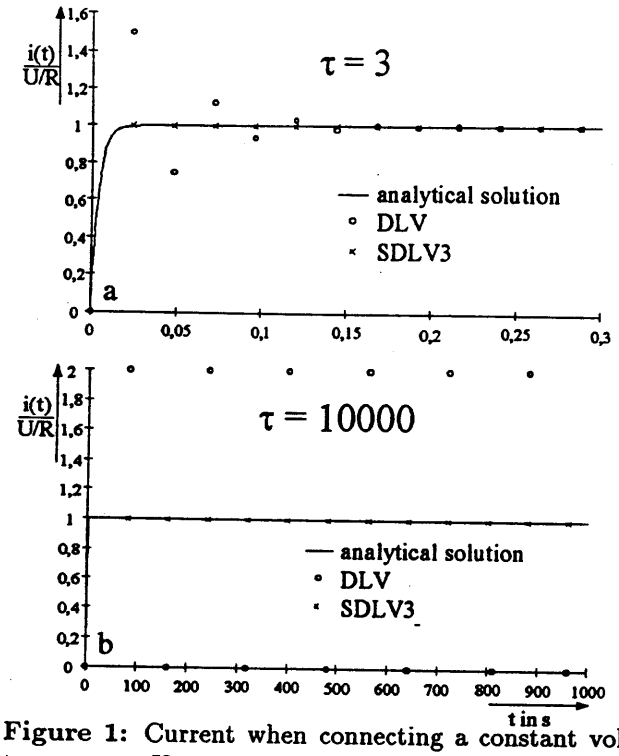

Figure 1: Current when connecting a constant voltage source U to a one–phase RL–serial element for various relative step sizes τ

A further characteristic of all difference admittance methods is an increasing drop of the simulated frequency when the step sizes are increasing. This can also be shown with the help of the $\mathcal{Z}$–transformation using the example of the connection of a constant current source I to a one–phase LC–parallel resonant circuit [5]. This behavior is, as a characteristic of the bilinear transformation, well–known in digital signal processing. The bilinear transformation originates from the approximation solution of a differential equation with the trapezoid rule and the subsequent application of the $\mathcal{Z}$–transformation. It is used to design the transfer functions of digital filters from the known transfer functions of analogous filters.

4 Consideration of initial conditions

The difference admittance method, which originated with the help of the trapezoid rule, requires all branch voltages and branch currents of the network at the beginning of every integration step. Because after a switching operation or after a network fault due to the condition for continuity only the voltages of the capacitive and the currents in the inductive branches are known, this method is not useful for the first step after a discontinuity.

If the implied euler rule is used, however, only the known condensator voltages and inductivity currents are necessary. But because the accuracy of the implied euler rule is dependent on the slope, it only allows relatively small step sizes.

If one combines both methods into a difference admittance method with an introductory implied euler step, however, the advantages of both methods can be utilized. First, as shown in figure 2, an implied euler step with a very small step size is carried out. The step size must be small in comparison to the largest natural frequency of the network. Subsequently, the calculation is continued with the difference admittance method with a substantially larger step size. This necessitates, however, calculating double the difference admittance values and the step coefficients. This has the advantage that the step coefficients of the DLV for the step size Δt coincide with the calculation factors of the implied euler method for the step size $\frac{\Delta t}{2}$. Because the step size of the implied euler step must be very small and the DLV tends toward numerical oscillations when the step size is large, it does not make sense to cling to this advantage.

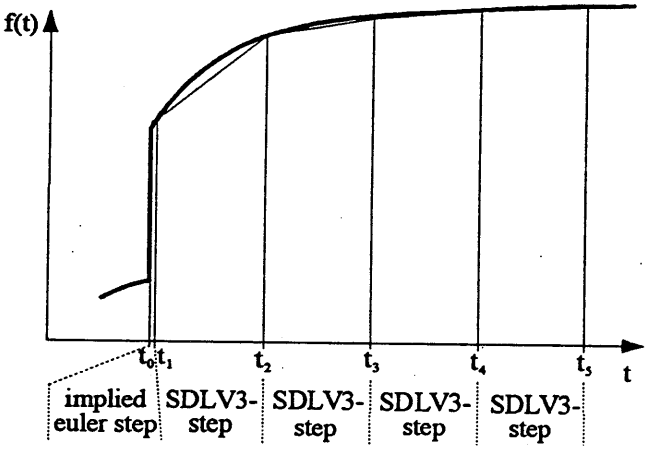

Figure 2: Difference admittance method with introductory implied euler step

5 Simulation of interconnected networks

To simulate an interconnected network with space phasor components the network can be divided into three parts as shown in figure 3. The main part is the linear network shown in the middle of figure 3. It consists of equipment which can be described by linear equivalent circuits. The z–component is not required for this because it is conjugated complexly to the s–component. The fault location is the coupling between s and h–component network. The three error equations can be obtained by transforming the fault equations from the abc–components into space phasor components and subsequently inserting the relation $g_z = g_s^*$. The third part consists of the equipment which in space phasor components cannot be described by linear equivalent circuits, as for example a generator. Using the well–known equivalent circuits in hdq–components ac-

cording to [8] as a starting point, two characteristic equations of the dq–components and one characteristic equation of the h–component will now be created for the generator, as is described in [4]. If the mechanical equation is solved approximately, the electrical rotor angle ϱ can be calculated and along with it the space phasor generation and the re–rotation of the rotor–fixed dq–system on the stator–fixed space phasor can be executed. Two characteristic equations for the stator–fixed space phasor of the generator and one characteristic equation for its zero–sequence system can be obtained from this. If these three characteristic equations are inserted into the characteristic equations of the linear network, a clearly solvable system of 6 equations (2 equations of the space phasor system and 1 equation of the zero–sequence system of the linear network and the generator, 3 fault equations) with 6 variables ($\mathrm{Re}\{\underrightarrow{i}_F\}$, $\mathrm{Im}\{\underrightarrow{i}_F\}$, $\mathrm{Re}\{\underrightarrow{u}_F\}$, $\mathrm{Im}\{\underrightarrow{u}_F\}$, i_{Fh}, u_{Fh}) is found.
This method has the advantage that it is only necessary to approximate the electrical rotor angle ϱ to carry out the integration step. An iteration is therefore almost fully unecessary and so the calculation time is shortened. When using previously common procedures the connection point voltages or currents had additionally to be approximated at the beginning and iterated at the end of the integration step. Using the general description according to [7], it is also possible to connect as many non–linearly describable equipment as desired at every node of the network.

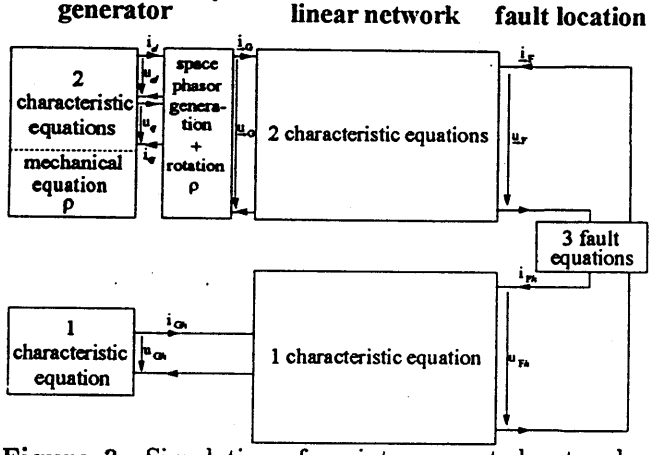

Figure 3: Simulation of an interconnected network with space phasor components

6 Simulation examples

6.1 3–phase short circuit in a interconnected network with ideal voltage sources

Figure 4a displays a three–phase network, made up of two ideal voltage sources, which each supply, over a transformer, an overhead line, and a reactor, a common load. The corresponding equivalent circuit of the space phasor system is displayed in figure 4b. Should now a 3–phase short circuit without impedance occur at the load, then the fault current $\underrightarrow{i}_F$ in the equivalent circuit according to figure 4b will flow into the short circuit node.

Figure 5 shows the absolute value $|\underrightarrow{i}_F|$ of the space phasor of the short–circuit current by simulation with the difference admittance method with an introductory implied euler step. The maximum simulation time was 0,4s. The analytical solution is marked solidly.

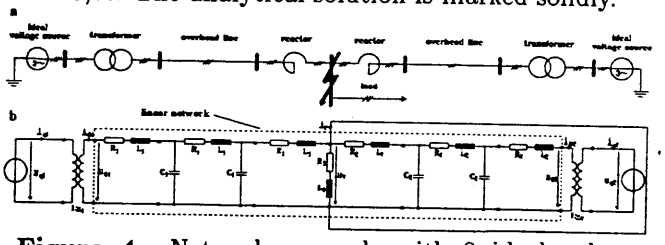

Figure 4: Network example with 2 ideal voltage sources and 3–phase short circuit at a load; **a** 3–phase representation; **b** equivalent circuit of the space–phasor system.

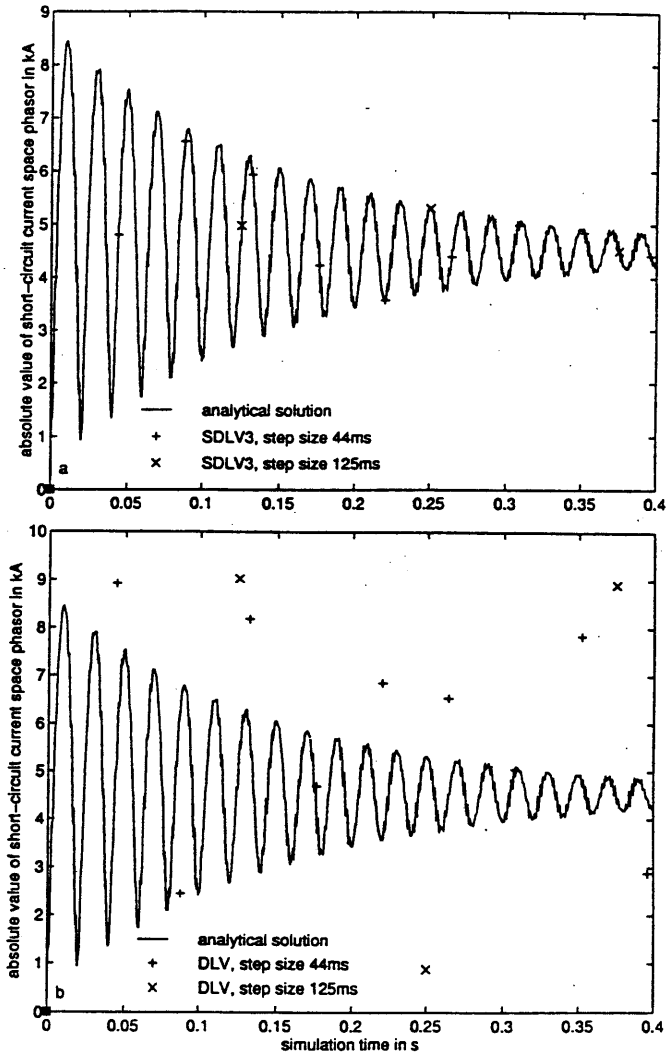

Figure 5: 3–phase short circuit in a interconnected network with ideal voltage sources; **a** SDLV3 with introductory implied euler step; **b** DLV with introductory implied euler step.

As shown in figure 5a, the results of SDLV3 with an introductory implied euler step are always exactly the same as the analytical solution. By DLV with an introductory implied euler step, on the other hand, clear deviations can be recognized in figure 5b.

When the maximum step size is increased to 2s, as can be seen in figure 6a, it is even possible with the SDLV3 to integrate over the transients with a very large step size of $\Delta t = 1,8$s and immediately obtain the steady state final–value. With DLV, on the other hand, an unwanted interference occurs. The introductory implied euler step is thereby carried out each with a step size of 1ns.

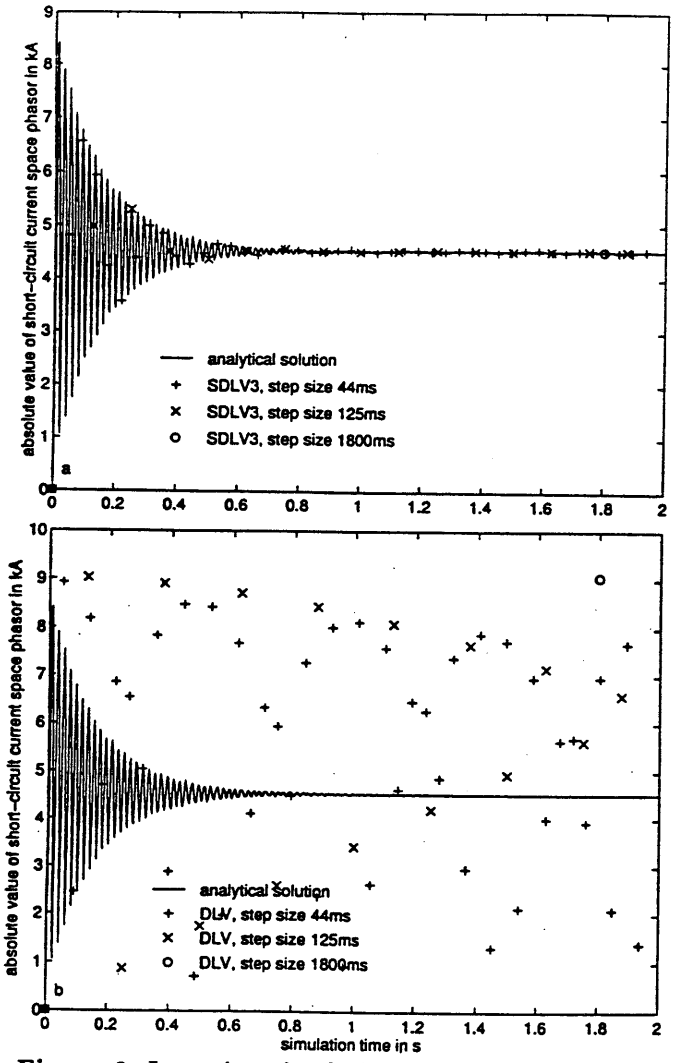

Figure 6: Long time simulation with large time steps. **a** SDLV3 with introductory implied euler step; **b** DLV with introductory implied euler step

6.2 3–phase short circuit in a interconnected network with rotating machines

Figure 7 shows a interconnected network which is made up of 3 generators, 3 transformers, 6 overhead lines, 3 loads and one supply network with a short circuit power of 15 GVA. As in figure 4 the overhead lines are simulated by a π–element, the loads by an RL–serial element and the transformers by an RL–serial element in line with an ideal transformer. The presentation of the generators follows as described in [4].

A 3–phase short circuit without impedance is simulated at node 9. The SDLV3 with introductory implied euler step serves as the simulation method. Figure 8 shows again the absolute value of the short circuit space phasor $\underrightarrow{i}_F$ for various step sizes. A reference result simulated with the sufficiently small step size of 10μs is marked solidly each.

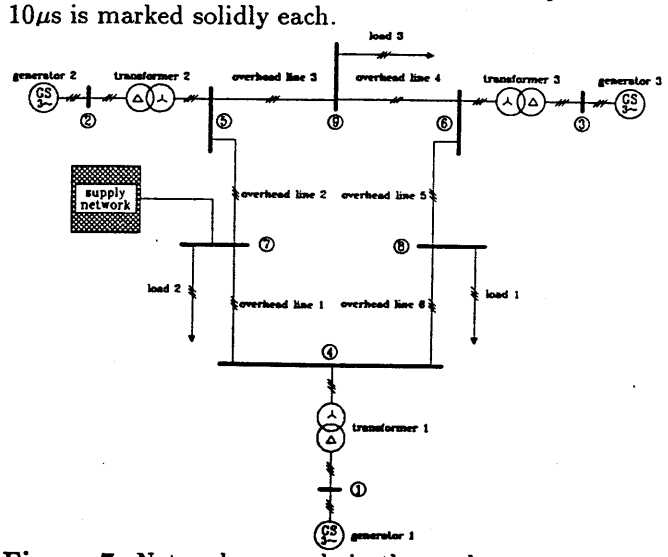

Figure 7: Network example in three–phase representation

In Figure 8a a small 11th harmonic oscillation can be identified in the reference result. Due to the transformation with the network frequency of 50 Hz, the D.C.–part of the space phasor becomes a 50Hz–oscillation. The simulation results for $\Delta t = 1$ms still match much more accurately those of the reference result. When $\Delta t = 4$ms, the frequency drop of all difference admittance methods can be observed. If the simulation time is increased, the quasi–steady–state solution is obtained for the reference result. At $t = 0,8$s a decrease in the amplitude can be noticed. The simulation results for $\Delta t = 4$ms merge in spite of the frequency drop exactly into the quasi–steady–state solution. The frequency drop has therefore absolutely no effect on the further calculation after dying out of the transients. Even at $\Delta t = 111$ms the results match the reference result relatively precise, even though the sampling theorem for the 50Hz–oscillation of the D.C.–part is clearly violated. Figure 8c shows that the drop of the amplitude after 0,8s becomes an oscillation with an increasing frequency, which is caused by loss of synchronism of generator 1. The results for $\Delta t = 111$ms and $\Delta t = 700$ms are nevertheless in the amplitude area of the oscillation. As can be seen in the results, it is possible with the SDLV3 to integrate over the fast and medium transients. We can speak here in terms of a sequence reduction, which means the result, when using large step sizes, corresponds to that of a sequence reduced system. There now exists the possibility of changing over the step size. One begins, for example, with $\Delta t = 0,1$ms for the fast transients of about some kHz. Following their dying out, one switches over to $\Delta t = 2$ms, for example, for the simulation of the D.C.–part of 50Hz. Following its dying out, one applies $\Delta t = 100$ms, for example, to the simulation of the power swings of about 1 Hz.

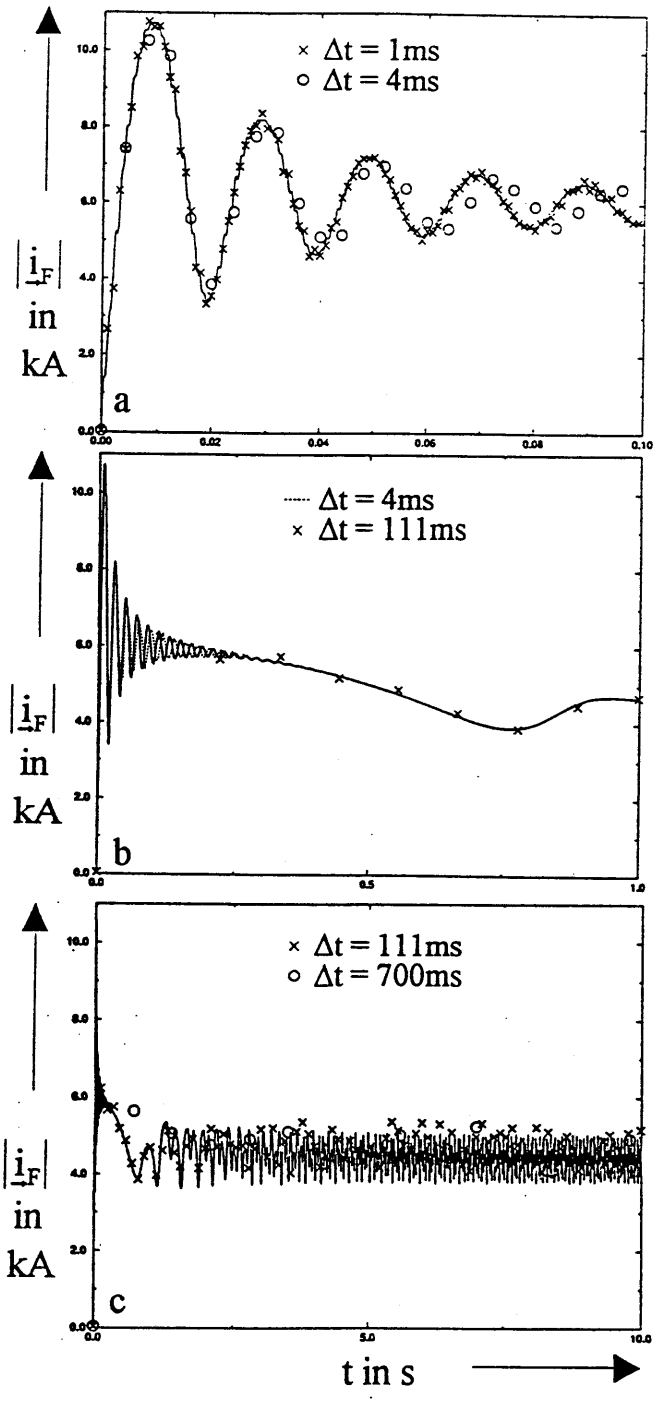

Figure 8: Short circuit current space phasor after a 3–phase short circuit without impedance; a $t_{max} = 0,1s$; b $t_{max} = 1s$; c $t_{max} = 10s$

6.3 Disconnection of a load in a interconnected network

A further example shows the disconnection process of load 3 in the interconnected network according to figure 7. The disconnection is carried out as a consequence of 1–phase, 2–phase, and 3–phase interruption, each in a current zero crossing with a current chopping limit of 10A. In figure 9 the current of generator 1 for various maximum simulation times for $\Delta t = 10\mu s$ is plotted. For purposes of comparison, the absolute value of the current space phasor (figure 9a–c) and the currents of the abc–components (figure 9d–f) are displayed next to each other.

As shown in figure 9a, all the fast transients have already completely died out after about 100ms, whereas the D.C.–part with the 50Hz–oscillation does not die out until about 250ms (figure 9a). Figure 9c shows that the power swings disappear after about 4s. When one compares figures 9a–c with figures 9d–f, the superiority of the representation in space phasor components over the abc–components is easily recognizable. The D.C.–part can no longer be recognized in figure 9e, for example, whereas in figure 9b it can be clearly seen as 50Hz–oscillation.

7 Conclusion

For simulation of transients in power networks the difference admittance method is most commonly used. If the eigenvalues of the branches are taken into consideration, the widely used difference admittance method DLV can be further developed into the synchronized difference admittance methods SDLV1, SDLV2, and SDLV3. In contrast to SDLV3, numerical oscillations occur when using DLV with medium to large step sizes. In addition, all difference admittance methods display an increasing drop in the natural frequency with increasing step size.

The simulation is normally carried out with abc–components. If, however, space phasor components are used, the work load is substantially reduced. The SDLV3 is the only difference admittance method which enables the simulation of linear, non–zero–sequence networks in space phasor components with a step size as large as desired, which is independent of the network frequency.

The disadvantage of the difference admittance method is that after a switching operation or a network fault all branch voltages and branch currents must be known as initial values for the next step. If, on the other hand, the implied euler step with a very small step size is carried out first, only the already steady capacitor voltages and inductivity currents are necessary as initial values.

The application of the considerations discussed here is demonstrated on simulation examples. This shows that it is also possible to simulate a larger interconnected network with anisotrope equipment with large step sizes. The SDLV3 allows to integrate over the fast and medium transients under a broad violation of the sampling theorem. This offers the possibility for a step size change–over. To ensure the acquisition of any given transients, the step size should always be chosen at about a factor 10 smaller than the period of the frequency to be displayed.

The SDLV3 with a introductory implied euler step by the application of space phasor components introduces a method which is excellently suitable for fast simulation of power networks with simultaneously high accuracy.

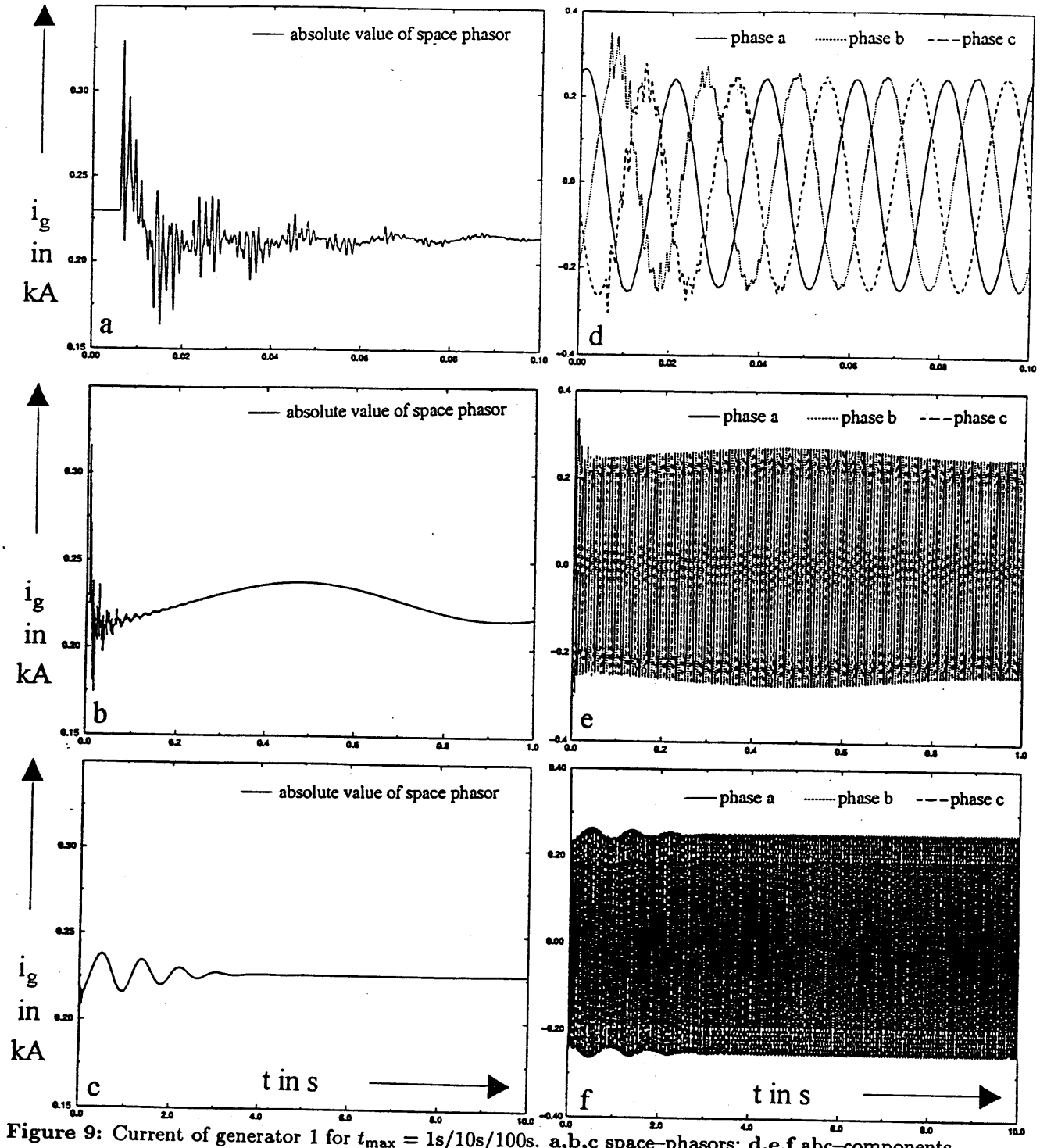

Figure 9: Current of generator 1 for t_{max} = 1s/10s/100s. **a,b,c** space–phasors; **d,e,f** abc–components.

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