Modeling of Power Electronic Apparatus: Additional Interpolation Issues

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Abstract: **Fixed time-step programs based on the trapezoidal algorithm present a challenge to the modelling of power-electronic devices. This is due to the fact that all switchings are constrained to occur at multiples of the basic simulation time-step. Interpolation of the switching instant is one answer to this challenge. The paper presents the impact of using interpolation on the simulation of HVDC and FACTS devices, in particular on the removal of firing angle jitter as well as on the elimination of spurious non-characteristic harmonics. It is also shown that a considerable accuracy improvement can be obtained with interpolation applied to the control system components only.**

Keywords: Electromagnetic Transient Simulation Programs, Interpolation, HVDC, FACTS, STATCOM, Harmonics

I. INTRODUCTION

Power electronic apparatii such as high voltage Dc converters (HVDC) and flexible ac transmission (FACTS) devices, present a special problem for simulation with electromagnetic transients programs (referred to as emtp-type). A typical power electronic switch such as a thyristor or gate turn-off (GTO) thyristor may open and close several times in a cycle. Fixed time-step emtp-type [1] programs usually allow such switchings to occur on integral multiples of the time-step. However, this can cause various problems such as spurious inductive current chopping and additional jitter in the values of various measured quantities. On the other hand, the fixed time-step approach usually results in faster simulation compared to programs (such as used for the simulation of electronic circuits) that use a variable time-step.

The interpolation method, originally proposed by Kulicke [2] is one approach that allows for a more accurate switching instant to be modeled (i.e., does not confine the switching instant to an integral of the time-step); without resulting in an excessive penalty on simulation time. The method uses the system quantities at the exact firing instant (in between time-steps) which are estimated from a linear interpolation of the values at the integral time-step intervals. The time penalty for using interpolation is minimal.

Earlier papers have shown that the introduction of interpolation results in improved accuracy in the simulation of a large HVDC Network[3]. In this paper some additional issues are discussed. These include the effect of using partial interpolation in which the interpolation is only applied to the control system elements. The impact of interpolation on the generation of false non-characteristic harmonics and the use of interpolation in solving the phenomenon of voltage chatter at inductive nodes[4] is presented. The paper also compares the performance of previously used methods for improving the results from fixed time-step programs such as artificial snubber circuits with the interpolation method. Also presented are situations such as certain HVDC modulation studies, in which using interpolation becomes a necessity.

The effects of interpolation are demonstrated using the CIGRE HVDC benchmark system[5] and a simple STATCOM (Static Synchronous Compensator) as simulation examples. The interpolation algorithms discussed here are those used in the emtp-type program PSCAD/EMTDC.

II. INTERPOLATION ALGORITHM

A. Interpolation in the Circuit Solution Algorithm

Emtp-type programs typically use a fixed time-step for the numerical solution of the power system's differential equations. The trapezoidal rule is used to convert the differential equations into algebraic equations that allow for the calculation of the network voltages at the end of a time-step from a knowledge of the sources and the initial values at the beginning of the time-step[1]. For most HVDC/FACTS type studies a value of Δt in the range 25 μs-50 μs is considered acceptable. Note that the time-step of 50 μs can only be used if the natural transients in the network have time-constants or periods less than this value. However as the bandwidth required for most HVDC/FACTS studies is in the 0-5 kHz range, this is not a serious concern.

With semiconductor switches such as thyristors, GTO devices and so on, the switch can only be turned on or off at an integral multiple of this basic time-step. A 50 μs time-step corresponds to typically 1° of a fundamental frequency waveform. This results in a number of drawbacks:

1. In the case of a thyristor or diode turning off, the current zero may occur in between two points of the discrete time grid. If the series element is inductive, spurious voltage spikes may arise. This is one reason why artificially large snubber circuits across the device may have

to be modelled [6].

2. The 1° (approximately) jitter in firing angle leads to the generation of spurious non-characteristic harmonics. This is particularly serious if there is a network resonance in the neighborhood of these harmonic frequencies.
3. The error may be compounded if several cascaded control or measurement blocks (i.e., extinction angle measurement) each have the 1° or so of uncertainty. Kuffel et al[3] report a total jitter of up to 5° while using a 50 μs time-step.
4. Certain simulation studies, such as modulation of dc for Sub-synchronous Resonance (SSR) damping require a modulation signal to the firing angle with an amplitude of fractions of a degree. The 50 μs time-step is too coarse.

HVDC and Static Var Compensation schemes have a firing angle jitter specified to be about 0.1°. It is desirable that the simulation program at least reproduce this accuracy. The 0.1° requirement translates into a time-step in the order of 5μs or smaller. However, a time-step this small would lead to a prohibitively large computation time.

One way around this is to use a variable time-step [7] so that if a switching instant is detected, the program changes to a small time-step and reverts to the original time-step. However this requires a re-triangularization of the matrix and in general results in longer CPU times as compared to the interpolation method used in the current program.

An alternative is to use linear interpolation [2,3]. This method can best be described with the example of a simple diode. The waveform in Fig. 1 shows the current through a diode with a standard fixed time-step switching algorithm. The current reverses at some time in between Δt and 2Δt, but because of the discrete nature of the time-step, the impedance of the device can only be made infinite (i.e., diode turns off) at integrals of Δt, here 2Δt. The first recorded instant of zero current is thus at 3Δt.

Fig. 2 shows the same device with the switching interpolated to the correct instant. As before, the program calculates the solution at t = Δt and t = 2Δt. However, on noticing that at the latter time, the current has already crossed zero, it estimates the turn-off time to be t =1.2 Δt based on a linear interpolation of the current within the switching interval. All the voltages and currents in the trapezoidal solution method are then also interpolated to this intermediate time in a linear fashion. The admittance matrix is then re-formulated and the solution continues with the original time-step, yielding the new solution one time-step later at t = 2.2 Δt. One additional interpolation step between t = 1.2 Δt and 2.2 Δt yields the solution at t = 2 Δt. The latter apparently cosmetic step is taken to put the solution back on the original time grid.

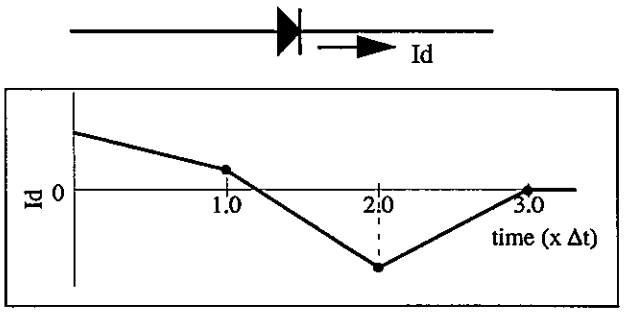

Fig. 1. Simulated diode switching off at a current zero - fixed time-step

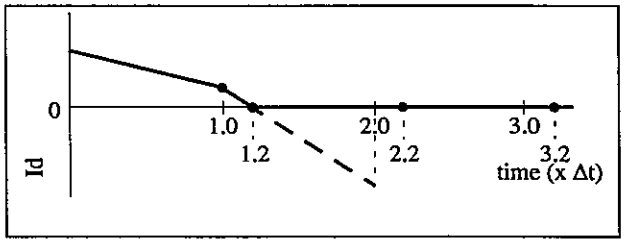

Fig. 2. Simulated diode switching off at a current zero - with interpolation

Although interpolation requires a few additional computations in the algorithm, it has been shown that this only introduces a small computation time overhead[3].

The results obtained from interpolation using a large time-step match those obtained with using a very small time-step. Thus using the above approach it is possible to get very precise switching times without recourse to a small time-step and the associated large CPU time.

B. Interpolation Used for Chatter Removal

One drawback of the classical emtp-type trapezoidal solution algorithm is that it can lead to the phenomenon of chatter. The problems appears as a time-step to time-step symmetrical oscillation or "chatter" in the voltage waveform of a node to which only switches and inductances are connected [4]. The chatter is initiated by the turn-off of the switch and occurs even when the switch turns off at a natural current zero. The dotted line in Fig. 3 shows a waveform with

chatter, resulting from a natural turnoff of a thyristor connected to an inductor. As inductive switching is very common in power electronic circuits it is important to find a solution to this problem. Other researchers [4] have proposed using a modified integration procedure at the instant of switching. However, the problem can also be solved by using interpolation. The method used in the paper makes a half-time-step interpolation to the network solution as represented by the solid line in Fig. 3. The voltage solution at this point is zero and any further chatter is avoided.

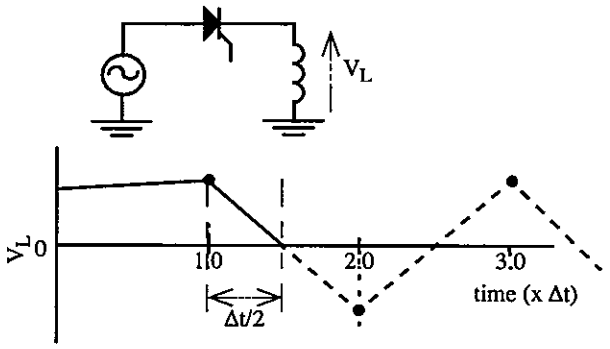

Fig. 3. Chatter and its removal

The two procedures of interpolation and chatter removal are performed within the same algorithm. With this approach it becomes possible to connect any number of switching devices in an arbitrary configuration. This is not possible in many solution algorithms that use a fixed time-step unless time-consuming iterative techniques are employed.

A circuit similar to that in Fig. 3, except with a diode instead of the thyristor and a series R-L load with R =1 Ω and L = 5 mH is simulated with the results for inductor voltage shown in Fig. 4 Note that if artificially large snubber circuits across the diode valve are not modelled, the voltage manifests chatter. Even with the snubber circuit, some voltage spikes are seen with a simulation time-step of 50 μs. Only when the time-step is reduced much further, say to 5 μs, does the chatter nearly disappear. On the other hand, if the chatter-removal algorithm is enabled, no chatter is observed even when the diode has no snubber circuit.

C. Partial Interpolation-Controls Only

Introducing interpolation in the entire network solution involves changes to the basic algorithm of the program. However some emtp-type programs do have an interface to a higher level language (i.e., FORTRAN) using which users can write their own control algorithms. As the control system model is user-developed it is possible to introduce interpolation in this part of the model only. Partial interpolation may be described with reference to a block developed for the measurement of the firing angle of a thyristor valve. The firing angle (α) is defined as the time (converted to units of angle by multiplying with the system's angular frequency) from the zero crossing of the forward biasing voltage to the time at which the firing pulse is issued. The firing pulse is generated for example, by the intersection of a timing ramp with the firing angle order signal.

The value of α calculated without interpolation uses the difference in time-step values calculated from the nearest points on the time grid. With linear interpolation between the time-grid points, a much more accurate measurement of α is possible as seen from Fig. 5. With partial interpolation, it should be noted that the turn-on of the valve still occurs at an integral multiple of the time-step, however the signals within the measurement and control algorithms may be treated with more accuracy. As will be shown in the section on results, control-only interpolation works best when the time-step is chosen so that the fundamental period of the system frequency is an exact multiple of the time-step.

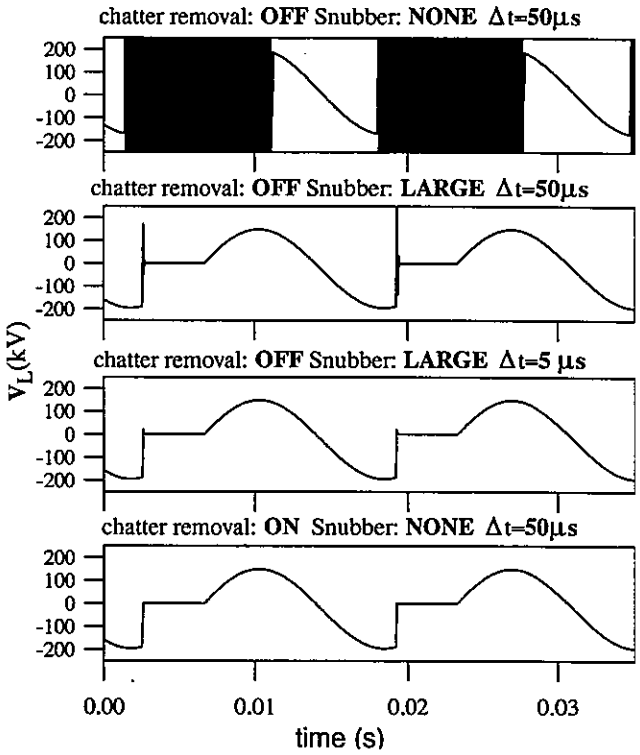

Fig. 4. Performance of chatter removal algorithm

III. SIMULATION EXAMPLES

A. Impact on steady-state quantities

The impact of using interpolation in an emtp-type algorithm is demonstrated using the CIGRE HVDC Benchmark system shown in Fig. 6. The data for this system are

readily available and published in literature [5]. The steady state extinction angle is shown in Fig. 7. A 50 μs time-step, which happens to be an exact sub-multiple of the fundamental period of the 50 Hz system. Without interpolation (a), there is a steady state fluctuation of about 3°.

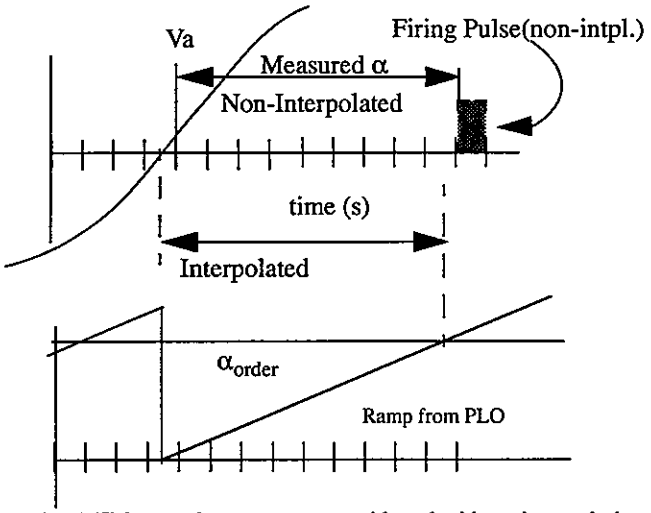

Fig. 5. Firing angle measurement with and without interpolation

With full interpolation (d) the jitter is less than 0.01°. With controls interpolation only (b), the observed jitter of approximately 0.5° is a considerable improvement over the case with no interpolation. With only the network (circuit) solution interpolated (c), the accuracy is slightly worse than that with control interpolation. Note that this option (c) is also a partial implementation of interpolation. The thyristor turn-off instant is interpolated as it is a circuit solution event, i.e., no pulse is given from the controls.

However, if the fundamental period is not an exact multiple of the time-step, then the interpolation of controls gives only minimal improvement as seen from Fig. 8 which is generated with $\Delta t = 43$ μs.

Again, the jitter is about 2.5° for the non-interpolated case (a). With controls interpolation (b), the jitter is only marginally better than in the case with no interpolation.

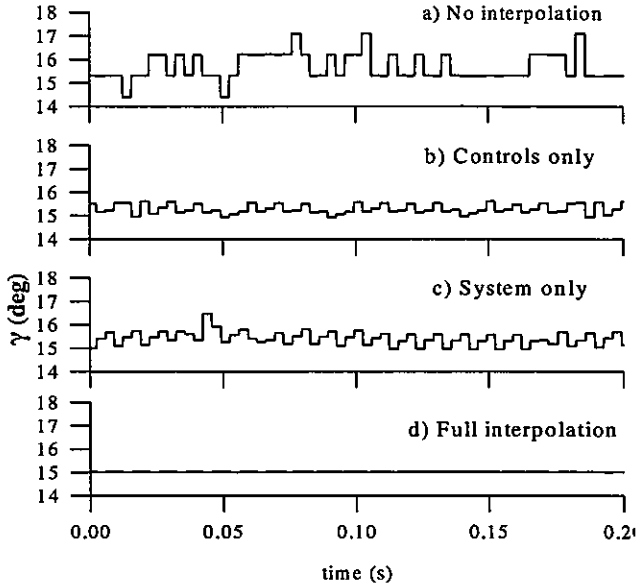

Fig. 7. Impact of interpolation on extinction angle (Δt=50μs)

This is because the difference between the turn-off time and the exact point on the time-grid varies continuously, which is not the case when the period is a multiple of the time-step. Making the fundamental period to time-step ratio an exact multiple is a trick that has been long known to users of emtp type programs. With full interpolation (d) the performance is almost identical to that with the 50 μs time-step with a slightly higher jitter of about 0.04°.

The above tests prove that with full interpolation, extremely accurate solutions are obtained. Furthermore, they are not affected by the choice of time-step. Controls-only interpolation on the other hand gives improved results, but

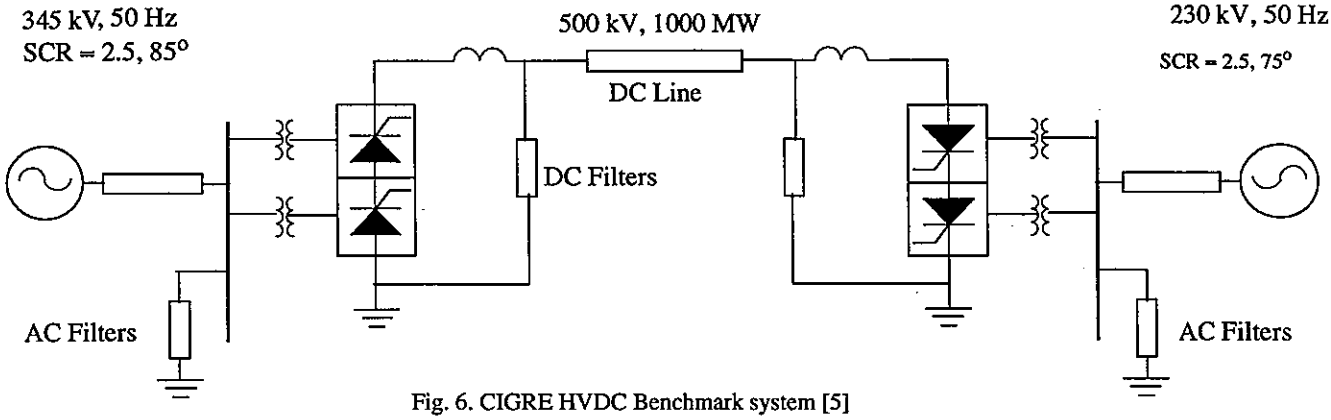

Fig. 6. CIGRE HVDC Benchmark system [5]

can be considered effective only if the fundamental period bears an integer ratio to the time-step.

B. Generation of spurious harmonics

Fig. 9 shows the study system in which a Static Synchronous compensator (STATCOM) is used to regulate the midpoint voltage of a 230 kV transmission line. A STATCOM has gate turn-off (GTO) thyristor elements so that both the turn-on and turn-off of the device is dictated by the control system.

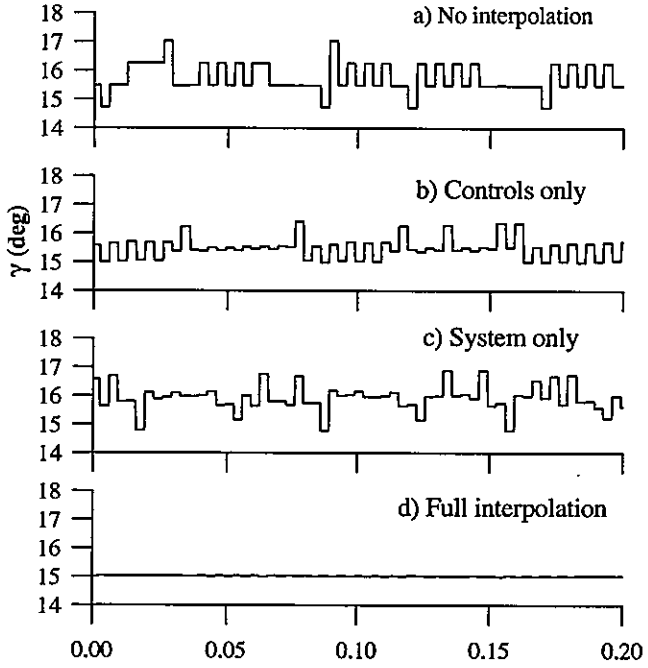

Fig. 8. Impact of interpolation on extinction angle (Δt=43μs)

The harmonics observed on the mid-point voltage waveform are shown in Fig. 10. The generation of spurious non-characteristic harmonics is clearly visible when interpolation is not used. If additional system resonances are present at these non-characteristic frequencies, erroneous highly distorted voltages and currents may result unless interpolation is used or unless the time-step is reduced to very small values. Also note that the forced turn-off of the GTO requires that a diode must turn on in the same time-step. Otherwise there is no alternate path for the GTO current to transfer to, resulting in large spurious voltage spikes. Unless interpolation is used this circuit cannot even be simulated without the use of uncharacteristically large snubbers with $\Delta t = 50$ μs.

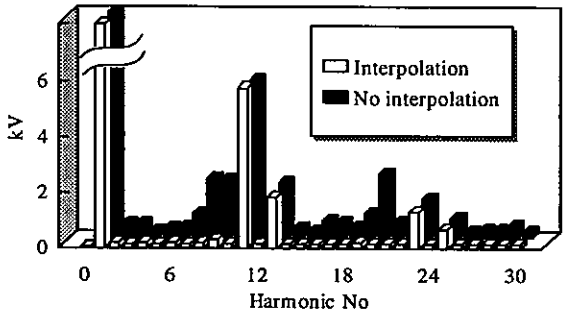

Fig. 10. STATCOM ac voltage harmonics

C. Cases where interpolation is a must.

For many HVDC modulation studies such as the damping of subsynchronous resonance (SSR) oscillations in generators connected to a dc converter, the converter's firing angle has to be modulated over fractions of a degree[8], necessitating the use of interpolation or a very small time-step. The electro-mechanical resonance being studied lasts over tens of seconds thereby making the use of small time-steps impractical.

For example, Fig. 11, which has been generated using full interpolation, shows the angle modulation for SSR damping in the case of a 300 MW generator feeding a 300 MW dc rectifier. The modulation swings start out at around

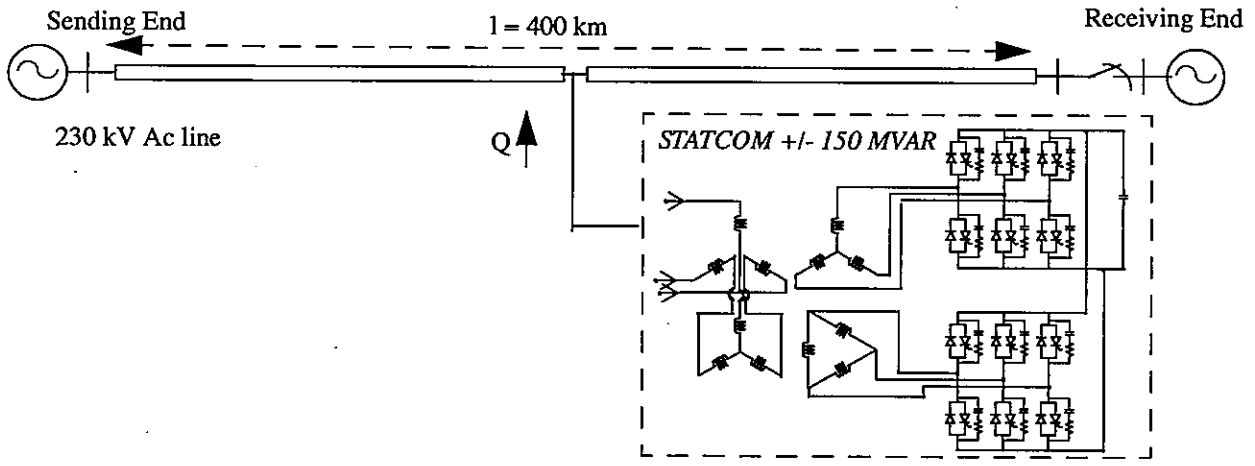

Fig. 9. STATCOM for midpoint voltage control

+/- 4°, and drop to even smaller values as the simulation progresses.

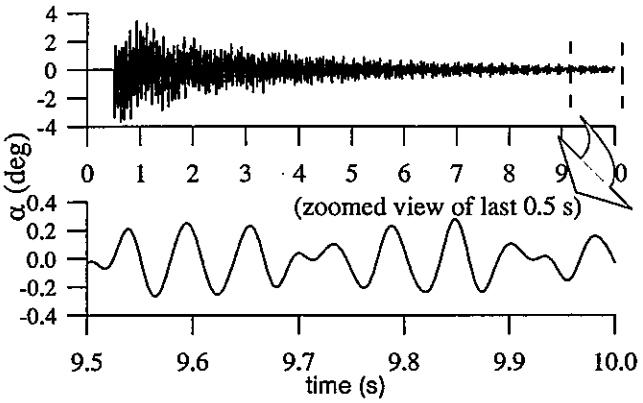

Fig. 11. Firing angle for SSR damping

In fact for a similar SSR case, Fig. 12(b) shows unstable oscillations in the shaft torque which are excited spontaneously due to the spurious jitter produced in the HVDC system for Δt=50 μs and interpolation disabled. These oscillations are at the under-damped SSR modal frequencies (predominantly 15.7 Hz) . Note that the system is stable as in Fig. 12(a), with the use of interpolation or with the use of an extremely fine time-step as in Fig. 12(c).

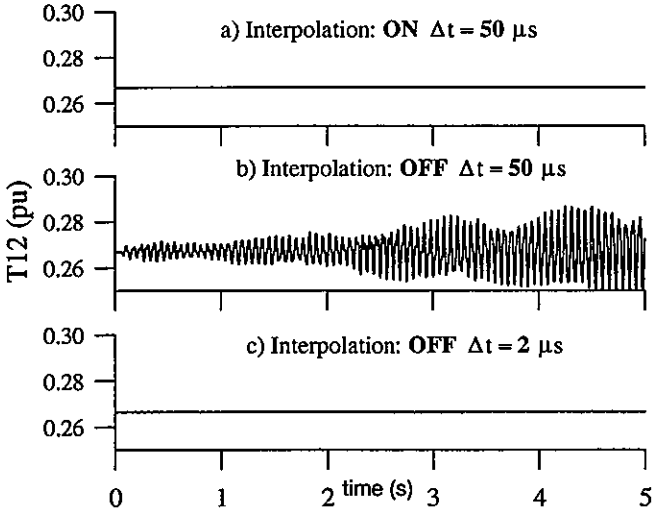

Fig. 12. Spurious SSR oscillations due to large time-steps

Similarly interpolation must be used when simulating other types of resonances, such as core saturation instability in HVDC converters, that can be excited with spurious firing angle jitter.

IV. CONCLUSIONS

Numerical interpolation allows for the precise simulation of switching phenomenon. It thus allows greatly improved accuracy when simulating power electronic circuits which are in a constant state of being switched. Furthermore, the accuracy remains high even when the fundamental period is not an exact multiple of the time-step. In certain studies involving ac system resonant conditions or requiring small modulations of firing angle, interpolation is a must.

If the emtp-type program being used does not have interpolation but does have a higher level language interface, partial interpolation of the control system only can provide satisfactory results. However, in this case it is necessary to choose a time-step which is an exact sub-multiple of the fundamental period.

Jitter caused by the fixed time-step affects the magnitude of non-characteristic harmonics; the characteristic ones being less affected.

V. REFERENCES

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