Investigation of the TCSC as a Fault Current Limiter

A.R.M. Tenório

Companhia Hidro Elétrica do São Francisco - CHESF
Rua Delmiro Gouveia, 333
Recife - PE - 50761-901
Brazil

N. Jenkins

UMIST
Manchester Centre for Electrical Energy
Ferranti Building, PO Box 88
Manchester, M60 1QD
UK

Abstract – **This paper investigates the capability of the TCSC (Thyristor Controlled Series Capacitor) when acting as a fault current limiter. The basic aspects of the TCSC current limiter are considered such as: resonance frequency of the LC circuit, energy requirements of the surge arrester and strategies for detecting the fault condition. One of these strategies is based on the rate of rise of the line current, whereas the other is based on current amplitude. The former is a very fast detection strategy capable of effective limitation of even the first peaks of fault current. A TCSC model developed for the EMTP-ATP program [1] is used in order to simulate this TCSC current limiting action in a simple power system.**

Keywords: Fault Current Limiter, TCSC, EMTP Modelling, FACTS devices.

I. INTRODUCTION

The management of power systems in countries in all parts of the world is now changing and there is a strong tendency towards separating generation from the primary transmission grid. In this deregulated environment the power utility responsible for operating the primary grid loses control over the siting and scheduling of generation. Therefore, large concentrations of generation can be developed in areas where previously little generating plant existed. This makes the limitation of the fault current level an important issue, which is now investigated by electric utilities, researchers and manufacturers.

The most common solutions to high fault current levels are: uprating of switchgear and other equipment; splitting the grid and introducing higher voltage connections (AC or DC); introducing higher impedance transformers and series reactors; and using complex strategies like sequential network tripping [2]. Nevertheless these alternatives may create other problems such as loss of power system security and reliability, high costs, and increase of power losses.

In the last few years, interest in devices that are able to limit the fault current levels has increased. The main desired features of these fault current limiters are [3]:

- Zero impedance under normal operating conditions
- High impedance under fault conditions
- Fast transition from normal to limiting mode
- Fast recovery to normal operation after fault is interrupted
- High reliability over long periods with minimal maintenance
- Limited volume and weight
- Low cost

Obviously the ideal fault current limiter does not exist. However, any practical device should meet the ideal requirements as far as possible.

Fault current limiting devices can be divided into two main categories: superconducting and non-superconducting. Although research into fault current limiters based on superconducting materials has made progress in the last few years, it is likely to be some time before they become commercially available for high voltage transmission applications. Research is continuing to make these devices technically efficient and economically attractive. Non-superconducting fault current limiters are based on power electronic devices with conventional series reactors or a combination of capacitors and reactors. A small number of non-superconducting dynamic fault current limiters are in commercial operation in high voltage transmission systems. One approach for this power electronic based device is the TCSC.

In this paper the TCSC's capability of acting as a fault current limiting device will be demonstrated and some interesting aspects with regard to this operation will be discussed. An important aspect of the TCSC fault current limiter is the detection of the fault condition. A method of fault current detection based on the rate of rise of the line current will be described. Finally a brief assessment of voltage sags in a power system with a TCSC fault current limiter will be made.

II. THE TCSC MODEL FOR THE EMTP-ATP PROGRAM

A simplified diagram of the TCSC model for the EMTP-ATP program is shown in Fig. 1. A detailed description of the modelling can be found in [1,4,5]. The TCSC is divided into three distinct systems: power circuit; measurement and control systems; firing and synchronisation systems.

The power circuit is composed of a capacitor bank in parallel with a thyristor controlled reactor (TCR) and a MOV arrester to protect the capacitor. The thyristor valve includes a snubber circuit. All components were modelled using conventional, built-in EMTP models.

The measurement and control systems work independently in each phase, and consist of band-pass and notch filters, a current quadratic measurement device, and a proportional-integral (PI) controller. A comparison between the measured line current and the reference current is made, and the error generated is fed into the PI controller whose main function is to bring to zero its steady-state error. An open loop impedance mode is possible in addition to the closed loop current control mode. In this mode a reactance order is set and the firing system then provides a suitable firing angle order to the thyristors.

The synchronisation and firing systems comprise a linearisation curve, a pulse generating unit and a synchronisation unit that is based on either an individual firing pulse (IFP, i.e. current zero crossings) or an equidistant firing pulse (PLL- phase locked loop system). All control blocks of control/measurement and synchronisation/firing systems were modelled using ATP-TACS (Transient Analysis of Control System).

There are three special modes of operation: thyristor switched reactor (TSR), thyristor blocked mode (TBM) and waiting mode (WTM). These modes of operation are activated in special circumstances by the operation mode selector. TSR means that the thyristors are fully conducting. In this condition the capacitor bank is bypassed through the TCR, and the TCSC impedance changes rapidly from a capacitive value to an inductive one. This mode provides the means of limiting the line current by increasing the line impedance by a value that depends on the design of the TCSC. The WTM means that the TCSC waits for a certain time with a fixed firing angle until another mode of operation is set. The TBM means that the PI regulator and firing system are blocked, and the TCSC will operate at 180°.

III. UNDERSTANDING THE ABILITY OF THE TCSC IN LIMITING FAULT CURRENTS

TCSCs are already being utilised for power flow control and dynamic compensation, and they may also be used for minimising short circuit effects. The TCSC's ability to adjust its impedance rapidly can be used for limiting fault currents. Through the TSR mode the TCSC is able to pass from a capacitive range of operation to a fixed inductive impedance. This feature takes full advantage of the inherent speed of solid-state devices. The TCSC impedance in TSR mode can be expressed by (1), as follows:

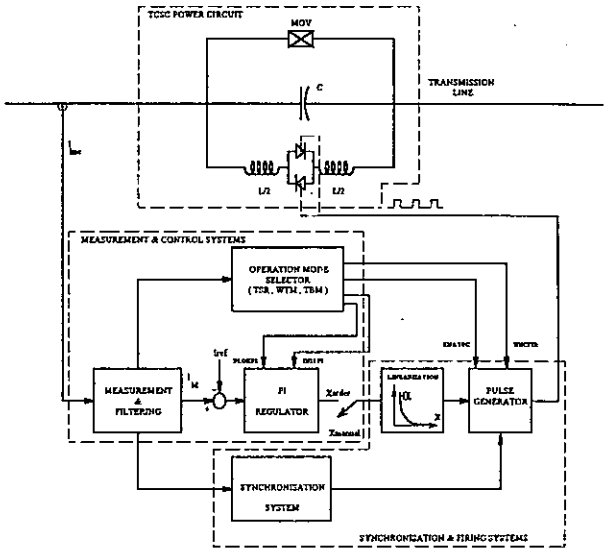

Fig. 1. Structure of the TCSC modelling

$$X_{TSR} = jX_C X_L / (X_C - X_L) \qquad (1)$$

where X_C = capacitor reactance
X_L = inductor reactance

To perform as a fault current limiter the TCSC has to be dimensioned to withstand the short circuit current and present a high inductive impedance. As a consequence it is necessary to change some characteristics of the TCSC, such as equipment ratings and natural resonant frequency of the LC circuit. The natural resonant frequency of the TCSC circuit is given by (2), expressed in per unit of the fundamental frequency [1]:

$$k = \sqrt{X_C / X_L} \quad pu \qquad (2)$$

In addition, the firing angle α in which the TCSC develops a resonance can be expressed by (3), as follows [1]:

$$\alpha_r = \pi - (2n-1).\frac{\pi}{2k} rd \quad \text{for } n = 1,2,\ldots \qquad (3)$$

In order to limit the fault current one could think simply of putting a single reactance in series with the transmission line. Such a scheme is sometimes used for industrial applications. However, this has some disadvantages in the steady-state such as increase of losses and voltage drop. Although TCSCs also add losses to the power system, they may be located in such a way as to decrease the global losses. Moreover TCSCs can use their reactors to take advantage of the boost effect whereas series reactors operate in a directly proportional way.

Table 1 shows the inductor reactance (X_L) in per unit of the capacitor reactance (X_C) and the equivalent inductive reactance (X_{TSR}) when the TCSC is operating in TSR mode. This table also shows the natural resonant frequency (f_o, in Hz), the resonant angle (α_r), the natural resonant frequency k (in pu), and the boost factor ($B=X_{TSR}/X_L$).

Table 1 was generated from (1),(2), and (3). As can be seen, the higher the reactance X_L, the higher the boost factor B. The boost factor increases from 1.111 pu (for X_L=0.1 pu) up to 10 pu (for X_L=0.9 pu). From the fault current limiting point of view a higher boost factor is preferred, although the natural resonant frequency is then closer to the fundamental. It should be noted that for X_L=0.1 pu the TCSC has two resonant angles (151.54° and 94.61°) in the range between 90° and 180°, and consequently such a TCSC design should be avoided. On the other hand, a value of X_L=1 pu means that the TCSC is resonant at the fundamental frequency, which must also be avoided.

As a trade-off solution a reactance X_L= 0.7 pu appears to be a reasonable compromise giving a resonant frequency around 71 Hz and a boost factor of 3.333 pu, i.e. the equivalent inductive reactance in TSR mode (X_{TSR}) is 3.333 times that of the reactor (X_L). This leads to a factor k=1.195. This same factor k was also used in [6]. The criteria above were adopted for the TCSC investigated in the EMTP simulations. However, special care should be taken since power systems may have specific resonant problems and the values quoted here are not proposed as general recommendations.

IV. TCSC RATINGS AND POWER SYSTEM STUDIED

The TCSC was rated for -j21 Ω to -j52 Ω continuously. This corresponds to the following TCSC parameters: f=60 Hz, C=126.31 μF (X_c=-j21 Ω) and L=38.99 mH (X_L=j14.7 Ω). The linearisation curve was calculated using specific software developed for this purpose [1]. Its firing angle range varies from 114° to 180°. A surge arrester (MOV) rated for 33 kV was used for protecting the capacitor bank against overvoltages.

The power system simulated consists of a 100 km, 230 kV transmission line that feeds three loads in a ring configuration. All transmission lines in the ring configuration have a length of 30 km and the loads can be said to be electrically close to each other. All loads are considered to have a power factor of 0.85. The loads are: S2 = 50 MVA, S3 = 70 MVA, and S4 = 20 MVA. Fig. 2 shows the power system under study. The short circuit capacity at bus 1 is 10 GVA.

The TCSC is placed in series with the transmission line 1-2 in order to demonstrate the capability of such a piece of equipment in limiting fault currents. This TCSC was rated to vary from -j21 Ω up to -j52 Ω, i.e. virtually a compensation degree of 100%. In the TSR mode the TCSC has an impedance of j49 Ω which almost doubles the line impedance in this condition.

Although simple, this radial power system illustrates some interesting features of the TCSCs with regard to fault current limiters.

Table 1. Boost effect as a function of the inductor reactance

X_L (pu)	$k=f_o/f$ (pu)	fo (Hz)	α_r (°)	X_{TSR} (pu)	B (pu)
0.1	3.162	189.74	151.54, 94.61	0.111	1.111
0.2	2.236	134.17	139.75	0.250	1.250
0.3	1.825	109.54	130.70	0.428	1.428
0.4	1.581	94.86	123.08	0.666	1.665
0.5	1.414	84.85	116.36	1.000	2.000
0.6	1.291	77.46	110.28	1.500	2.500
0.7	1.195	71.71	104.70	2.333	3.333
0.8	1.118	67.08	99.50	4.000	5.000
0.9	1.054	63.24	94.61	9.000	10.00

V. DEMONSTRATION OF THE TCSC AS A FAULT CURRENT LIMITER

The criterion to demonstrate the TCSC capability in limiting fault current was chosen as a three-phase to ground short circuit applied somewhere in the power system shown in Fig.2. However, the fault current detection is made independently per phase in such a way as to ensure correct operation even with unbalanced faults.

By using the TSR mode feature, it is possible to change the TCSC impedance from capacitive to inductive in a very short time. Although the mechanism for changing the TCSC impedance is very rapid, it is important to note that a rapid logic device should also be used for deciding whether a fault condition is occurring or not.

Two different strategies for identifying the fault condition were studied. One is based on the line current amplitude and the other is based on the rate of rise of the line current.

A. Detection Based on Line Current Amplitude

The overcurrent detector based on line current amplitude was simulated together with the TCSC model. A three-phase to ground fault was applied to bus 2 (Fig.

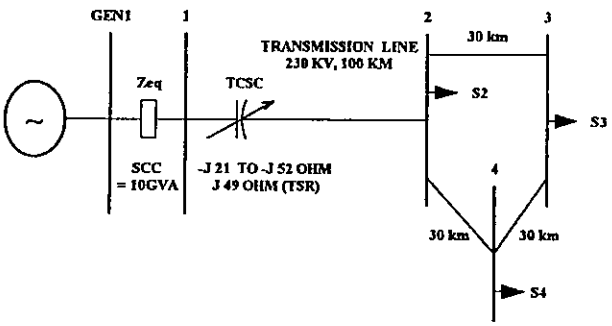

Fig. 2. One-line diagram of the power system

2). The results are shown in Fig. 3. Fault currents are seen from bus 1.

The fault was applied at $30x10^{-3}$ s but the overcurrent detectors identified a fault condition at $34.95x10^{-3}$ s, $37.90x10^{-3}$ s, $36.90x10^{-3}$ s respectively for phase A, B, and C. The pickup values used for these overcurrent detectors were set to 2000 Arms.

As can be seen from this simulation for phase B (Fig. 3.b), the TCSC using detection based on line current amplitude is not able to limit all peaks of the fault current. The largest current peak in phase B was increased from 3337 A to 4245 A (increase of 27%). However, the highest current peak in the three phases was reduced from 5225 A to 4233 A (reduction of 19%). If an effective limitation during the fault in all current peaks and phases is required, a fault detector based on a predictive strategy, e.g. rate of rise, should be used. Otherwise a fault detector based on current amplitude is likely to be adequate.

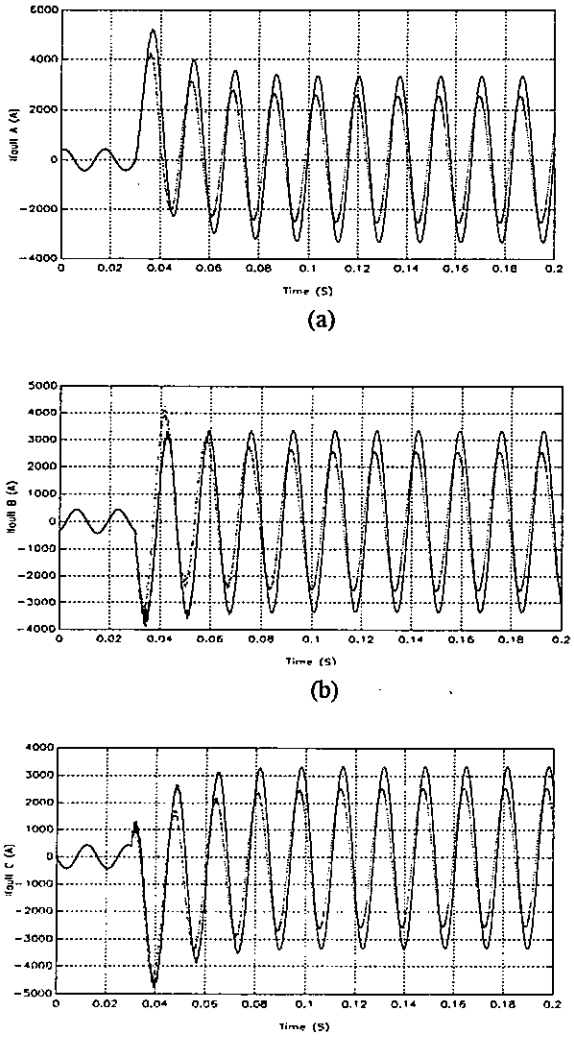

Fig. 3. Fault currents for phases A,B, and C - fault current amplitude (dotted: with TCSC / solid: without TCSC)

B. Detection Based on the Rate of Rise of the Line Current

The rate of rise of line current is found using a washout filter, after the current quadratic measurement device, tuned to give a suitable response[1]. The washout filter has the following transfer function:

$$F(s) = k_d s/(1+T_d s) \qquad (4)$$

The simulation with the fault detection based on the rate of rise of the line current is shown in Fig. 4. A three-phase to ground short circuit was applied to bus 2 (Fig. 2) at $30x10^{-3}$ s and it remains until the end of the simulation ($200x10^{-3}$ s). Fault currents are again seen from bus 1.

As can be seen, the TCSC using a fast fault detector is able to limit the fault current even in its first peak in all of the three phases. The highest current peak in the three phases, which occurred in phase A, was reduced from 5225 A to 4270 A (reduction of 18%). The steady-state current peaks were reduced from 3343 A to 2550 A

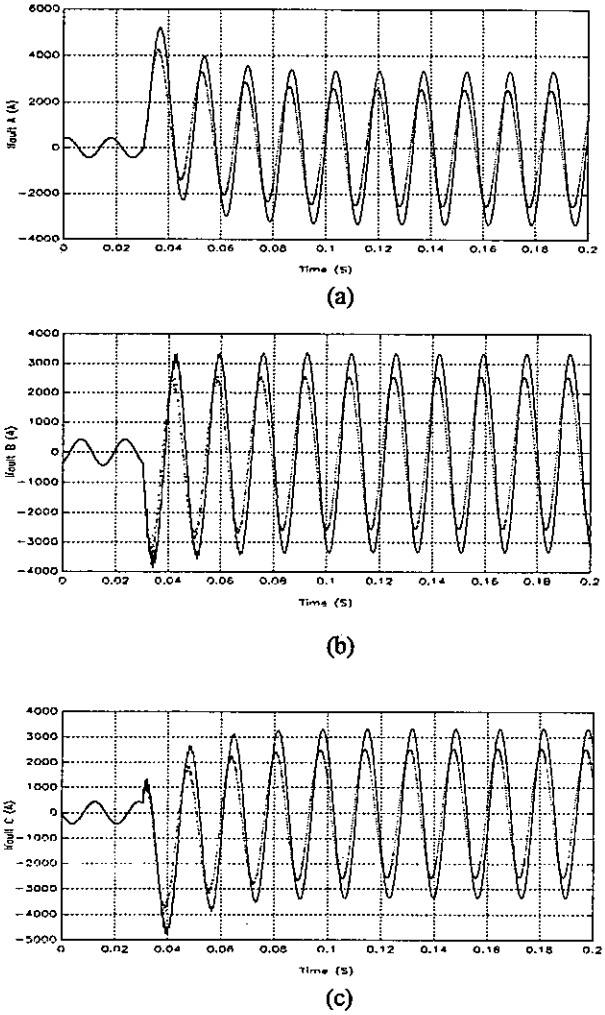

Fig. 4. Fault currents for phases A, B, and C - rate of rise of the current (dotted: with TCSC / solid: without TCSC)

(reduction of 24%). The fault detectors were adjusted for a pickup value equal to 100 pu/s and they identified a fault condition at 30.80×10^{-3} s, 30.47×10^{-3} s, 31.24×10^{-3} s respectively for phase A, B and C. The rate of rise of 100 pu/s was a conservative value only achieved in short circuits and even considering this high value a very fast detection was observed.

This fault detector puts the TCSC in the TSR mode when a rate of rise of the line current is greater than a pickup value (here 100 pu/s). The TCSC remains in the TSR mode for a time equal to a set value (here one cycle). After that, this device resets the TSR mode when a line current is less than a reset value (here 1000 Arms) for a time longer than a reset time (here one cycle). The setting of this device depends on the power system in which it will be used. In actual applications, studies should be carried out in order to determine optimum settings.

The instant of application of the fault was varied in order to sweep a whole cycle. The fault location was also varied. The results showed that the TCSC with a fast fault detector is an effective fault current limiting device for different instants of fault application and different fault locations. There was a 17% average decrease for the highest current peak and 24% for steady-state current peaks [1].

With regard to the surge arrester's energy absorption, it may be noted that up to 200×10^{-3} s the maximum energy absorption was around 15 MJ, which is in accordance with the commercially available arrester's duties. The TSR mode, i.e. thyristors fully conducting, acts as an additional protection against overvoltages on the capacitor bank, since the TCR presents a smaller impedance path for the fault current, so decreasing the surge arrester's duties.

C. TCSC Re-synchronisation after Limiting Fault Current

In order to study the TCSC re-synchronisation after the fault removal, a three-phase to ground fault was applied to bus 2 (Fig. 2) at 30×10^{-3} s and it was removed at the first current zero after 130×10^{-3} s. Fig. 5 shows the results of this simulation with regard to phase A. After the fault removal, when the line current falls below 1000 A rms, the TCSC is reinserted into the circuit. In this reinsertion a DC current offset appears in the line current. Fig. 5 shows two current waveshapes overlapped.

The dotted current waveshape was plotted with the TCSC working on individual firing pulses, whereas the solid current waveshape shows its operation based on the PLL system. As can be seen the PLL-based system rapidly damps the DC offset out. The TCSC operation based on individual firing pulses provides a less damped response. However, both firing strategies are able to damp the DC offset out. It may be concluded that the PLL-based system is more effective regarding TCSC re-synchronisation.

With respect to the surge arrester's absorption, it may be noted that the maximum absorption occurred on phase B and the amount of energy required is about 9.4 MJ.

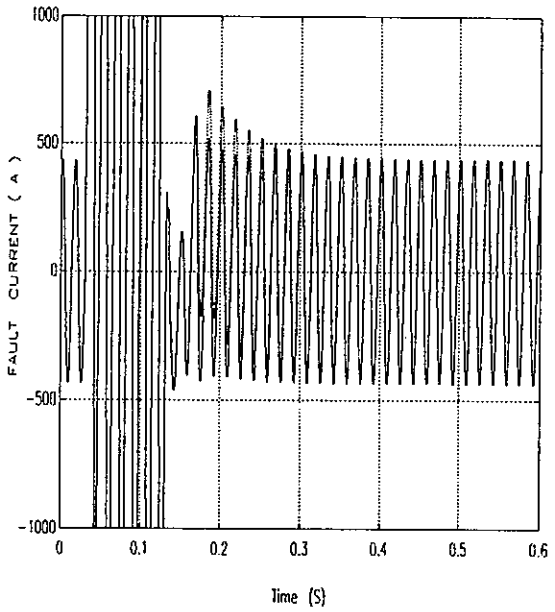

Fig. 5. Damping of the DC current offset
(dotted: with IFP / solid: with PLL)

VI. A BRIEF ASSESSMENT OF THE VOLTAGE SAG BY USING TCSC FAULT CURRENT LIMITER

A voltage sag is a reduction in voltage with a duration between half a cycle and several seconds. Voltage sags are a well known issue in power systems that nowadays is gaining significance due to the growth of sensitive loads. The major problem is to know whether the sensitive load will trip or not when a sag occurs in a power system. Power quality surveys reveal that 80% to 90% of the customer's problems are due to voltage sags [7]. Most of them are due to short circuits in the power system.

A simple model for calculating the sag magnitude (the voltage magnitude during the sag) can be seen in Fig. 6. This model is based on a voltage divider and it is particularly useful for radial distribution systems. Nevertheless, it serves to describe and explain the phenomenon in a simple and clear way. First of all it is necessary to determine the point-of-common-coupling (PCC) and its short circuit impedance (Z_1), i.e. the system equivalent that combines all the rest of the power system. It is also necessary to work out the reactance between the PCC and the fault location (Z_2). If the fault impedance is neglected or included in Z_2 the sag magnitude can be expressed by (5):

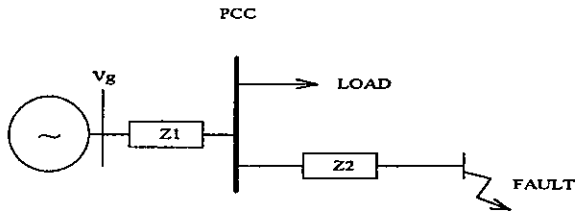

Fig. 6. Simple model for assessing voltage sag

$$V_{sag\ magnitude} = \frac{Z_2}{Z_1 + Z_2} V_g \qquad (5)$$

where V_g is the equivalent source voltage.

By considering (5), it is easy to conclude that to decrease the sag severity (i.e. increase $V_{sag\ magnitude}$) , it is necessary to decrease the impedance Z_1 (strengthen the power system) and/or increase Z_2 (weaken the fault path from the PCC). It should be noted that these requirements are sometimes conflicting because the PCC for a particular configuration may be the fault location for another one.

The TCSC can be used to weaken the fault path by introducing an inductive impedance (TSR mode) in the same way it does as a fault current limiter. Then, when the TCSC is limiting fault current, it also improves the power quality of the supply by mitigating sag severity.

To demonstrate the TCSC capability in enhancing sag severity, a sensitive load is considered to be connected to bus 1 (Fig. 2) and a three-phase to ground short circuit is applied along the transmission line 1-2. The fault location was varied in intervals of 10 km. The results of this simulation are summarised in Fig. 7.

As can be seen from Fig. 7, the sag severity of the transmission system compensated by a TCSC is less than that of the uncompensated transmission line. For example, consider a sensitive load that trips for a sag magnitude of 80%. With the TCSC the critical distance (least distance from the PCC in which a fault still causes load tripping) is roughly 25 km. Without the TCSC the critical distance is 40 km. For this particular sensitive load, the TCSC decreases the critical distance (and thus the number of trips) by about 40%.

VII. CONCLUSIONS

The TCSC capability of limiting fault current has been demonstrated. Two strategies have been studied for fault detection. One is based on current amplitude, whereas the other is based on the rate of rise of the line current. The latter is a very fast detection strategy useful for effective limitation even of the first peaks of the fault current.

The TCSC is able to meet the apparently contradictory requirement of increasing transmission capacity with a decrease of the fault levels. All TCSC equipment must be designed to withstand fault current and its effects. The surge arrester's energy requirements are within the range of commercially available arrester's absorption.

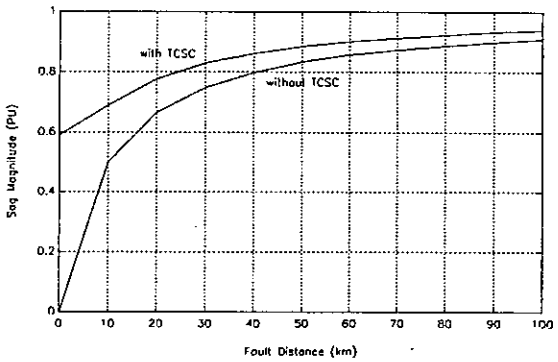

Fig. 7. Sag magnitude as a function of the distance to PCC

A PLL-based synchronisation system seems to be more efficient in damping the DC current offset after fault interruption following the TCSC reinsertion.

As a consequence of its current limiting action, the TCSC can also enhance the quality of the supply by decreasing voltage sag severity.

VIII. ACKNOWLEDGEMENT

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