DISTANCE RELAYING IN ENVIRONMENT OF ADVANCED SERIES COMPENSATION DEVICES

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Abstract-**The paper investigates the fault conditions for distance relays operating in the environment of both fixed and controllable series compensation devices. The model of a GTO-based scheme for the series compensation of long transmission lines is presented. The behaviour of seven digital distance relays installed in different places of the system is studied. Particular emphasis is placed on: short-circuits on the compensated lines, fast power modulation actions taken by the power controller and short-circuits in the controllable series compensation device itself. Conclusions derived from the digital simulation of the system are presented which discuss the response of the distance relays in the presence of series compensation.**

keywords: FACTS, series compensation, power system protection, distance relaying.

I. INTRODUCTION

Flexible AC Transmission Systems (FACTS) offer an option for the exchange of energy over very long distances providing flexible operation of the power system. The term FACTS covers a range of plants and equipment such as High Voltage Direct Current transmission systems (HVDC), Controlled Series Compensators (CSC) and Static Var Compensators (SVC). FACTS devices become increasingly important to the power system operation. Their proliferation is expected to affect the traditional method of protection design. The efect of FACTS devices on the system protection is yet to be analysed effectively. Converter-related transient phenomena occur during control of FACTS devices, switching operations and short-circuits in the AC system. All this affects operation of protective relays installed in such environment [1,2]. In critical cases it is necessary to carry out extensive simulations in order to verify existing designs, adjust settings of the relays and search for new developments.

This paper is focused on the analysis of fundamental frequency based distance relays operating in the vicinity of CSC schemes combined with fixed series capacitors. The paper presents the compensation scheme with its control, analyses transient phenomena in the system, studies operation of distance relays installed, and gives recommendations with respect to the design of the relays and their settings.

II. THE STUDIED SYSTEM

The series compensation scheme shown in Fig.1 is primarily designed to increase the power loadability between the areas I and II through the two parallel lines L_1 and L_2. The scheme combines fixed series compensation with the small rating series connected GTO inverter.

The Series Capacitors (SCs) are protected against overvoltages using Metal Oxide Varistors (MOVs), which, in turn, are protected from overheating by their energy-based thermal protection [3,4,5]. The degree of series capacitive compensation is limited by the risk of subsynchronous oscillations and is adjusted at 60%.

Additional increase of transmittable power is achieved by a VSI. The six-pulse Voltage Source Inverter (VSI) is connected via an interface Series Transformer (ST) into the line. The line side of the ST consists of three independent windings, while the valve side is Δ-connected for the circulation of triplet harmonics. The series AC voltage injected by the scheme either leads or lags the line current by exactly 90°. Thus, the VSI acts as a source of pure leading or lagging reactive power. The main gain of this scheme, comparing with the fixed compensation, is that the injected voltage is controlled independently from the line currents. Like the SCs, the ST is protected by its MOVs and their thermal protection.

The VSI compensator controlls within its capability the line power. Its control is shown in Fig.2 and comprises of four main loops [6]:

(1) The grid Control loop fires the GTOs according to the Pulse Width Modulation (PWM) technique with fixed frequency modulation index.
(2) The synchronizing loop measurers the line currents and provides stable phase shift either +90° or -90° between the injected AC voltage and the line current.
(3) The DC Voltage Stabilizer keeps the DC voltage across the DC Capacitor within the pre-defined limits ensuring certain margin of reaction for the whole scheme.

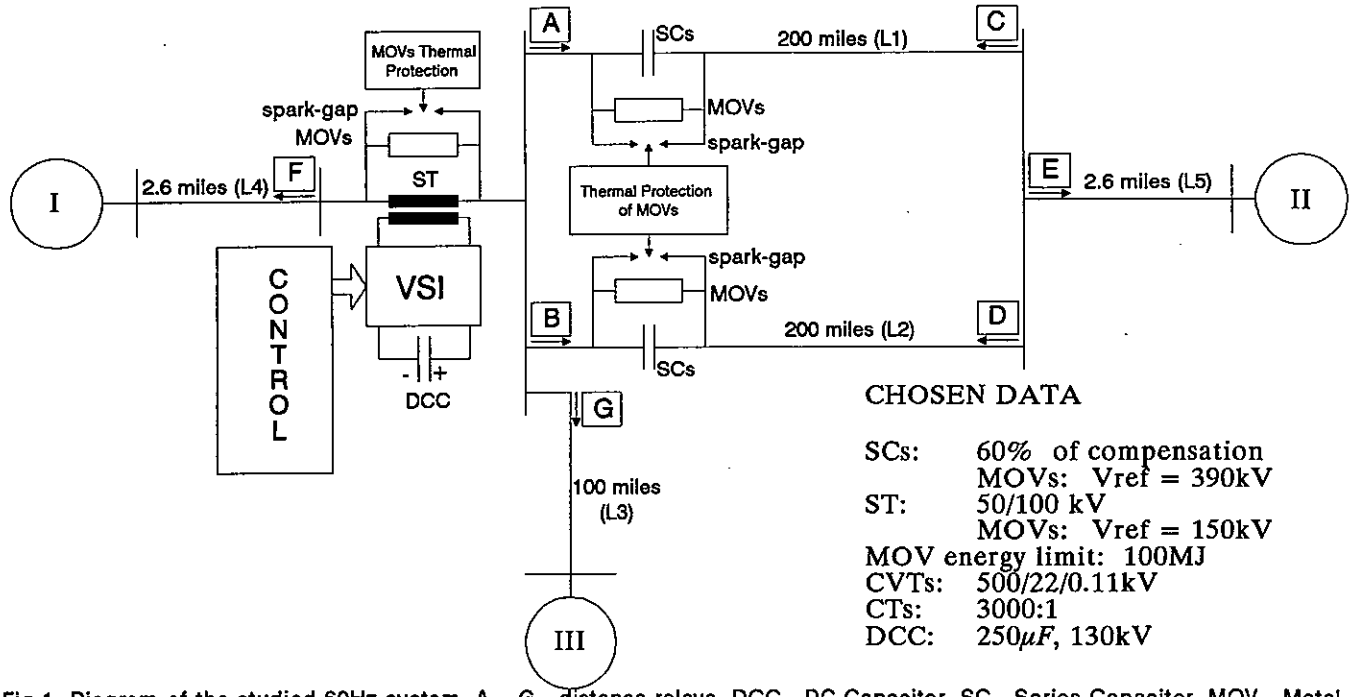

Fig.1. Diagram of the studied 60Hz system. A .. G - distance relays, DCC - DC Capacitor, SC - Series Capacitor, MOV - Metal Oxide Varistor, ST - Series Transformer, VSI - Voltage Sourced Inverter.

(4) The Active Power Modulation loop controls the power flow of the line within the capability of the VSI.

III. The Distance Relays

With reference to Fig.1, seven locations (A to G) are chosen for the distance relays.

All the elements of the measuring chain of a relay have been taken into considereation. Capacitive Voltage Transformers (CVTs) are represented by their 4th order linear models while Current Transformers (CTs) are simulated taking into account their saturation branches [7]. The analog anti-aliasing filters are represented by the 2nd order approximation with the cut-off frequency set at ⅓ of the sampling rate [8].

ATP-EMTP [9] has been used as a simulation tool.

Numerous simulations have been performed using the developed model. The studied factors include: variety of control actions taken by the power controller; pre-fault power flow; fault type, location, resistance and inception angle; source impedances; energy limit for the MOVs; and others.

Such statistical picture taken for the considered system enables to draw a number of conclusions regarding the operating conditions for the distance relays installed close to the CSC schemes.

IV. The Sample Cases

A. Short-circuit on the line L1

The VSI produces lagging vars when the R-to-S short circuit occurs in the middle of the line L_1. Fig.3 displays the phase currents measured by the relay A. The MOV in the phase R on the line L_1 operates for 112ms and next becomes by-passed on the command of its thermal protection. It causes visible change in the line currents. 233ms later, the MOV in the phase S is shunted and the fault loop becomes resistive-inductive what reflects in the decrease of the fault currents (no compensation on the line). During the fault, the phase currents on both sides of the line (the relays A and C) display considerable distortions with components of comparatively low frequency (including the healthy phase, Fig.4).

The VSI operates to maintain the reference power

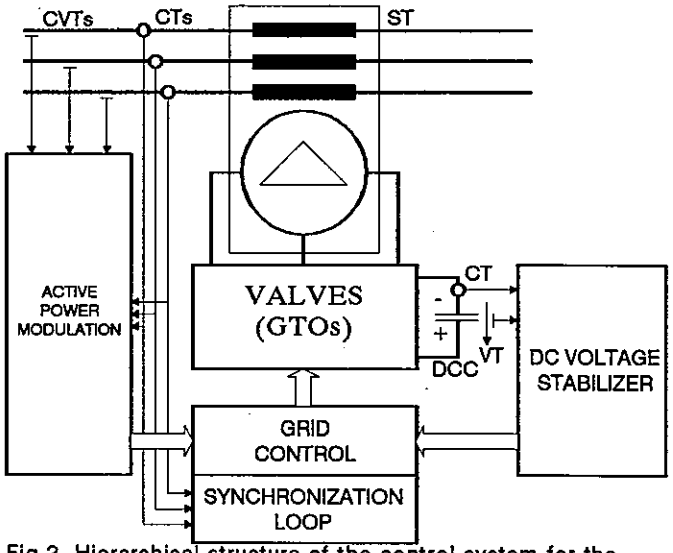

Fig.2. Hierarchical structure of the control system for the series connected VSI.

what causes certain slow changes in the amplitudes of the currents (Fig.3).

In the first stage of the fault, the relay A sees the fault much closer than actually located (due to the equivalent RC circuit of the SCs and the MOVs [4]); after shunting the MOVs, the impedance trajectory of the relay A moves to its natural position (onto the line impedance vector, Fig.5a). The relay C behaves like in the case of a conventional line since it does not see the SCs in the analyzed fault loop (Fig.5b).

Conclusions

During faults on a series compensated line:

(a) the relay which sees a fault through the series capacitors (relay A) may overreach and in the classical approach its first zone reach should be set at no more than 0.7 x (1 - *compensation rate*),

(b) the relay which sees a fault behind the series capacitors (relay A) faces the known problems of voltage and current inversion what may cause both the first zone unit and the directional element to fail [2,10],

(c) the relays that do not see the series capacitors in their fault loops (relays C, D and E) operate as in the case of a traditional (non-compensated) transmission line,

(d) the relay on a sound parallel line (relay B) sees the series capacitors in its fault loop also when a fault occurs on the parallel line (L_1) and it is partly affected by the phenomena caused by the series capacitors (overreaching); however, the possibility of false tripping is small since for a fault on the line L_1 the whole line L_2 is included in the fault loop of the relay B,

(e) during low current faults, the MOVs may not operate and do not damp the subsynchronous oscillations; such as oscillations are a source of considerable measuring errors for all the relays operating in the vicinity of the series compensated line under a short-circuit [10],

(f) asymmetrical triggering of spark-gaps protecting

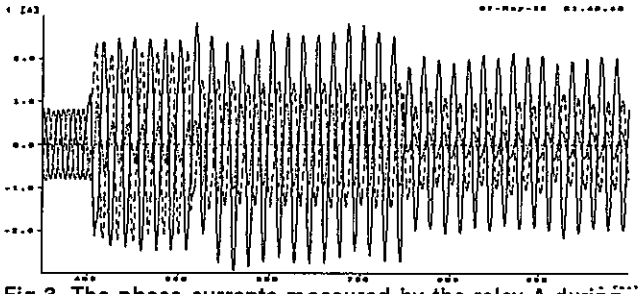

Fig.3. The phase currents measured by the relay A during the R-S fault in the middle of L1.

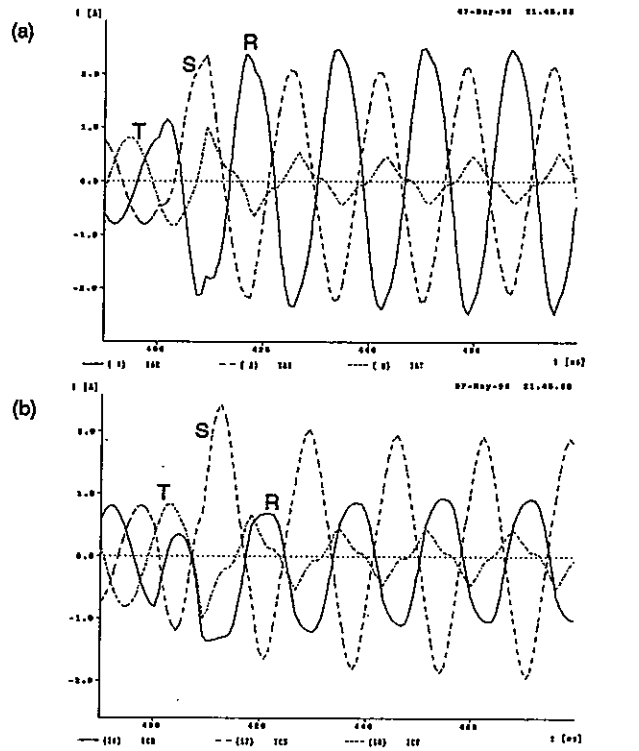

Fig.4. The phase currents measured by the relay A (a) and C (b) during the R-S fault in the middle of L1.

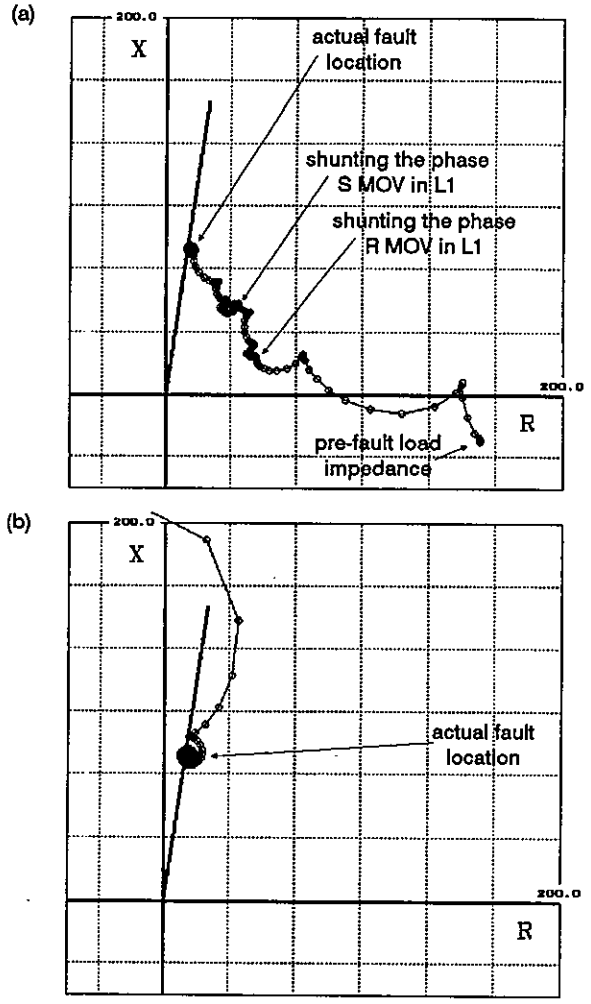

Fig.5. Impedance trajectories of the relay A (a) and C (b) for the R-S fault in the middle of the line L1 (full-cycle Fourier filters used for the measurement [8]).

the MOVs from overheating makes the whole system unbalanced and affects both the relays and the power controller itself,

(g) the power controller tries to maintain the ordered power transfer during short-circuits and other events (triggering the spark-gaps), what reflects in subsynchronous oscillations in the currents and affects the impedance measurement,

(h) in general, however, the fixed series capacitors and their MOVs mitigate the power controller itself as far as distance relaying is considered,

(i) the measuring algorithms for distance relays should take into account: 1) the possibility of subsynchronous oscillations and 2) the harmonic profile of currents due to operation of both the MOVs and the VSI [11],

(j) the power control scheme remains stable during majority of faults on the lines L_1 and L_2 and there is no need to shut it down even for long fault clearing times.

B. Power modulation

The considered power system is sound, but the power transmitted between the areas I and II is modulated as shown in Fig.6a.

The currents measured by the relays located on the power transfer channel (relays A to F) activate all the relays.

The impedances measured by the first zone units of the relays A to F move on the impedance plane. However, as shown in Figs.6b and c, there is no danger of false trippings.

During the modulation of the transmitted power, the measured impedance components display the oscillations of the subsynchronous nature even for smooth changes of the power (Figs.6d and e).

Conclusions

In a sound system with the power controller operating:

(a) the relays installed in the vicinity of the VSI activate during both ramp and step changes of the reference power,

(b) there is no danger of false trippings since the measured impedances although move on the impedance plan, but keep away from the first zone region,

(c) during smooth changes of the transmitted power, the measured impedances show oscillations with the period of 100ms or more; such oscillations may cause certain problems for power swing blocking units of the relays [8].

C. Fault in the Series Transformer (ST)

The VSI operates in the leading mode when a phase-R-to-ground fault occurs on the line side of the ST close to the busbar of the relays A and B (Fig.1). The system I is very powerful and supplies the fault current at the level of 200kA (Fig.7a). The MOV across the phase R of the ST limits the voltage drop to 150kV, but gets by-passed on the command of its thermal protection 188ms after the fault inception. This operation increases even more the fault current since it is only limited by the impedance of the line L_4 (Fig.7a).

The voltage measured by the relays A, B and G drops almost to zero in the faulty phase R (Fig.7b). In the sound phases, in turn, certain subsynchronous oscillations occur (Fig.7c). The phase R current in the line L_1 increases due to the short circuit, but not dramatically (Fig.7d). The very large current through the phase R winding of the ST induces certain changes in the sound phases S and T due to the coupling via the VSI side of the ST and the VSI itself. Therefore, the currents in the phases S and T of the lines L_1, L_2, L_3 and L_4 change although a single-phase-to-ground fault takes place. The phase S current increases (Fig.7e), while the phase T current decreases (Fig.7f). In addition, certain oscillations are observed in these signals.

The phase S current in the lines L_1 and L_2 is so significant that makes the MOVs operating and bypassed 515ms after the fault inception. After this event, the lines L_1 and L_2 are asymmetrical since only the phases R and T are series compensated.

Due to the increase of the phase S current, the relays A, B, C, D, E and G would probably detect a phase-to-phase fault instead of the actual phase-to-ground fault. The maloperation of the phase selection unit of the relays results in serious consequences. The transient R-to-S impedance (incorrectly selected as the measure of the distance to a fault) of the relays A, B, C, D and G enters the first quarter of the impedance plane what would probably cause false trippings (Fig.8).

Taking into account the currents measured by the relay F (Fig.7a), it will make the proper phase selection and operate correctly, but only if the directional element operates correctly (the impedance itself assumes zero - Fig.8c).

The relay E, in turn, measures approximately half the impedance of the relay C (Fig.8b), but watches the opposite direction and therefore will operate correctly.

Conclusions

During faults in the ST and/or the VSI circuits:

(a) the sound phases may be significantly affected what leads to incorrect phase selection and in consequence to maloperation of the relays,

(b) the power controller operates rapidly and close to its limits what reflects in extra oscillations in both currents and voltages,

(c) failure of the ST and/or the VSI may lead to unexpected events such as shunting the MOV in the connected lines, but in the sound phase.

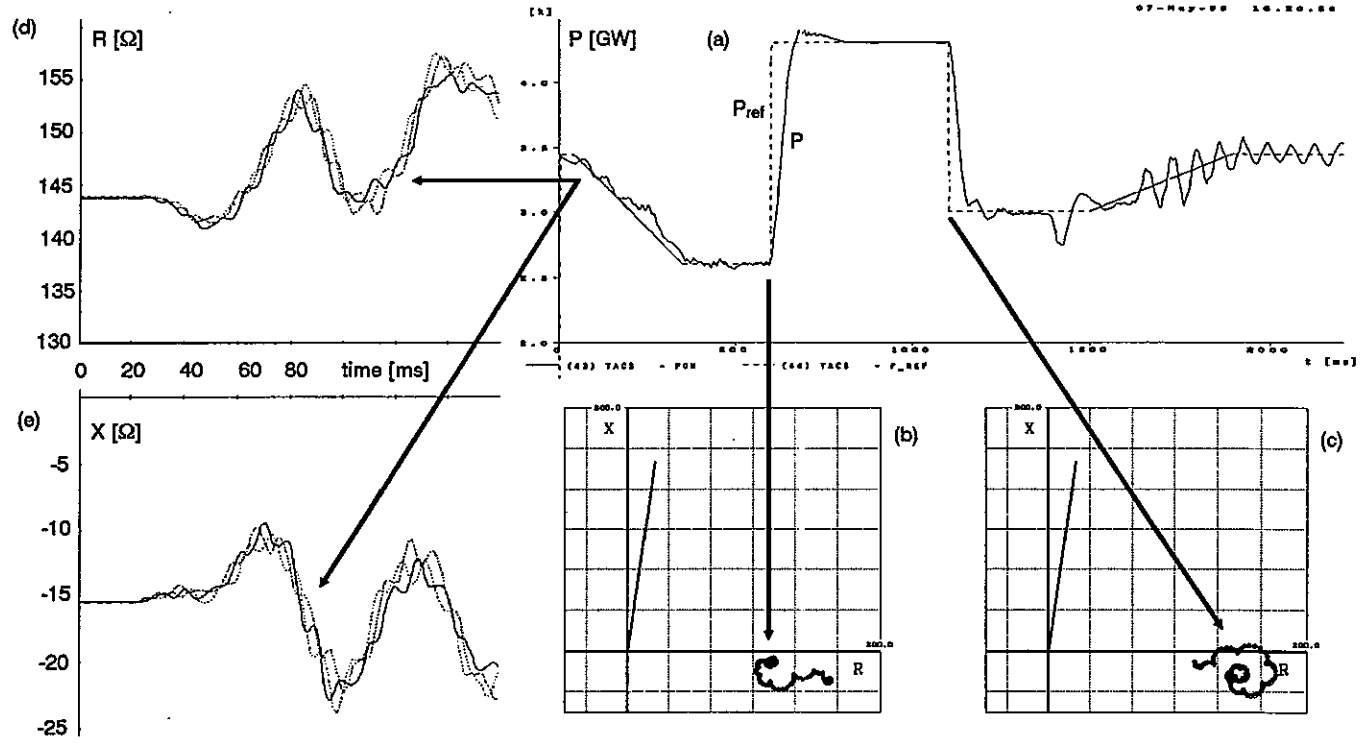

Fig.6. The effect of power modulation. The reference and actual power (a), the impedance trajectory of the relay A (fault loop R-to-S) at the step increase of the power (b) and the step decrease of the power (c), the impedance measured by the relay A (fault loops R-to-S, S-to-T and T-to-R) with the use of full-cycle Fourier algorithm during the ramp change of the reference power - the resistance (d) and the reactance (e).

IV. Conclusions

The paper presents the model of a sample power system including: • controllable series compensation scheme based on a VSI together with its control system and overvoltage/thermal protection, • fixed series capacitors on two parallel lines together with their overvoltage/thermal protection, and • a number of digital distance relays with their CVTs, CTs and anti-aliasing analog filters.

Numerous simulation runs have been performed in this system. Particular emphasis has been placed on: • short-circuits on the transmission lines, • fast power modulation actions, and • faults in the VSI circuits themselves.

The behaviour of the distance relays installed in such as system has been studied. Particular attention has been paid to: • measuring algorithms including the sub-synchronous oscillations and the harmonic profile of the signals, • distance overreaching, • voltage and current inversion, and • power swing blocking, directional and phase selection units of the relays.

A number of phenomena affecting operation of the distance relays have been pointed out. A number of recommendations have been given with respect the relay design and setting.

Complexity of the fault phenomena and mutual influence of the installed devices call for tide integration of the protective relays, the protective devices of the ST and SCs, the fault protection of the ST, and the control algorithm of the VSI itself.

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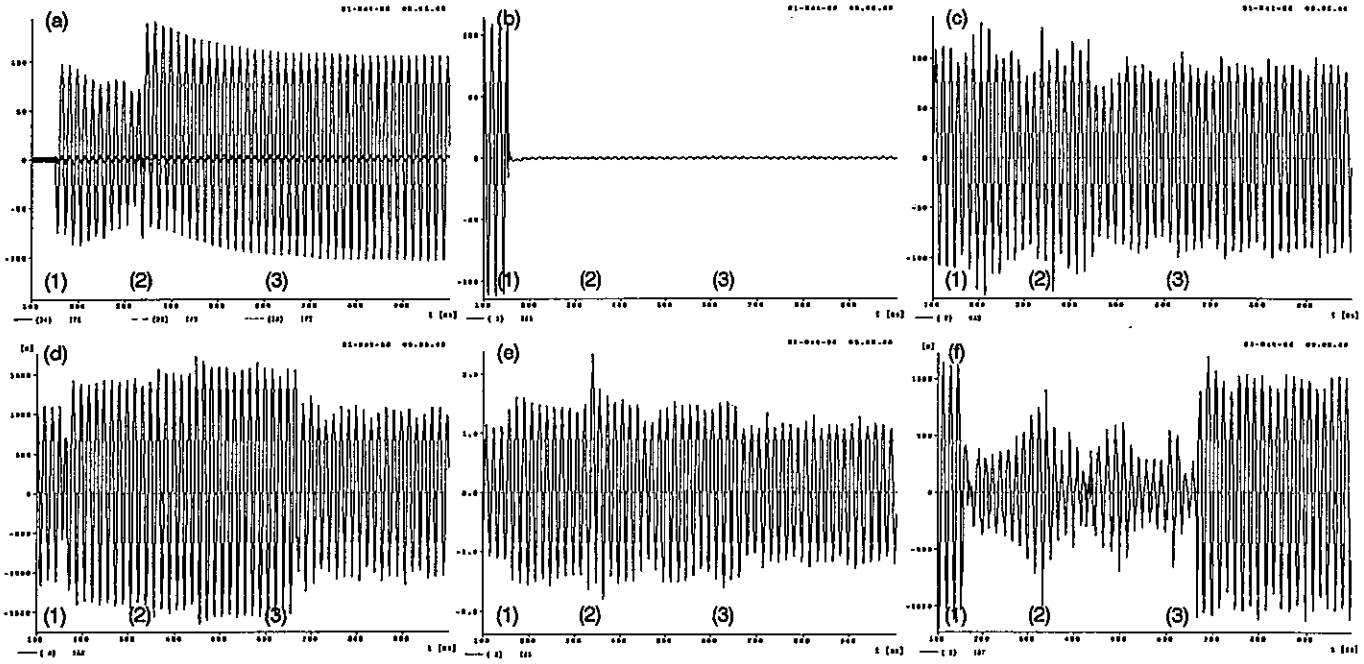
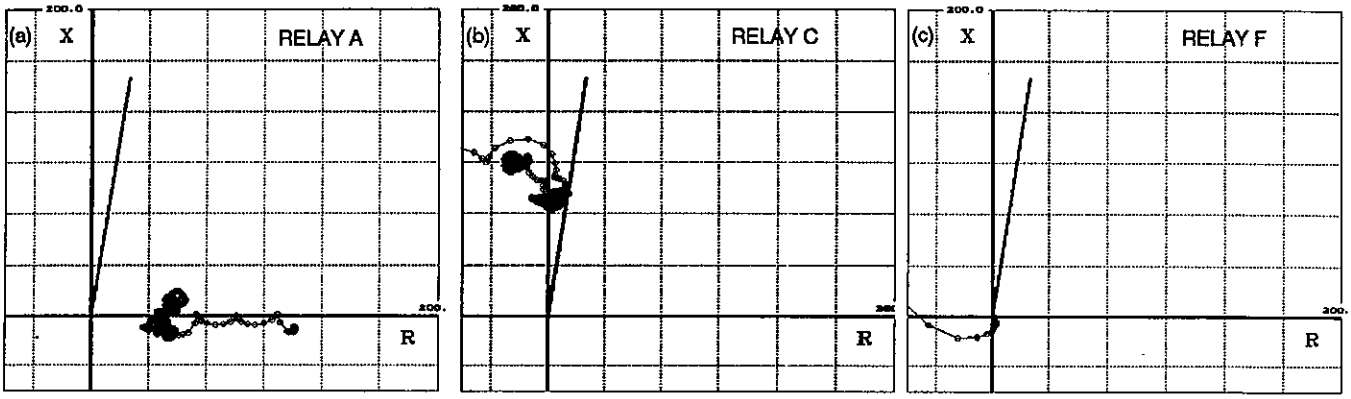


Fig.7. Short-circuit in the ST. The relay F currents (a), the relay A phase R (b) and S (c) voltages, the relay A currents in the phase R (d), S (e) and T (f). (1) - the fault inception, (2) - the by-passing of the phase R MOV of the ST, (3) - the by-passing of the phase S MOVs in the lines L1 and L2.



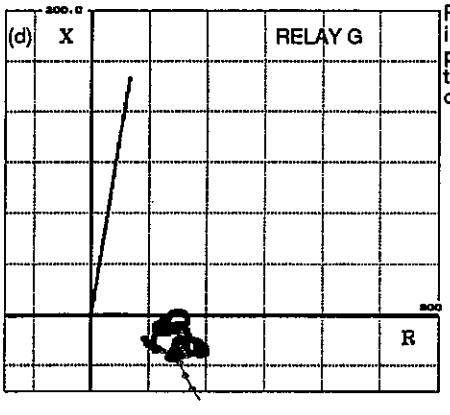


Fig.8. Short-circuit in the ST. The impedance trajectories of the chosen relays.

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