Enhanced Modeling of the Fortaleza SVC Incorporating a PLL-based Firing System Validated Against Laboratory Tests

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Abstract - **This paper describes a detailed modeling of the Fortaleza SVC, which is located at north area of CHESF's power system in Brazil. The purpose of this modeling is to represent an actual SVC to be considered in operating and engineering studies from electromagnetic point of view. The SVC control system is described in detail incorporating a special feature that allows thyristor equidistant fire pulses by means of a PLL-based firing system. It is also presented the laboratory tests, which made it possible to model the PLL chip used in the Fortaleza SVC. Some additional features of the Fortaleza SVC are also shown. Finally an assessment of the Fortaleza SVC response to power system disturbances is made under the PLL-based firing system point of view.**

Keywords: Modeling, Static Var Compensator, Phase Locked Loop, Equidistant Firing Pulses, EMTP.

I. INTRODUCTION

The time domain simulation is one of the most important tools for power system transient analysis. The modeling of FACTS devices, in particular SVCs, in powerful programs such as ATP-EMTP makes it possible to carry out power system simulations, which were previously done in transient network analyzers (TNA) only. These TNA simulations demand both a laborious and costly representation of the SVCs, which sometimes lead us to represent the SVC controls as a replica of the actual ones. Therefore, the electric utilities gain an additional flexibility for simulating SVCs in both power systems and equipment studies.

The Fortaleza SVC modeling for the ATP-EMTP program was developed using a detailed representation, taking into account the actual voltage regulator electronic circuitry. The block diagrams and transfer functions were determined by a careful and functional analysis of the actual electronic circuitry. The PLL-based firing system model was developed through some specific tests in laboratory with the SVC voltage regulator replica.

II. FORTALEZA SVC CONFIGURATION AND ATP-EMTP MODELING

In terms of modeling the Fortaleza SVC can be divided into three parts [1], as shown in Fig. 1: power circuit; control system; and synchronization/firing systems.

A. Power Circuit

The Fortaleza SVC comprises two sections, namely Y and Δ ones. Each section in turn consists of both a fixed capacitor bank (FCB) and a thyristor controlled reactor (TCR), which together with the step-down transformer (230/26/26 kV- 200/100/100 MVA) form a twelve-pulse arrangement. Note that this scheme can also be operated as a six-pulse arrangement when one of the sections is lost as shown in Fig. 1 (left-hand side). The power circuit still comprises a thyristor valve and a surge capacitor that are located at low voltage side. In twelve-pulse operation, the Fortaleza SVC is able to generate/absorb continuously from 200 Mvar capacitive to 140 Mvar inductive within a voltage range of 230 kV ± 5%.

The SVC power circuit was modeled by using regular, built-in ATP-EMTP models. It is worth mentioning that the thyristor valves were represented in a simple way through a small resistance in series with a type-11 switch, controlled by TACS (transient analysis of control systems) variables, and an equivalent snubber circuit per each branch of the TCR.

B. Control System

The control system is made up of the followings parts: measurement and filtering; formation of error signal; basic control loop; fast control loop; formation of the controller voltage (susceptance order); and working point. In addition to this, some features were added in order to meet power system transient requirements.

1) Measurement and Filtering: in order to obtain the measured system voltage, PTs and CTs are used on the high voltage side in such a way as to form for all phases the following signals: $V_{ab} + k\ I_c$; $V_{bc} + k\ I_a$; $V_{ca} + k\ I_b$ (where k is the slope). These signals are rectified, summed, and smoothed in order to form the measured voltage (V_m), which is an image of the voltage on high voltage side. Then V_m is compared with a set-point (Vref-reference voltage) generating an error signal. This error signal pass through a notch filter (120 Hz), and then it is fed into the regulator control loops. Fig. 2 shows a description of this process.

2) Control System: the control system consists of two control loops, namely: basic control loop (BCL), and fast control loop (FCL), as shown in Fig. 2.

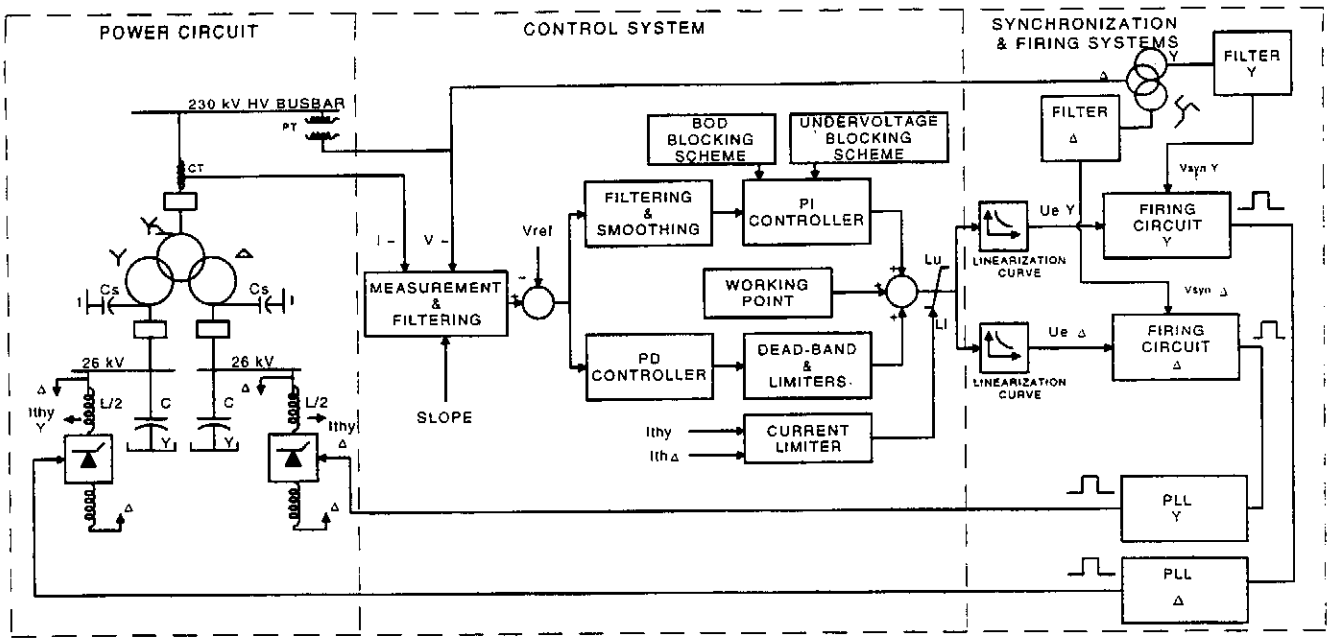

Fig. 1. Block diagram of the Fortaleza SVC modeling

The BCL acts as a continuous regulator being the main controller. Its control strategy is based on a proportional-integral (PI) regulator with dynamic limiters. The proportional gain (Kp) and the time integrating constant (Tn) are set in order to optimize the SVC response for several power system operating conditions. The PI regulator is of fundamental importance to the control system under small or major disturbances as well as in the steady-state, where its integral part brings the input error back to zero.

The FCL complements the BCL with a predictive strategy that becomes useful for large disturbances, where a very fast SVC response is required. Then the FCL is fitted with a dead-band, and both a capacitive and an inductive limiters.

The controller voltage (Uc) is thus obtained from the sum BLC+FCL, which represents a signal proportional to the SVC susceptance. A dc voltage is still added to the controller voltage in such a way as to produce the zero Mvar operating point, in case of a PI regulator blocking action. This dc voltage is called the working point (WP) and it is was set to zero, which corresponds to a firing angle of 119°.

3) Current Limiter (CL): this circuit allows to limit the TCR's overload in accordance with a pre-set capability curve by decreasing the SVC inductive range. A comparison between the two sections (Y and Δ) is made and then a maximum rms current is determined. This TCR current is compared with the pre-set overload curve (current x time). The current limiter resulting action is to limit the inductive range of the Fortaleza SVC up to 113°.

4) Undervoltage Blocking Scheme (UBS): the occurrence of faults in the transmission system causes voltage sags. In this condition the control system takes the SVC to a very capacitive operating point, which may cause severe overvoltage when the fault is cleared. This condition may be aggravated if a load rejection occurs following the fault. In order to avoid this undesired behavior, the UBS blocks the PI regulator 10 ms after detecting an undervoltage below a pickup value, and deblocks it 10 ms after the system voltage reaches a dropout value. In terms of modeling the PI blocking is done by closing its dynamic limits to zero.

Note that this UBS is of great importance for power systems with low short circuit ratio (Ssc/Qsvc), which is exactly the case of the CHESF's north area.

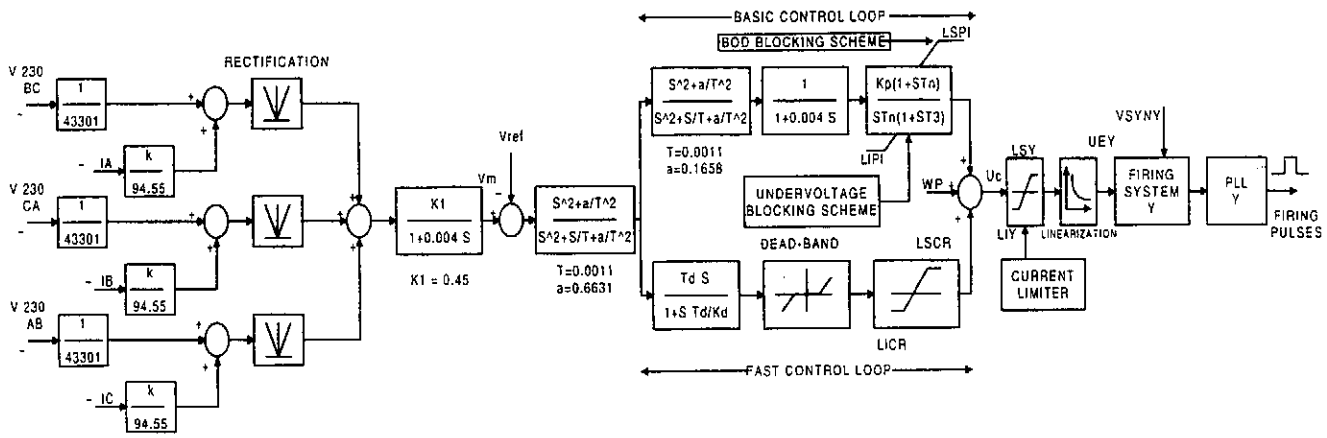

Fig. 2. Simplified block diagram of the control system

5) BOD Blocking Scheme (BBS): TNA simulations have shown that some operating conditions, e.g. faults at 69 kV Fortaleza busbar with a subsequent full load rejection, may give rise to severe overvoltages [2]. These overvoltages may cause thryristor protective firing (BOD), which in turn could activate the CL circuit. This may result a dynamic interaction BBS/CL sustained over the time that would cause SVC tripout. To avoid this undesired behavior, the BBS initializes the PI regulator at an adjustable inductive value (115°) for 10 ms after the BOD occurrence. After this time, the PI regulator is released to normal operation from that point of operation. In terms of modeling the BBS was represented in the following way: if the thyristor valve voltage exceeds 64 kVpeak, the PI regulator is initialized at 115° (Uc=-0,36 V) during 10 ms. In simulations where protective firing is likely to occur, the CL and BBS must properly be represented.

C. Synchronization and Firing Systems

The synchronization voltages are obtained from the 230 kV busbar voltages through both a PT 230 kV/115V and a synchronization transformer, which ensure that these voltages are in phase with the thyristor valve voltages. Fig. 1 shows this measurement scheme.

The relationship between the TCR fundamental current and the firing angle is non-linear. The linearization curve existing in the actual equipment was electronically approximated by 5 straight segments. In terms of ATP modeling this was accomplished by means of a 56-TACS device (point-by -point user-defined non-linearity).

The firing system initially modeled uses the IFP (individual fire pulses) scheme, i.e. firing pulses generated by zero-crossing techniques, as shown in Fig. 3. This firing system based on the IFP, although being easy to model, presents in the actual equipment a poor firing accuracy (maximum ±2°). This maximum firing angle asymmetry can be improved to 0.2° by means of a supplementary firing logic called equally spaced firing system (PLL).

The modeling of individual firing pulses system is based on ramp generators (integrators), which are reset at each new synchronization voltage zero. On the contrary, the PLL modeling is a quite difficult task, since all its functions are confined into a single chip - CD 4046 [3]. Moreover, the CD 4046 catalog does not contain sufficient information for a correct modeling of its dynamics. As a consequence of this difficulty it was necessary to perform investigations into the literature on PLLs and laboratory tests in the existing replica of the Fortaleza SVC voltage regulator .

The main concern on the PLL modeling was the correct representation of its static and dynamic characteristics. Fig. 3 shows, in a schematic/TACS block diagram, the firing system for the branch 'ab', section Y. In this diagram, the PLL is represented as a single block (SVCOY). The firing pulses of all phases, which are originated from the zero-crossing scheme, are summed in an OR gate (superimposed pulses), generating thus a pulse train with a frequency of 360 Hz. This pulse train is 110μs-delayed, i.e. 2.4° of 60 Hz, and then it is sent to the PLL. The PLL 4046 chip is an edge-controlled digital memory network [5], capable of maintaining a zero degree shift between input and output signals. In fact, the PLL modeled is a closed loop control system whose main objective is to generate an output pulse train with both the same frequency and in phase with the input one. Therefore, it is possible to generate equally spaced pulses with a high precision, minimizing thus both the dc current and even harmonics generated by the TCR in non-ideal condition, i.e. under firing angle asymmetry.

In terms of modeling the PLL can be divided into three parts, as follows: phase comparator; loop filter; and voltage controlled oscillator. This can be seen in Fig. 4.

1) Phase Comparator (PC): this detector works based on a positive edge transition logic in which its output can be as follows: 1 state; 0 state; and 'tri-state' (a high

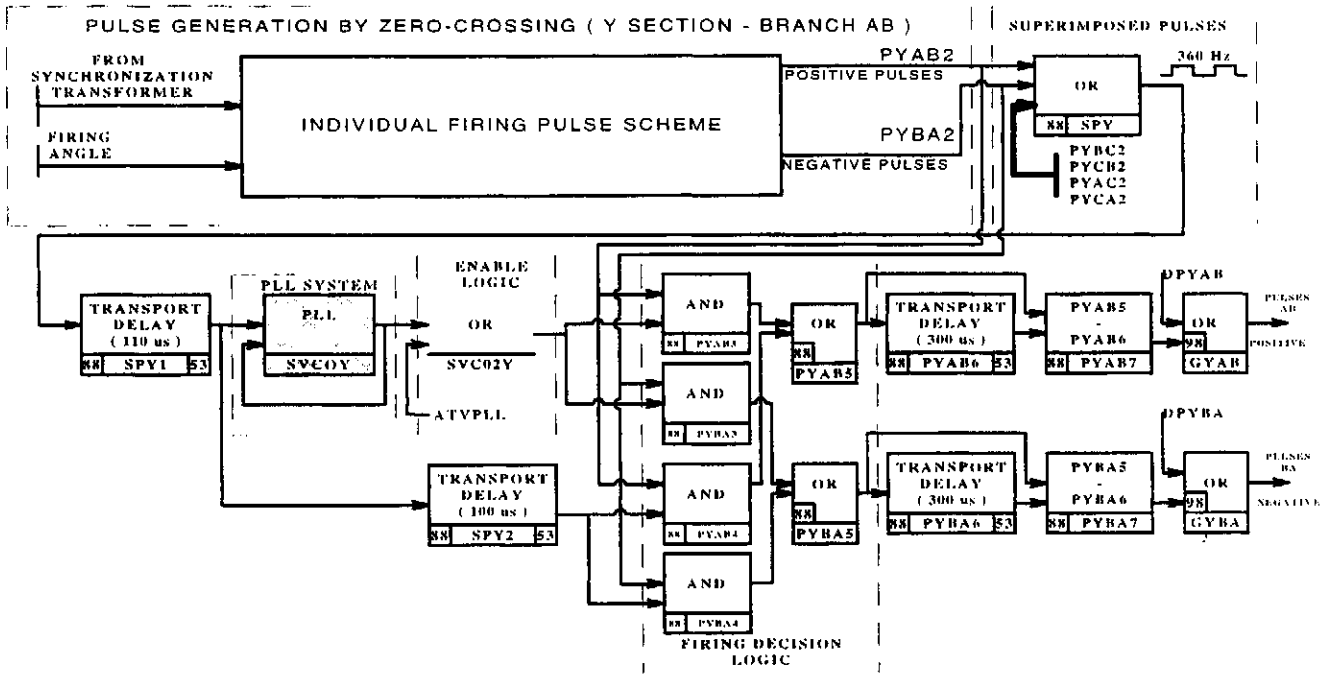

Fig. 3. Simplified TACS block diagram of the firing system - section Y - branch AB

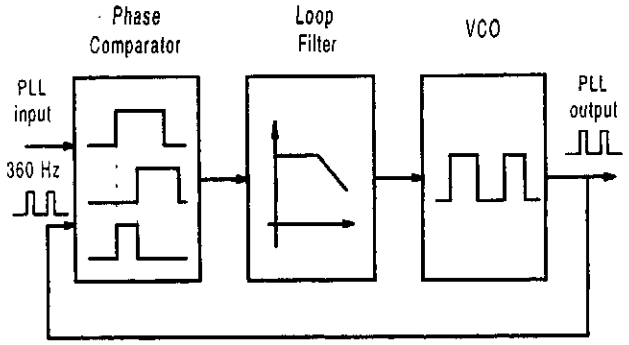

Fig. 4. PLL block diagram

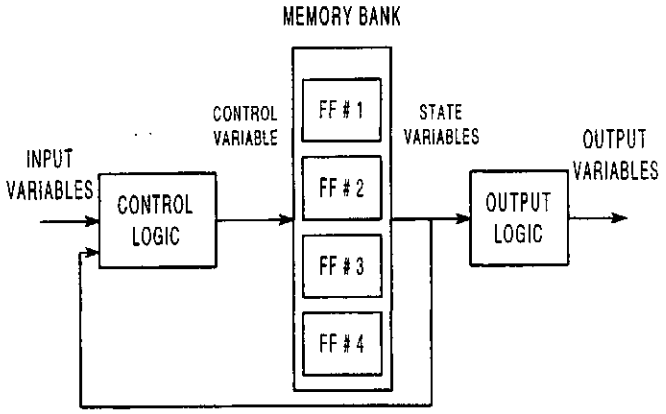

Fig. 6. Moore machine diagram

impedance state), as the comparison signal is respectively delayed, advanced or in phase with the input signal, as shown in Fig. 5. In terms of modeling this phase comparator can be represented by a kind of sequential circuit called Moore machine [5] that has its output variables independent of the input ones; changing, however, its output variables only when the state of the sequential system changes following a pulse input [5]. The Moore machine was designed from the state diagram II found in [3]. Fig. 6 shows this modeling that is divided into three parts: control logic; memory bank; and output logic. As a consequence of the TACS being a tool for modeling basically analog systems, the modeling of this phase comparator has been shown to be a complex and laborious matter. The control logic was represented by a set of eight Boolean equations, whereas the memories were represented by a bank of four R-S flip-flops. Then a model for representing the R-S flip-flop was developed in TACS. The output logic comprises two Boolean equations.

2) Loop Filter (LF): the loop filter consists of an RC circuit, as shown in Fig. 7. Its input (Vi) is the phase comparator output. Therefore, the loop filter input can be as follows: +15 V (1 state); 0 V (0 state), and tri-state. Then the loop filter behaves as a sample & hold device (when in tri-state) and as a proportional-integral controller in other states. The TACS block diagram of the loop filter can be seen in Fig. 8. It is important to note that the loop filter adjustment (values of R7, R8, and C5) practically defines the PLL's dynamics, i.e. the PLL's time response.

3) Voltage Controlled Oscillator (VCO): the VCO is a frequency generator with a high linearity that is controlled by a dc input voltage. This input voltage is the loop filter output, and it is worth 6.9 V for 360 Hz (laboratory measurement). Basically the VCO input is an average voltage, which takes into account the integral of the phase errors between the VCO generated pulses and those generated by zero-crossing scheme. Therefore, the VCO is continuously correcting the pulse train frequency with a view to minimizing the firing angle asymmetry.

The CD 4046 catalog presents the VCO static characteristics, i.e. curves 'voltage versus frequency', but nothing is found regarding its dynamic characteristic. In order to represent properly its dynamic, it was necessary to perform some laboratory tests and a more detailed investigation into different types of VCOs. As a consequence of the difficulty in obtaining a frequency response of the VCO, it was applied several steps to the VCO input. From a detailed analysis of these step responses, it was possible to build and validate a VCO model accurate enough for representing it dynamically. Fig. 9 shows a block diagram of the VCO.

4) Firing Decision Logic (FDL): the PLL is quite useful for the steady-state, where there are neither sudden phase alterations nor large unbalances. As a consequence of PLL slowness, in some transient conditions the thyristor firing should be accomplished by means of the IFP scheme. The firing decision logic verifies whether the PLL pulse train is within a interval -2.4° to +2.4° with respect to the pulse train generated by the IFP scheme. In case affirmative, the PLL will fire the thyristors. Nevertheless, in case of the PLL pulse train is outside of the ±2.4° interval, the firing decision logic enables the IFP scheme to fire the thyristors. In this case a severe disturbance is likely to have occurred.

5) Validation of the PLL Modeling for the ATP-EMTP Program: in order to validate the PLL model, it was applied a frequency step of 146 Hz (from 360 Hz to 506 Hz) to its input. This laboratory test was carried out by using an auxiliary VCO, where a 5V-step applied to its input yields a variation of 146 Hz in its output. The loop filter output voltage was chosen as a variable for comparison between values measured in laboratory tests and those simulated with ATP-EMTP model. The loop

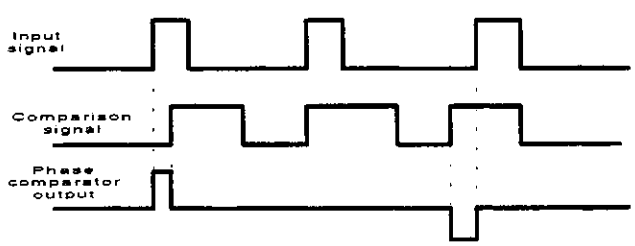

Fig. 5. Phase comparator logic

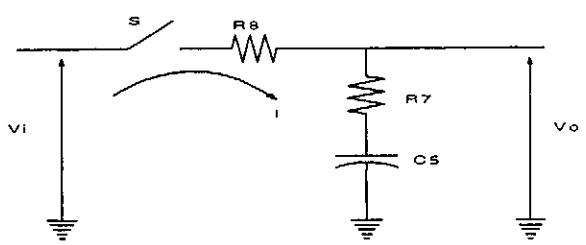

Fig. 7. Equivalent circuit of the loop filter

filter voltage was used due to its important role played in the dynamics of the PLL-based firing system. As can be seen from Fig. 10, both step responses present overdamped behavior with a settling time around 500 ms. In order to make a qualitative comparison, it was measured through a digital oscilloscope the proportional gain of the loop filter. The measured value is worth 0.8160 V/V, whereas the theoretical value is equal to 0.8246 V/V, R7/(R7+R8) in Fig. 8,which was used in the ATP simulations. Therefore, it can be concluded that the PLL modeling was both qualitatively and quantitatively validated.

III. CONSIDERATIONS ON THE FORTALEZA SVC MODELING FOR THE ATP-EMTP PROGRAM

A. SVC Model Initialization

The SVC model initialization is well described in [1], but it consists of mainly a introduction of a dummy voltage source on 26 kV busbar in both sections of the SVC by about 30 ms. Moreover the control system should be blocked, and the SVC remains operating at the working point (zero Mvar) during approximately 60 ms. These transients are quite long due to the PLL slowness . With the objective of shortening the initialization transient of the PLL integrated into the rest of the model, a decrease of the time integrating constant of the loop filter by a factor of ten for about 60 ms seems to be quite efficient for the power system studied.

B. Choice of the Time-Step

The SVC model for the ATP-EMTP program incorporating a PLL demands very small time-steps. This is primarily a consequence of the PLL firing accuracy of ± 0.2° (9.26 µs), i.e. to reproduce PLL's dynamics it is advisable to use a time-step less than 5 µs, being recommended 2 µs. Of course, this is not a constraint regarding numerical oscillations; much on the contrary this is a physical constraint, since ATP-EMTP is not able to reproduce the dynamics of a system with a time-step smaller than its most important time constant. Moreover the PLL-based firing system generates pulse train with a high precision and then for a power frequency of 60 Hz the PLL train pulse frequency is 360 Hz, i.e. a period of

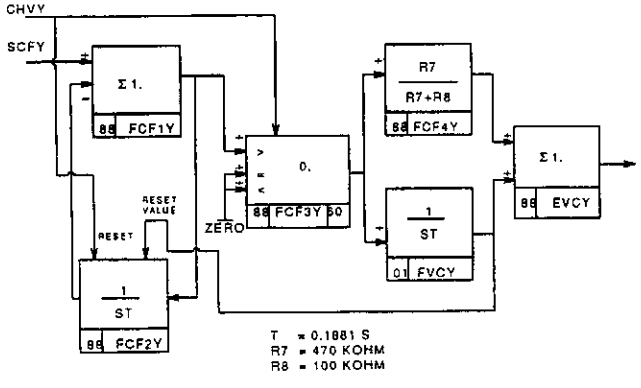

Fig. 8. TACS block diagram of the loop filter

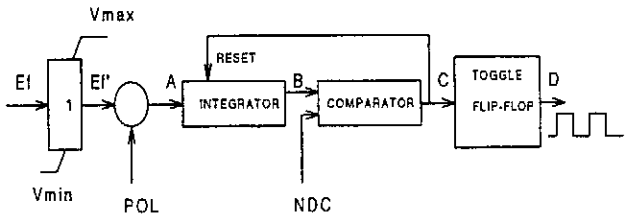

Fig. 9. Block diagram of the VCO

2,777.8 µs. Therefore, for a time-step of 10 µs the PLL would generate pulse train frequencies between 361.01 Hz and 359.7 Hz, which correspond to a period of 2,770 µs and 2,780 µs (multiples of 10 µs) respectively. Therefore, a time-step quite small improves effectively both the VCO and phase comparator accuracy.

IV. SVC MODEL RESPONSE TO DISTURBANCES

The comparison between the SVC model simulations (using the IFP scheme) with TNA simulations has already been made and can be found in [1]. These results show a good agreement; validating, therefore, the digital model developed using the IFP scheme. The PLL is a symmetrization module for the steady-state, with a control action very slow by conception. Nonetheless, as designed for the Fortaleza SVC, its dynamics interferes in the transient behavior, e.g. sudden voltage variations, faults, and voltage unbalances.

The power system studied can be seen in Fig. 11 in a simplified one-line diagram. The network configuration was chosen to develop a very low short-circuit capacity. The modeling of this power system was accomplished using built-in ATP-EMTP models, such as: transposed transmission lines, network equivalent consisting of voltage (source 14) behind positive and negative sequence impedances, and load and reactors represented as constant impedance.

A. Application of -10% Voltage Step to the Voltage Regulator Set-point (Vref)

A -10% voltage step was applied to the voltage regulator set-point (reference voltage) at 80 ms. As a consequence of having a slow dynamics, the PLL frequency starts changing

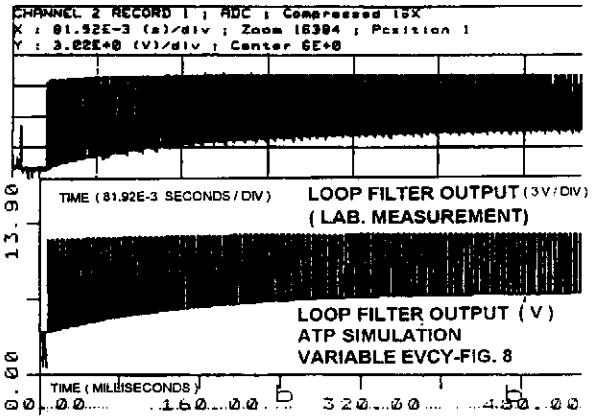

Fig. 10. Validation of the PLL model

effectively from 90 ms and tends to accommodate after 180 ms. Fig. 12 shows the input/output of the PI controller (voltage regulator) under these circumstances, i.e. with and without the PLL.

As can be seen, in the simulation with PLL, the control response (PI output) is slightly underdamped. It accommodates around 210 ms, i.e. a settling time around 130 ms. The simulation using the IFP scheme (without PLL) presents a settling time around 85 ms. In terms of control system, it can be concluded that the PLL-based firing system introduces a delay that can be translated into a less damped response.

B. Application of a Single-phase-to-ground Fault at 230 kV busbar

The performance analysis of the equally spaced firing system (PLL), under solid single-phase fault nearby Fortaleza SVC, has concluded that the PLL, used in the Fortaleza SVC, gets a pulse train of 60 Hz rather than 360 Hz, as usually expected. This is a consequence of the coincidence of the distinct phase's zero-crossings under single-phase-to-ground faults. Therefore, this PLL frequency is significantly reduced depending on the fault duration. Fig. 13 shows the loop filter output that is a dc average voltage modulated by pulses, which are proportional to PLL phase errors (detected by the phase comparator). This dc voltage is proportional to the VCO frequency and represents the PLL's dynamics. After the fault removal, note that the re-synchronization time is around 420 ms.

C. PLL Performance Submitted to a Negative-sequence Voltage Unbalance

In order to assess the performance of the equally spaced firing system under voltage unbalances, it was injected into the network 2% of negative-sequence at Bom Nome substation busbar, roughly 500 km away from Fortaleza substation busbar. Note that even in the presence of this unbalance the PLL is able to maintain its accuracy range (± 0.2°). In addition the PLL is also able to decrease the negative-phase sequence unbalance at Fortaleza busbar from 2.2% (without PLL) to 1.4% (with PLL).

V. CONCLUSIONS

The development of a detailed SVC model for the ATP-EMTP program makes it possible for electric utilities to carry out planning, operating, and equipment studies, which were previously done through TNA only.

The PLL modeling of the Fortaleza SVC has been shown to be a difficult task, demanding laboratory tests and the synthesis of digital sequential circuits using TACS.

The utilization of PLL-based firing system incorporates an additional retard, which means a less damped response to small disturbances. As designed for the Fortaleza SVC, the PLL is sensitive to frequency drops when under faults that causes zero-crossing coincidences. This in turn causes a retard in the re-synchronization of the SVC into the network.

Even though a 2% negative-sequence voltage being considered, the PLL is able to maintain its accuracy and reduce this unbalance.

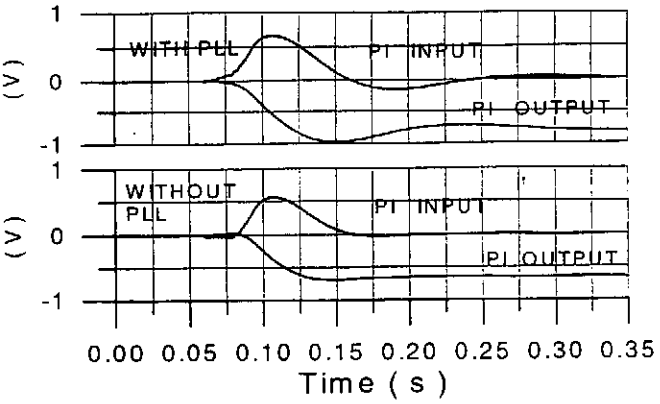

Fig. 12. SVC response to a -10% voltage step

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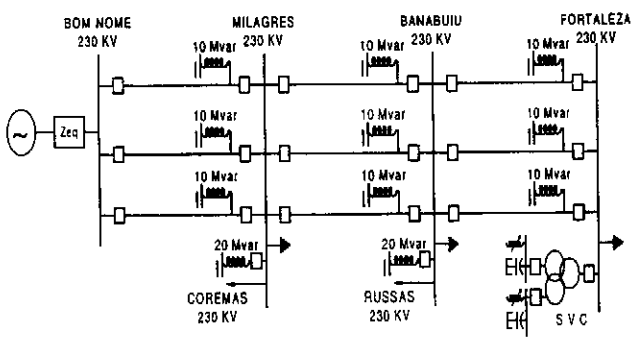

Fig. 11: Simplified one-line diagram of CHESF's north area equivalent

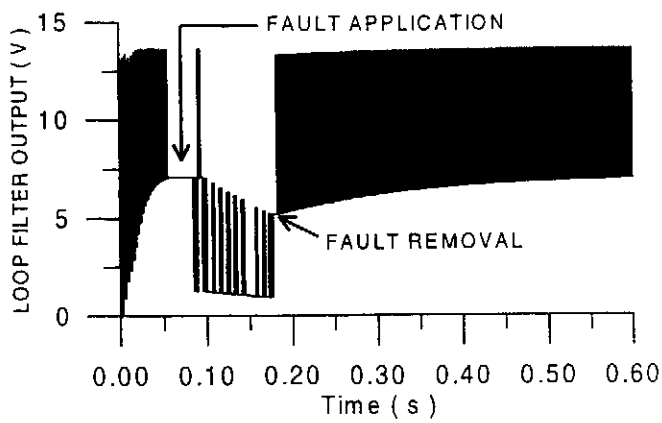

Fig. 13. PLL performance under single-phase fault at 230 kV busbar