Real-time Power System Simulator on a PC Cluster

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Abstract- **The authors have prototyped a real-time simulator of power systems using a PC cluster. PC clusters are parallel processing systems which consist of commodity PCs and high speed networks. Advantages of the simulator on a PC cluster are 1) low cost, 2) upgradability and 3) scalability. When this paper is submitted, the real-time simulator using a cluster of 8 PCs can handle 7 equivalent voltage sources, 7 transformers, 7 three phase transmission lines, and 1 interface between analog and digital simulation in a 50 microsecond time step. In this paper, the authors introduce the outline of the real-time simulator on the PC cluster.**

Keywords: EMTP, Real-time, Simulation, PC, Cluster

I INTRODUCTION

Thanks to the ceaseless progress of computer technology, several computing architectures are now being used to realize real-time simulators of power systems[1, 2, 3, 4]. However, some of those simulators are relatively expensive and some others are not easy to upgrade and extend. The authors have prototyped a real-time simulator of power systems using a PC cluster.

The PC cluster is a parallel processing system which consists of PCs and a high speed network. Advantages of the simulator on a PC cluster are

1) low cost,
2) upgradability and
3) scalability.

1) Because the PC market is very competitive, the cost of a PC is very low compared with its performance. Therefore simulators on PC clusters can be very cost-effective.

2) By using a standard C++ for programming and a standard operating system, the authors have developed a simulator which can enjoy the fast upgrade of PC technology. Appearance of faster PCs can mean faster simulators.

3) The PC cluster introduced uses a very fast network called Myrinet[5] and a fast communication library called PM[6] which achieves 15 microsecond round trip time.

Therefore, the simulator on a PC cluster can be extended with little communication overhead if users need to simulate a larger power system.

In this paper, the authors introduce the outline of the real-time simulator on a PC cluster as an ongoing project.

In section II, the the hardware of the PC cluster is discussed. In section III, the software of the simulator is discussed. In section IV, some examples of simulation results are shown. In section V, the speed of the simulator is described. Finally, in the section VI, this paper is summarized and the future plan of this project is explained.

II HARDWARE

The PC cluster that the authors introduce in this paper consists of 8 PCs as computing nodes and a network which is called Myrinet. Every PC in the cluster has a 333MHz Pentium II Processor, 128MB Memory, a 6.0GB HD Drive, a Myrinet Card and an Ethernet card. One PC in the cluster has AD and DA cards to be connected to analog circuits. In Table 1, the main specification of the PC cluster is shown.

Table 1: PC Cluster Specification

Nodes	8
CPU	Pentium II 333MHz, 512KB cache
Memory	128MB/node SDRAM
HDD	6GB/node
Network	Myrinet 1.28Gbps Bi-directional 100BASE-T 100Mbps
OS	Linux 2.0.33

Fig. 1 shows the appearance of the PC cluster and Fig. 2 shows the outline of the simulation system including an analog circuit and an interface with it. As shown in Fig. 1, the 8 PCs are mounted in a rack to reduce the physical volume but each module is equivalent to a commodity PC/AT machine.

As this paper is submitted, this cluster of 8 PCs is the maximum size that has been verified for real-time simulation. However, a cluster of 128 PCs is now working at the Real World Computer Partnership (RWCP) using the same network. Large scale systems will be tested for real-time simulation in the near future.

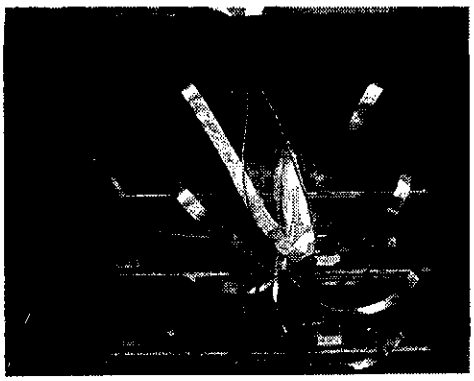

Figure 1: Appearance of PC Cluster

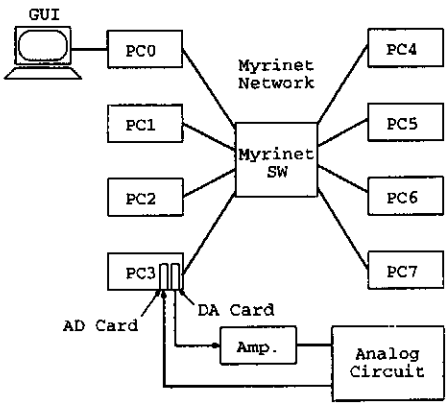

Figure 2: PC Cluster node configuration

III SOFTWARE

In the simulator described in this paper, all the PCs are working on PC-UNIX, Linux. The UNIX functions are being used to compile the simulation software, share the input files, start the simulation program and run an input file editor and a runtime GUI interface.

The simulation program has been written in C++, and compiled independently from power systems that will be simulated. Power system data(topology and parameters of elements) are given as an input file to the program. The user-level communication facility called PM[7] is used in our real-time power simulator. PM is a communication facility on Myricom Myrinet giga-bit network, and consists of user level library, device driver and firmware on the Myrinet interface card. As the result of eliminating extra message copy overhead and controlling Myrinet hardware by user program directly, PM achieves 113.5 MBytes/sec bandwidth and 15 microsecond round trip time.

The same executable code can be executed in real-time mode or non real-time mode by being given the different options when it is started. The source code of the simulation program is completely portable so that it can be compiled and executed on the other UNIX systems if real-time, parallel execution and an analog interface are not required.

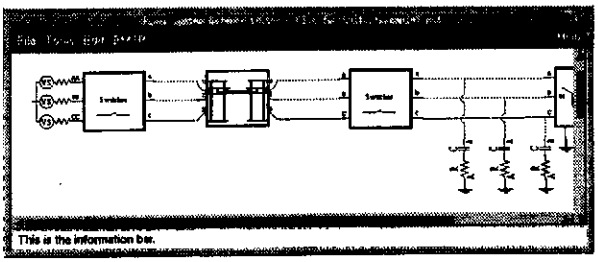

Figure 3: Editor GUI Window

When the simulation is done in real-time mode, one of the PCs in the cluster is dedicated to handle inputting and outputting of data for simulation. The remaining PCs are executing the simulation of a power system in real-time by prohibiting the execution of the other processes. In this paper we call the PC which handles inputting and outputting of data, the host PC and the PC which executes the simulation as the simulation PC. During the real-time simulation, the simulation PC can not communicate with the other PCs through the Ethernet, therefore the results from simulations and operations from the user are sent through the Myrinet network.

The algorithm for the proposed simulator is equivalent to the conventional EMTP's algorithm[8], although, at the present stage of the project, only few models have been implemented. Those models which are available now include Rs, Ls, Cs, single or three phase transformers, current or voltage sources, non frequency dependent transmission lines, circuit breakers, thyristor valves, synchronous machines.

The tool for editing power systems and making input files for the simulator has been prototyped. By using this editing tool, a user can define the power system on a graphical user interface. Fig. 3 shows an example window of the editing tool.

A runtime graphical user interface has been prototyped as well. Fig. 4 shows an example window of the runtime GUI. When a user runs the simulator, he/she can check the simulation result through the runtime GUI and change the state of switches in the power system.

IV SIMULATION RESULT

At the present stage, the simulation result of a large or middle scale power system has not been verified in detail. Simulations of large power systems have just been executed and the results show that they do not conflict with common sense.

However, at the previous stages of the project,

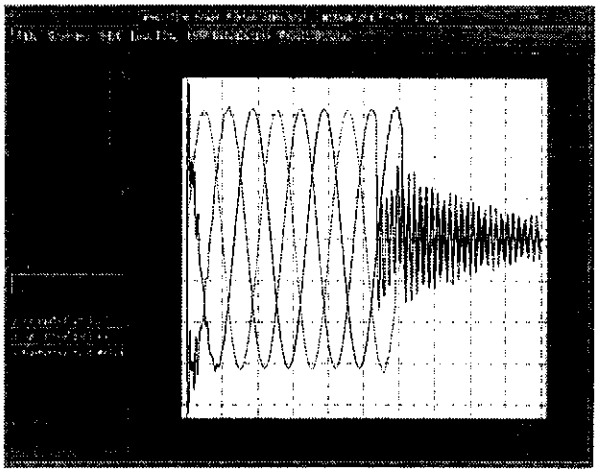

Figure 4: Runtime GUI Window

models of small elements such as Ls, Cs, Rs, transformers and non frequency dependent transmission lines were verified by comparison with the EMTP or analytical results. A PC cluster of 2 PCs (300MHz Pentium II) was built and the results from full digital simulation and hybrid (analog and digital) simulation were compared. Fig. 5 shows an example circuit for the test. In hybrid simulation (I), the resistive load which is enclosed by the dotted line was modeled by a physical analog circuit. Commodity AD and DA cards were inserted on an ISA bus of a PC in the cluster and realized an interface between digital and analog simulation. On the other hand, in the simulation (II), the whole circuit was modeled on the PCs. Fig. 6 and Fig. 7 show the current through the circuit breakers in the simulation (I) and (II), respectively. As the graphs show, the results of both cases coincide very well.

Additionally, in order to demonstrate the accuracy of the newly developed simulation program, in the simulation (III), the same simulation case was done by the EMTP, and its result was also compared with those of (I) and (II). In Fig. 8 shows the result from the EMTP. This result also coincides with the others very well.

Now the PC Cluster has been upgraded to one which has 8 PCs (330MHz Pentium II). A power sys-

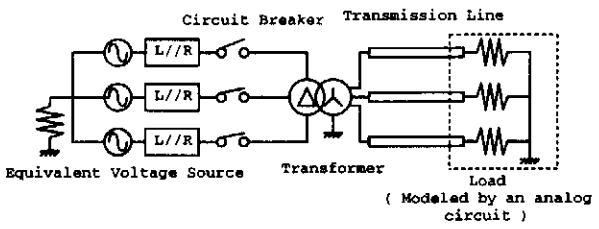

Figure 5: Example circuit

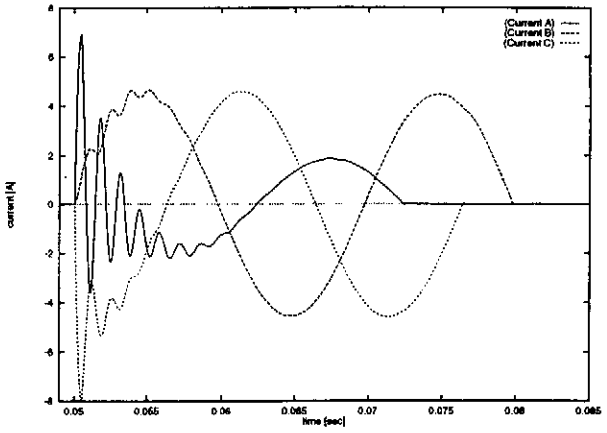

Figure 6: Current through the switch (Simulation(I), with analog interface on the PC Cluster)

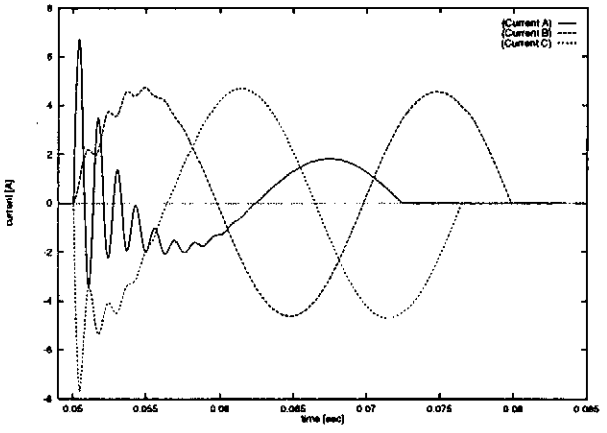

Figure 7: Current through the switch (Simulation(II), by full digital on the PC Cluster)

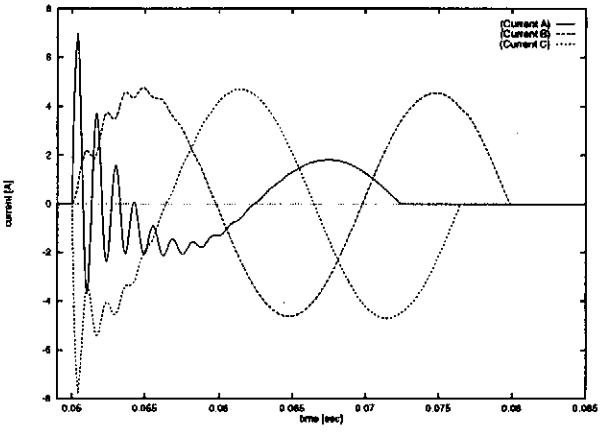

Figure 8: Current through the switch (Simulation(II), by the EMTP)

tem which can be simulated by the present cluster is shown in Fig. 9. The figure is a single phase diagram but the power system is modeled and simulated

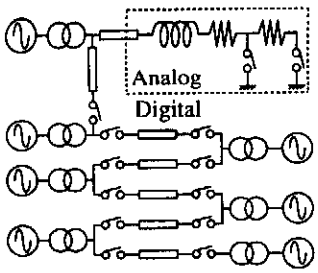

Figure 9: Simulation Case

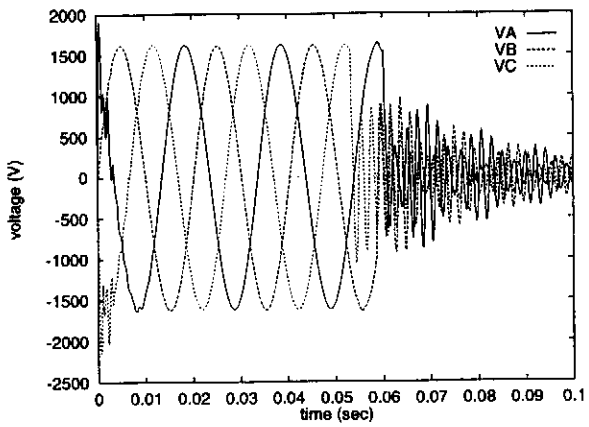

Figure 10: Voltage of the switch terminal(full digital)

as three phase. The system has 7 equivalent voltage sources, 7 transmission lines, 7 three phase transformers, 33 circuit breakers, some small elements and an analog/digital interface. The part enclosed by the dotted line is modeled by a physical analog circuit. Through commodity AD and DA converter cards on a ISA bus, the digital and analog simulations are connected. Although the simulation result is not verified in detail, one of the examples is shown in Fig. 10. The figure shows the voltage of the terminals on circuit breakers. The comparison of the simulation result with the EMTP is ongoing.

The minimum simulation time step for the power system shown in Fig. 9 is about 49 microseconds if real-time is required. However most of the CPU time is consumed in handling the AD/DA interface in this case because slow ISA bus cards are used now. In future PCI based AD and DA will be installed. If the analog part of the simulation case shown in Fig. 9 is omitted, the minimum time step for real-time simulation 'is about 27 microseconds.

V SIMULATION SPEED

In this section, the performance of the PC cluster which can be related to the limits of real-time simulation, is discussed.

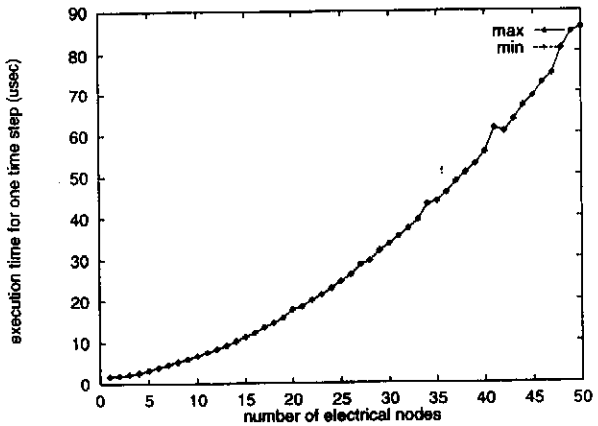

Figure 11: Simulation speed : number of electrical nodes

V.1 Number of electrical nodes in a substation / CPU speed

One of the most time-consuming calculations of power system simulation is solving linear equations. Even if the inversion or the LU factorization is done before the simulation loop, its calculation burden is proportional to the square of the number of electrical nodes. Therefore there is a limit to the number of electrical nodes in a substation.

To investigate this limit, power systems which consist only of electrical nodes and Rs are generated and simulated on one PC of the cluster. These power systems consist of only one substation and no parallel processing is used to measure the performance of one PC. Fig. 11 shows the CPU time elapsed for one time step of the simulation. The horizontal axis represents the number of electrical nodes. The elapsed CPU times of all the time steps during the simulation have been measured and it was found that there are small differences among the elapsed CPU times even in an execution of simulation. Therefore, the maximum and minimum elapsed times are shown in Fig. 11. In the figure, the difference is so small that it is impossible to determine.

From this figure it can be seen that one the performance of one PC is good enough to simulate about 35 electrical nodes of one substation in real-time when the time step is 50 microseconds. Additionally if we can use faster PCs, they are expected to be able to handle more nodes or smaller time steps in real-time.

V.2 Switching Devices / Cache miss

It is well known that fast computers of today depend on 'cache' for their marvelous performance. Cache works very well when a processor is using the same part of the memory repetitively but if the processor uses a part of the memory which has not been used previously, the cache miss occurs and the process

is slowed down. For real-time, every time step should be finished in the fixed time. That means that one cache miss during the millions of time steps destroys real-time.

For real-time power system simulation, it is conventional to calculate, process and keep all the possible admittance matrices before the simulation loop. That is because inversion or LU factorization of matrices requires much calculation and spoils the real-time performance.

However, the preceding calculation of the matrices increases the memory demand when the number of electrical nodes and switches in a substation increases. If the number of electrical nodes and switches in a substation are n and m respectively, the size of the admittance matrix is n^2 and the number of the possible matrices is 2^m. If the symmetricity is taken into account and the sparsity is not, M elements of real number data should be kept in the memory and may be used during the simulation, where M is given by

$$M = 2^{m-1}n(n-1). \quad (1)$$

M can be very large, especially if m is large or in other words the number of switches is large. When M is large, the memory area which keeps the precedingly processed matrices is large. Therefore, the change of the switching state in the simulation causes the change of the matrix and then the cache miss.

In order to investigate this difficulty on a PC, power systems which consist of electrical nodes, Rs and switches are generated and simulated on a PC. Fig. 12 shows the result. The vertical axis represents the elapsed CPU time for one time step and the horizontal axis represents the number of switches. The data are shown for when the numbers of electrical nodes are 20, 30, 40 and 50. (In the graph, the maximum and minimum elapsed CPU time is shown as in Fig. 11.) The reason that some data for the larger number of electrical nodes is lacking some sample points is that M is too big to allocate to the memory.

From Fig. 12, it is shown that when the number of switches in a substation becomes larger than some given number, the performance of real-time simulation deteriorates. The deterioration is worse when the number of electrical nodes is larger. This result shows that some techniques (for example, [9]) should be used for substations which have many electrical nodes and switching devices for real-time simulation on a PC.

V.3 Scalability / Communication overhead

In V.1 and V.2, the problems concerning one substation have been discussed. However, when a power system has several substations, those substations can be assigned to PCs on the cluster and the simulator can have scalability. In such a case, the communication overhead can be a problem. To check the communication overhead, power systems which have 1 to 8 substations are generated. In these power systems, each substation has electrical nodes and Rs. All the substations are connected by three phase transmission lines as shown in Fig. 13.

The same number of PCs have been used to simulate these power systems as that of substations. Here one substation has been assigned to one PC for a simple test. For the proposed simulator on the PC cluster, however, some number of substations can be assigned to one PC. As an example, one PC can simulate a whole power system of 8 substations if users don't need first simulation. On the other hand, the process for one substation can not be divided for several PCs so far.

Fig. 14 shows the CPU time elapsed for one time step of the simulation. The CPU time for one time step is different for each time step. In the graph, the maximum and minimum CPU time is shown.

The horizontal axis represents the number of substations. The data are shown for the cases where the numbers of the nodes in the substations are 20, 30, 40 and 50.

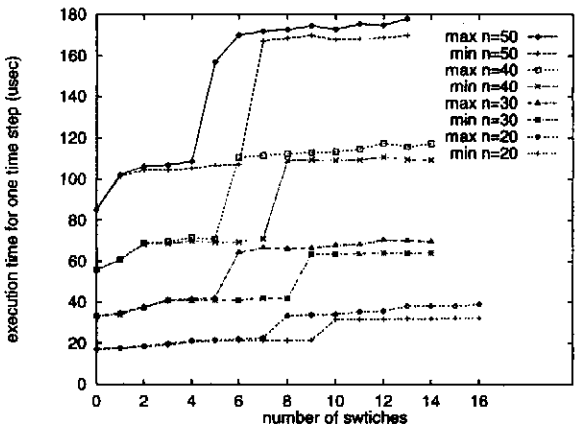

Figure 12: Simulation speed : number of switches

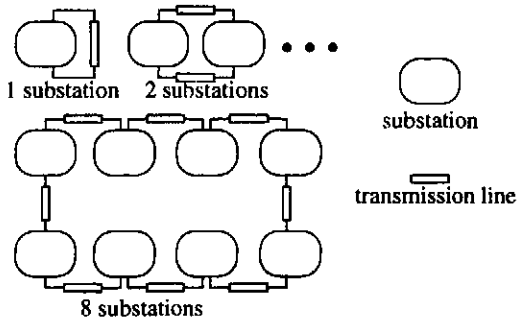

Figure 13: Array of substations

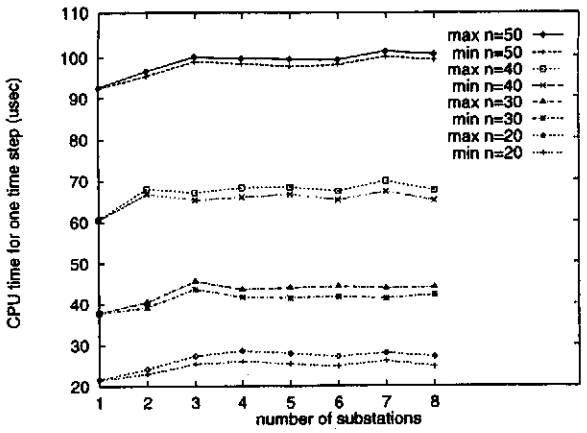

Figure 14: Simulation speed : number of substations

The graph shows very good scalability for up to 8 PCs in the cluster. From the graph, the communication overhead is less than 10 microseconds even when 2 to 8 PCs are working together.

VI CONCLUSION

In this paper, the prototyped real-time power system simulator on a PC cluster has been introduced. The outline of its hardware and software has been described. Additionally some simulation results and the performance of the simulator in terms of speed has been described as well.

The simulator on the PC cluster is

1) low cost,
2) upgradable and
3) scalable.

Now the real-time simulator on a cluster of 8 PCs can handle 7 equivalent voltage sources, 7 transformers, 7 three phase transmission lines and 1 interface between analog and digital simulation in a 50 microsecond time step.

The authors are expecting that larger PC cluster systems can also be used as real-time simulators and are going to test them. As discussed in subsection V.2 the problem related to cache has been found, therefore some countermeasures will be implemented. The authors will use newer and faster PCs as parts of the PC clusters and make the simulator faster.

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