Real – Time Simulator ARTEMAC for Enhanced Automated Interactive Testing of Digital Relays

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Abstract: **Real Time system simulation is an essential tool in establishing the performance of modern protection equipment. In case of digital simulators Siemens AG, in cooperation with the Technical University of Berlin, Institute of Electrical Power Engineering has developed the PC-based real time simulator Artemac for arbitrary protection devices. The system includes the capability of transient in-the-loop testing of modern protective relays. The first part of the paper describes the main features of the PC-based simulator system, including the closed loop testing approach. For relay testing an automated test procedure has been developed and implemented. The second part gives a comprehension of the test equipment. The test data are generated systematically or statistically in a variety of dynamic fault conditions. The test procedure is controlled by a diagnosis system, dependent on the selected strategy.**

Keywords: Artificial Intelligence, Automated Testing, DINEMO, Fault Detection, NETOMAC, Relay Testing, Real-Time-Simulation,.

I. INTRODUCTION

Interactive real-time testing of protective relays is a requirement for the testing of modern protective relays. Siemens AG in cooperation with the Technical University of Berlin developed the real time simulator Artemac for transient in the loop testing. This simulator system is in use in Berlin for manual and automated testing of Siemens protection devices, for quality control and development of digital protection devices. Using this simulator system, high-end testing on a PC-based low-cost system becomes possible. For generating the output values the simulation program NETOMAC is used which is running under real time conditions. The simulator software Artemac is able to run the testing of protection devices with a large extent automatically. For test optimization special testing strategies and fault detection strategies are implemented.

II. PC BASED SIMULATOR

Digital simulator testing can be used to evaluate the performance of digital relays under realistic conditions. In the last years, Technical University of Berlin, Institute of Electrical Power Engineering has developed a PC-based real time simulator for digital relays, special computers are not necessary. This system includes the capability of transient in-the-loop testing of modern protective relays. Fig. 1 shows the block diagram of the digital simulation system. The NETOMAC program (network torsion machine control) is used in order to determine the currents and voltages under real time conditions for transient testing of protection equipment [2].

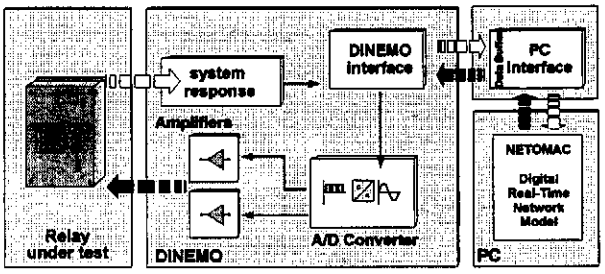

Fig. 1. Real Time Digital Network Model

DINEMO (digital network model) is a unit for real-time communication, which is able to carry out real time computed current and voltage signals [5]. The response of the real equipment, such as a tripping signal to open a breaker, has a feed back into the personal computer. In addition, because the simulation is running in real-time, the output contacts of the relay can be connected back to the NETOMAC circuit breaker models where the breakers can be controlled as in the real system. For realizing the communication between personal computer (16 Bit ISA-bus) and DINEMO (SCSI-bus), an I/O-card with integrated CPU has been developed. Voltage to current converters are used for adaptation of the signal level between D/A-converters and test equipment.

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III. CLOSED LOOP TESTING

In many situations the closed loop testing approach enhances efficiency in the conduct of the tests. Also, in other situations, closed loop testing is a requirement for properly determining the response of the equipment. In case of interaction, the sampling rate is a requirement for the quality of the output signals. The time needed for the simulation depends on the simulator and the complexity of the simulated network. Additionally, if both, simulation and communication, is done by the PC, most of the disposable time is used for the communication. Therefore it is useful, to separate simulation and communication.

Improving Simulation Performance

Realizing the closed loop testing approach, Technical University of Berlin developed an special interface card to connect the DINEMO and the personal computer. For that reason nearly 100% of the available time of the PC can be used for simulation. In this case a smaller time step for a better real time simulation becomes possible [1]. Fig. 2 shows the improving simulation performance using the i/o card. Besides, the number of signal channels has no more influence on the simulation time. Using this system, output rates below 250 µs are possible.

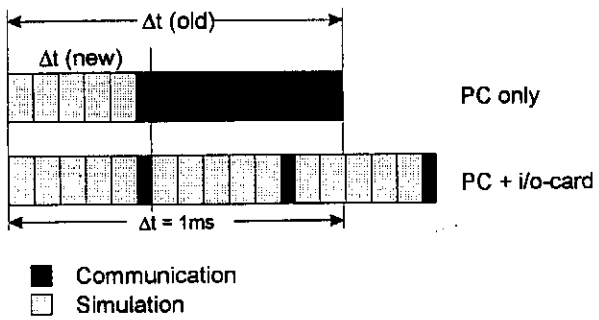

Fig. 2. Improving communication performance

The PC has to write out all data as fast as possible to gain more time for the simulation. As a logical consequence, there is an input and output buffer on the I/O-card between ISA-bus and the SCSI chip. All data to be sent from PC to DINEMO are written in a First-In-First-Out-register (FIFO). The time needed to transfer the data simulated from PC to the input buffer of the I/O card amounts a few µs per value. After this short time, the PC is no more longer blocked for the communication and the simulation of the fault continues. On the other side, all replying data received from DINEMO are written in an output register. After writing the data simulated in the FIFO input buffer of the I/O-card, the PC analyses the output register containing the actual status of up to 16 replying signals of the relays to be tested in the closed-loop.

Asynchronous Data Transfer

In case of designing and testing real equipment, digital dynamic power system simulation should reach or even be faster than in real-time. A mainly bottleneck is the occurrence of alterations of the nodal admittance matrix, e.g. due to a switching operation. Additional to the calculations, that are executed during a normal integration time step, a new preparation of the matrix is necessary. For that, discontinuous time-steps slow down the fastness of the simulation process. In case of closed-loop testing, which may dictate real-time conditions, the output rate has to adapt to the slowest simulation time-step.

Real circuit breakers always have a time lag between the tripping signal of a relay and connection or disconnection. The time lag ranges from 40ms to 60ms. This phenomena can be used to eliminate the influence of discontinuities [1].

Improving the performance of the closed loop testing approach, the buffers of the I/O-card are used, not only to separate simulation and communication. They are also used to buffer a number of pre-simulated output samples on the I/O-card before writing-out to the relay. When starting the interactive process, the first buffered sample is carried out to the relay in real-time and the action of the tripping response creates dynamic conditions on the simulated power system with a time-delay. This delay is dependent on the buffered rate of pre-simulated time steps.

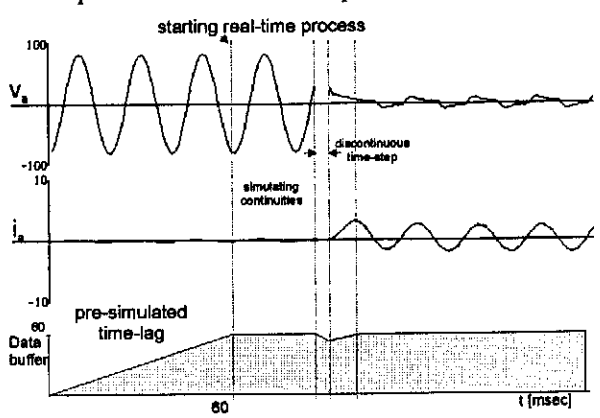

Fig. 3. Closed-loop testing approach

Fig. 3 shows the interactive testing process using the buffer approach. The pre-simulated time-interval is equal to the adjusted time lag of the

circuit breaker model. The following equation describes the numbers of discontinuities dependent on the adjusted time lag:

$$x_{DELAY} = \frac{t_{CB}}{t_{MAX} - t_{MIN}}$$

t_{MAX}	time step simulating discontinuities
t_{MIN}	time step simulating continuities
t_{CB}	time lag of the circuit breaker

In cases of simulating a continuity faster than real-time, the system is able to fill the buffer again. The whole point of the closed loop testing approach is that the buffer is decreasing simulating discontinuities and is increasing, simulating continuities. However, this movements have no influence on the adjusted time lag of the circuit breaker and the real-time condition. The system will lose the closed loop ability, if the buffer gets empty (too many discontinuities or continuous time-steps can not be simulated in real-time).

IV. AUTOMATED TESTING

Protective relays play an important role in today's complex power generation, transmission and distribution systems. Consequently, this process has given rise to the need for more broad-based dynamic automated testing.

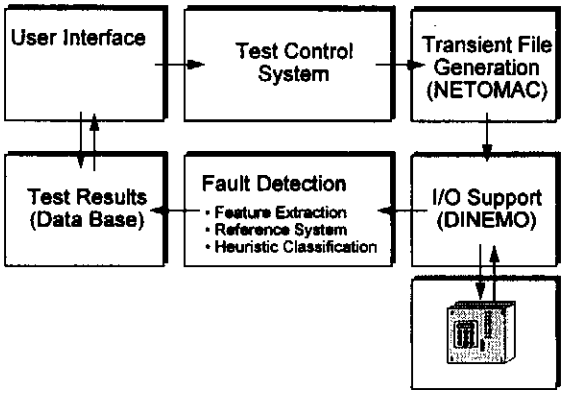

Fig. 4. Automated testing

Fig. 4 shows the automated testing approach. In order to meet the variety of requirements a modular simulator design may be needed.

The User Interface Module

The user interface module needs to support the following functions:

- Power system model selection unit
- Protection relay configuration.
- Test configuration
- Fault selection menu

Transient File Generation

The transient file generation takes advantage of the electromagnetic transient program NETOMAC, a product of Siemens AG. The model data are subdivided in static data and dynamic data. The dynamic data represent the several fault conditions which are used for fault detection and classification. Varying the conditions of the fault a large number of test cases are available. The cases selected are prepared and carried out automatically by the testing control unit dependent on the test case design.

Fault Detection Module

The fault detection module signals that a fault occurs. The fault detection system is separated in three units. Fig. 5 shows the basic steps in fault detection:

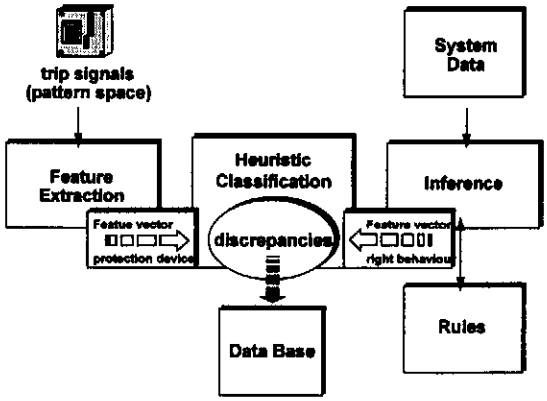

Fig. 5. Fault detection module

The first component is the feature extraction unit. The pattern map of the system response, like the tripping signals of a protection device are transformed into the feature space. Feature extraction always involves the destruction of some information about the original pattern. Therefore information which is specific only to an individual pattern but not general to the entire class is ignored or thrown away. The feature extraction bases on following rules:

- Activation and change of an analyzed signal
- Time of signal activation dependent on the fault conditions
- Stability of the signal

The reference system, which is the second part of the detection scheme, compares the extracted salient features with the inferred reference features. It uses the rules of inference combined by heuristic reasoning principles to find the right behavior for every fault case. The classification of a detected failure is dependent on the relay's protection quality and it's effects to the power system reliability.

Testing Strategies

The two major problems in the software business are the excessive cost and unreliability of software. It should be obvious that the high cost of software is largely due to reliability problems. The best way to dramatically reduce of software costs is to reduce the maintenance and testing costs [3]. Except for the idea of informal manual proofs, the entire concept of proving program correctness is of no practical use today. Therefore due to economical aspects protection equipment will be evaluated by testing. However, it is impossible to guarantee the absence of errors in a nontrivial program. The role of testing is to locate the remaining small numbers of errors in a well-designed program.

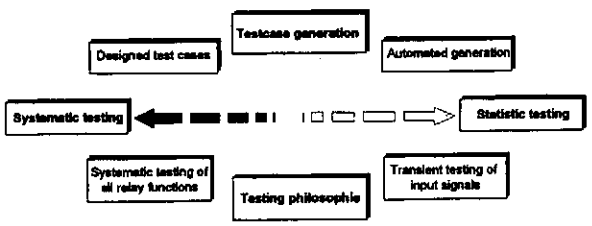

Fig. 6. Testing philosophy spectrum

In order to find discrepancies between the protection software and its external specification, statistic and systematic testing are useful strategies. The emphasis of the statistic approach is the testing with all kinds of dynamic fault conditions. In opposite to this, the systematic method is more orientated on the external specification of the relay.

Systematic Testing

Systematic testing uses cause-effect-graphing for segmenting the external specification into individual functions [4]. The art of test case design is really the art of selecting those test cases with the highest yield. Furthermore, each test case should represent a class of inputs. In this case, if the test case executes correctly, there is some confidence that a certain class of inputs will execute correctly, too.

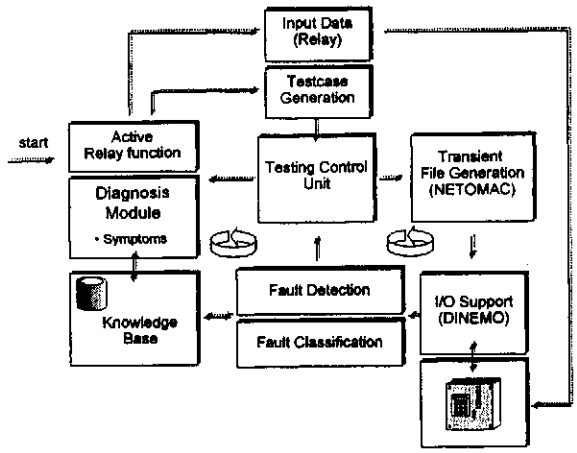

Fig. 7. Systematic Testing

For that, systematic testing with only a little testing investment is possible. Fig. 7 shows a block diagram of the systematic testing approach. Before testing a special part of the software, the relay is configured for evaluation these function. Each segmented function is tested with a special designed rate of test cases. If an error occurs, the fault diagnosis module attempts to find symptoms for each error. Refinements consist in deciding which components of the module are faulty.

Statistic Testing

Statistic testing is used for reliability control of protection equipment. In this case, the test data are generated automatically. For that, every fault case has the same probability to be tested. The extend of the sampling is dependent on the failure of the reliability estimation. In case of economical aspects, a strategy is implemented, using sampling testing in combination with a method of successive approximation to find discrepancies between the software and its external specification. Fig. 8 shows the schematic of the test procedure.

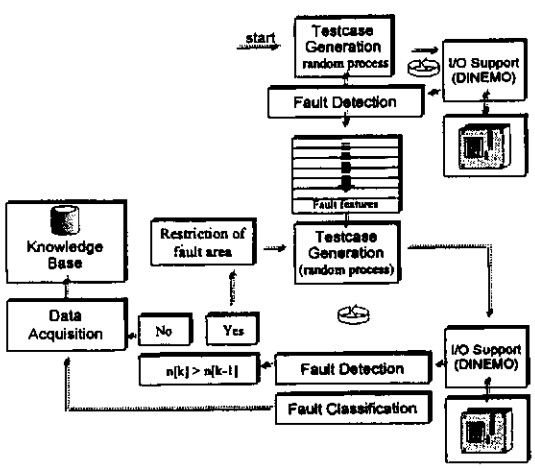

Fig. 8. Method of successful approximation

Starting this process, a sampling with large extension is tested. All errors, which occurs during this process, are stored in a buffer. In addition, the reliability of the relay is estimated in this test. After testing all cases, each stored type of error is investigated separately. Testing a fault event separately, the fault area is restricted, because only test cases of the restricted area are a part of the sampling. Successful approximation will rule out the dynamic conditions, which are responsible for an detected error.

V. RELAY TESTING

Varying the dynamic fault parameters a large number of test cases are available. The extent of the test is optional. Performance indices are used to quantify the reliability of the tested protection system. Fig. 9. Systematic test results shows an example for a systematic test result.

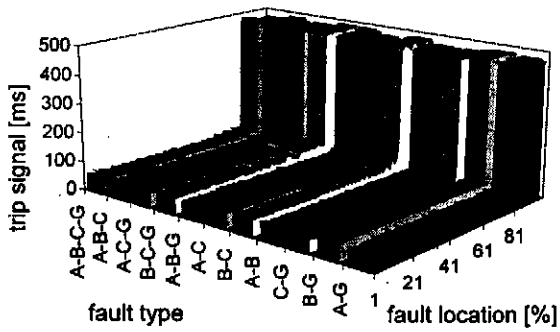

Fig. 9. Systematic test results

In this case a line protection relay was tested with ideal circumstances. The test includes more than 1000 cases, i.e., three-phase, phase-phase, phase-ground and phase-phase-ground faults. The fault location varied among 1 and 100 per cent of the transmission line length. All faults occurred in the maximum value of the voltage. The following schematic shows the relay configuration active during the tests:

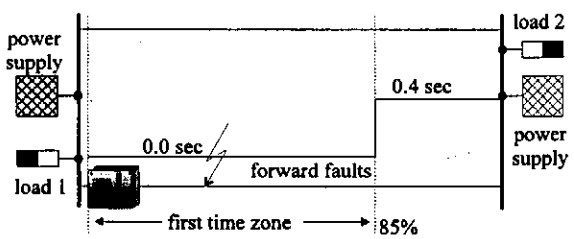

Fig. 10. Schematic of the relay configuration

VI. CONCLUSIONS

This paper described the Artemac real-time simulator for interactive dynamic testing of digital relays. Therefore Siemens AG in cooperation with the Technical University of Berlin developed a real time simulator system for high-end testing on a PC-based low-cost simulator system. Artemac is in use at the Siemens quality control department for digital relays in Berlin for manual and automatic testing of Siemens protection devices, for quality control and development of digital protection devices. The NETOMAC program is also used to design new algorithms under dynamic conditions. Fig. 11 shows an example of a transmission line relay on re-closing. The relay creates dynamic conditions on the simulated power system which are dependent on the timing of the initial response and action of the relay.

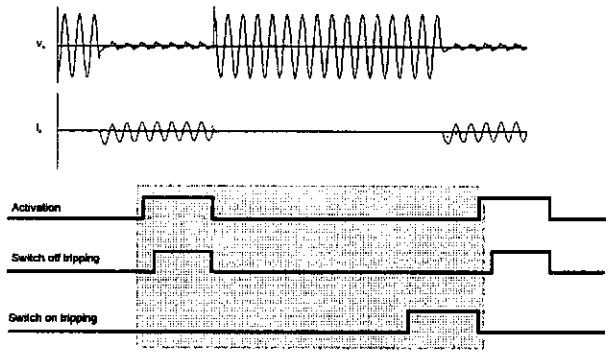

Fig. 11. Auto-re-closing process

The realization of the closed-loop-testing presented consists of the following components:

- A personal computer and the simulation tool NETOMAC, running under Windows 95.
- The I/O-card (ISA) developed, which uses the width of 16 Bit of the ISA-bus.
- The DINEMO, consisting of a communication interface, the A/D converter unit, the V/C converters and the voltage amplifiers.

Additionally Technical University has developed an automated testing environment, implemented as simulator surface, which will also be used for quality control. This application will reduce the testing costs and will rise the reliability of Siemens protection devices.

VII. REFERENCES

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Bernd Kulicke was born in Wernigerode, Germany in 1944. He received the M.S. degree in Electrical Engineering from the Technical University of Berlin and the Doctor degree in Power Engineering from the University of Darmstadt in 1970, on 1975 respectively. From 1970 to 1983 he was with the SIEMENS Company, working in the High Voltage and Power Engineering department. He is responsible for the development of the NETOMAC program and was mainly involved in performing system studies including electromechanical and -magnetical transients and stability problems. In 1984 he was appointed a Professor and Director of the Institute of Electrical Power Engineering at the Technical University of Berlin. Prof. Dr. Ing. B. Kulicke is a member of the IEEE Power Engineering Society.

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Olaf Ruhle was born in Germany in 1965. He received Dipl.-Ing. and his Ph. D. degree in electrical engineering from the Technical University of Berlin in 1990 and 1994 respectively. Since 1993 he is a member of Power Transmission and Distribution Group and the system planning department at Siemens in Erlangen, Germany. He is working on power system stability, dynamics of multimachine systems, control, optimization and identification problems in electrical power systems. He is responsible for the NETOMAC/NETCAD program support, sale and training worldwide.

Wilhelm Winter was born in Germany in 1963. He received Dipl.-Ing. and his Ph. D. degree in electrical engineering from the Technical University of Berlin in 1995 and 1998 respectively. Until 1997 he was mainly involved in the development of the NETOMAC based Real Time Digital Simulator in cooperation with the protection development group at Siemens in Berlin. Since 1998 he is a member of the HVDC/FACTS group and the Siemens System Planning Department. He is involved in studies of large interconnected power systems in time and frequency domain. He is responsible for the Neva Eigenvalue Analysis program development.