Network Decoupling by Latency Exploitation and Distributed Hardware Architecture

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Abstract- **This paper presents two basic concepts with the purpose of representing full size power system networks for real-time and on-line simulation, and their respective result s when applied to some simple electric networks. The first concept is the exploitation of latency characteristics where an electric network can be solved with different time steps according to the subsystems' time constants. The second concept is the implementation of a distributed solver architecture, where a network of inexpensive workstations can be used to achieve real-time simulation for fast power system transients. The paper also proposes the combination of these two ideas to further enhance the application domain of the real-time simulator.**

Keywords: Real Time, Latency Exploitation, Power system simulator, EMTP, OVNI, PC cluster.

I. INTRODUCTION

The Electromagnetic Transients Program EMTP [1] is the standard tool worldwide for power system transients simulation. There are situations, however, where very sensitive equipment needs to be tested under the same conditions it will experience in the power system. This requirement provided the motivation for the development of real-time digital simulators that still use the basic concepts for transient simulation presented in [1], but are capable of achieving real-time performance. Over almost a decade now, various research groups have been able to achieve real-time performance [2], [3], [4].

The real-time research group of the University of British Columbia has been continuously advancing the concept of a full-size real-time power system simulator, which eventually resulted in the OVNI ("Object Virtual Network Integrator") power system simulator [5]. The OVNI simulator is aimed at representing full-size power system networks for real-time and on-line simulation. To cope with the dimensions of the problem, partitioning techniques are required, both in the system solution and in the hardware implementation. OVNI achieves the proposed design objectives using off-the-shelf Pentium-based personal workstations. Simultaneous efficient solution of large networks is achieved using the MATE concept ("Multi-Area Thevenin Equivalent") [5] to parcel the solution along boundaries of maximum solution efficiency. Due to the requirements of sustained continuous simulation, all parts of the network have to be solved together, that is, Δt delays among subsystems are not allowed.

One of the natural ways to separate solution regions is to recognize that some subsystems or components have long time constants, and relative large solution steps Δt are sufficient for an accurate solution, while some other subsystems have short time constants and require much smaller Δt's. In these cases it is wasteful to solve the slow system at each Δt of the fast system solution. The exploitation of these latency characteristics was initially proposed in [6], and further explored in [7]. This paper shows the results obtained when simulating a lumped circuit and a circuit with transmission lines using the dual time-step methodology.

Using partitioning techniques in the hardware implementation as well as taking advantage of the decoupling introduced by the model of the transmission lines leads to the development of a distributed solver architecture, where a network of inexpensive workstations can be used to achieve real-time simulation for fast transients of large power systems [8]. This is particularly important for certain power networks in which real-time simulation would not be achieved in a single computer. The paper presents the results of simulation of a circuit with transmission lines implemented in the OVNI simulator.

The application of the latency concept can be ideally combined with the distributed solver architecture. In this case, for example, one computer can be assigned the task of solving a fast area of the power network presumably because of a component modelled in great detail, while another computer may be assigned the task of solving the rest of the network, which is slow compared to the fast component. This is part of the ongoing research and the relevant ideas have been outlined in the paper.

II. SIMULATION RESULTS WITH LATENCY EXPLOITATION

A. Lumped Parameter System

In order to test the accuracy of latency exploitation in a lumped network, the circuit proposed in [6] was adopted

1. Receiving a scholarship from CAPES, Brasil.
2. Receiving a scholarship from CONICET, Argentina

and it is shown in Fig. 1. In this figure, vf is the voltage of the "fast" capacitor (1μF) and vs is the voltage of the "slow" capacitor (100μF). The voltage source with a frequency of 60Hz is applied at $t = 0$, and the switch closes at the same instant. Three different simulations have been performed, using the trapezoidal rule of integration:

(1)Standard procedure using a small time step for the whole circuit: $\Delta t = 0.5\mu s$;
(2)Dual step size: $\Delta t_{fast} = 0.5\mu s$ for the fast part, $\Delta t_{slow} = 2.0\mu s$ for the slow part;
(3)Large time step for the whole circuit: $\Delta t = 2.0\mu s$.

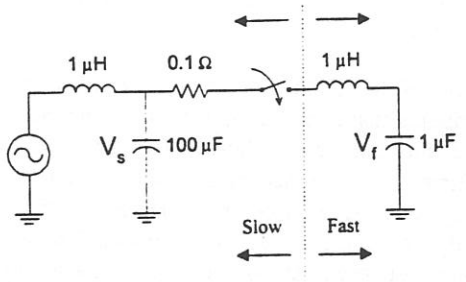

Figure 1: Lumped circuit for latency simulation

Fig. 2 shows the results of the simulations for the three methods for the voltage in the slow capacitor, while Fig. 3 shows the results for the voltage in the fast capacitor.

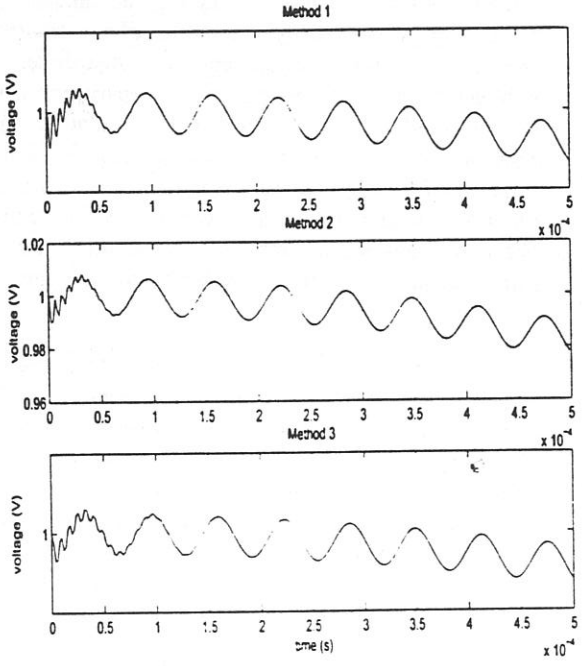

Figure 2: Voltage across the slow capacitor for the three methods proposed

The voltage on the slow capacitor is accurately predicted by the three methods. However, method 3 predicts wrongly the voltage on the fast capacitor, since a Δt of 2.0μs is not small enough to accurately simulate the fast dynamics of the fast part of the circuit.

B. Distributed parameter system

The application of latency concepts was also tested on a circuit with lossless transmission lines, similar to the one proposed in [6]. Fig. 4 shows the system studied. This circuit has two slow areas and one fast area. The system is energized at $t = 0$ by applying a sinusoidal voltage with frequency 60Hz and an initial charge of 1V is applied to the capacitor of the fast load.

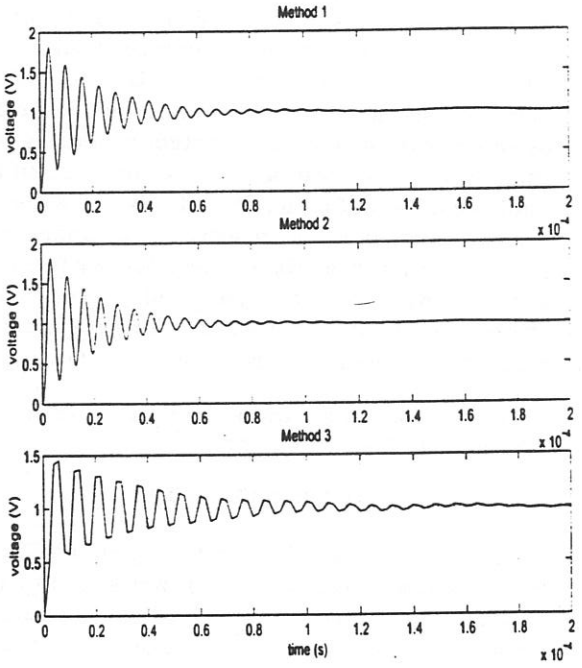

Figure 3: Voltage across the fast capacitor for the three methods proposed

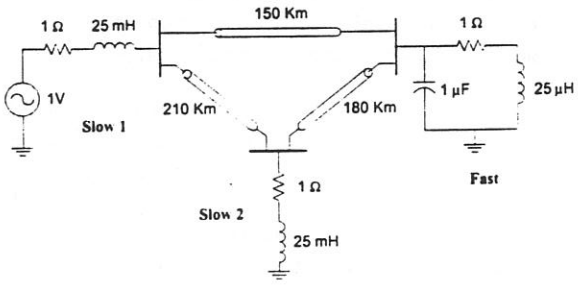

Figure 4: Circuit with transmission lines for latency simulation

Once again three different methods have been used for the simulations:

(1)Standard procedure using a small step size for the entire system: $\Delta t = 1.0\mu s$;
(2)Dual step size: $\Delta t_{fast} = 1.0\mu s$ for the fast part, $\Delta t_{slow} = 10.0\mu s$ for the slow part;

(3)Large time step for the whole circuit: $\Delta t = 10.0\mu s$.

Fig. 5 shows the voltage across the inductor on the slow part 1 for the three methods simulated and Fig. 6 shows the voltage across the capacitor on the fast part, again for the three different methods.

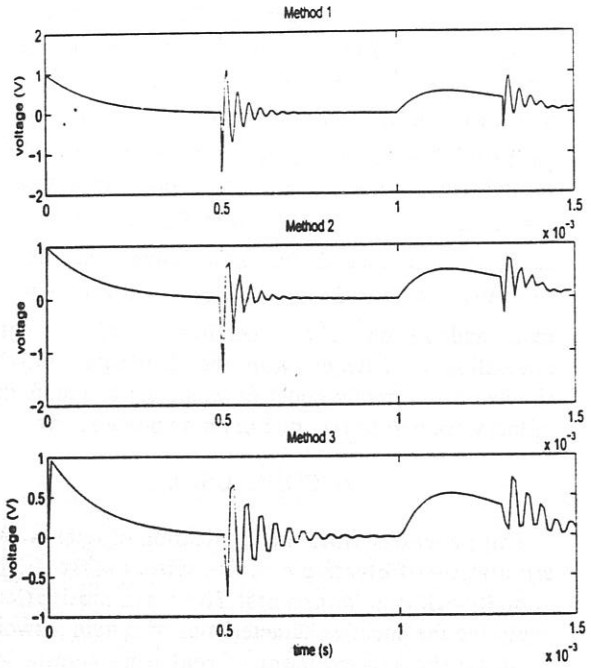

Figure 5: Voltage across the inductor on the slow part 1 for the three methods proposed

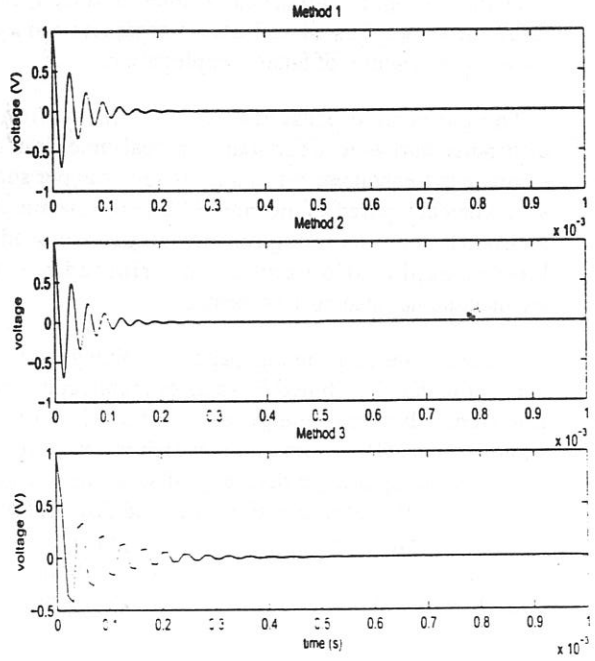

Figure 6: Voltage across the capacitor for the three methods proposed

Method 3 does not predict accurately the voltage across the capacitor and the inductor. Method 1, as would be expected, gives accurate results for both variables. Method 2 is capable of giving accurate results for the voltage across the capacitor situated on the fast part. Regarding the voltage across the inductor on slow part I, the results are still fairly accurate when compared to method 1. The effect of the fast system on the slow system is taken into account by an averaging technique that prevents aliasing of frequency components of the fast system that are beyond the Nyquist frequency of the slow one.

III. DISTRIBUTED HARDWARE ARCHITECTURE

The distributed hardware architecture based on the PC-cluster presented in [8] achieves real-time performance and linear scalability using an inexpensive proprietary card design that we developed in our own labs to fit our particular simulation strategy. This strategy is based on the concept of mapping a network of PCs to the characteristics of the power system solution network. Thus, the concepts of natural decoupling introduced by the model of the transmission lines, by MATE and by Latency are perfectly applicable to the distributed hardware solution.

Under the proposed distributed layout, a master unit is in charge of preprocessing the input data, performing the user interface functions, and distributing the solution among the PCs of the cluster. This distribution of cases is achieved through TCP/IP protocol. Each slave computer of the cluster calculates its part of the network solution while performing the interaction with its neighbors through the developed I/O interface card. A unique and shared synchronization source assures a perfect real-time behaviour for the cluster. The slave nodes only require the computational power (CPU), memory (RAM) and standard communication ports provided in any off-the-shelf mother board. If interaction with analog equipment is required, such as in the case of relay testing, it can be easily accomplished through D/A cards connected to the corresponding slave nodes.

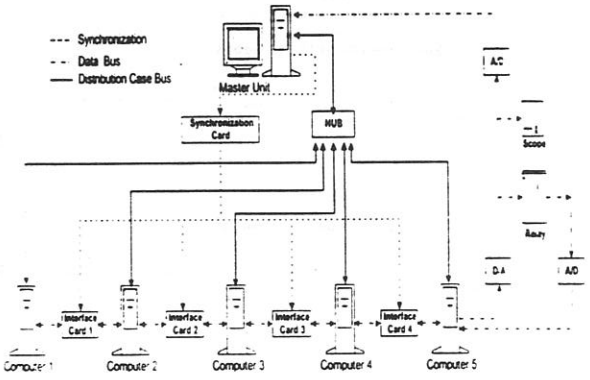

Figure 7: Distributed Hardware Architecture

IV. SIMULATION RESULTS WITH PC-CLUSTER

To obtain better insights on the performance of a real-time network simulator based on a distributed architecture, a system involving a cluster of five PCs is presented. The simulated network consist of a 234 node/349 branch system which includes sources, three phase transmission lines featured in single and double circuits, series capacitors with MOVs, six analog outputs, and Thevenin equivalent circuits for the external parts of the network, shown in Fig. 8. For this sample system, the OVNI simulator can operate in real-time with the proposed distributed architecture with a Δt of 46 μs, while the same system simulated in a single PC takes 162 μs. The timing results are shown in Table 1.

Table 1. Distributed hardware timing results for PII 400 MHz

Architecture		Nodes per Machine	Total Solution Time	Analog Outputs
Single PC		234	162.0 μs	6
PC-cluster	PC 1	54	45.34 μs	3
	PC 2	42	45.90 μs	0
	PC 3	42	45.81 μs	0
	PC 4	42	45.85 μs	0
	PC 5	54	45.32 μs	3

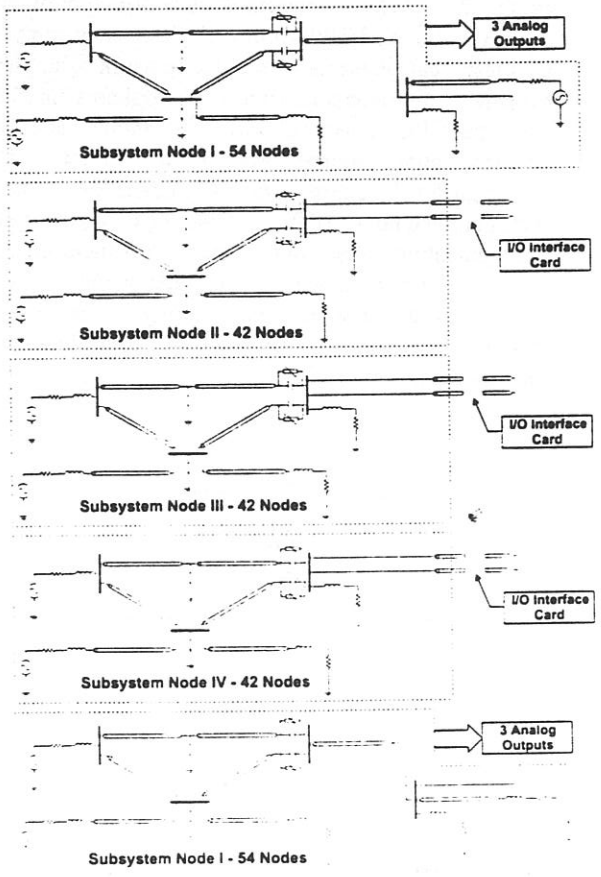

Figure 8: Sample Case running a PC-cluster of five PCs

V. LATENCY EXPLOITATION IN A DISTRIBUTED HARDWARE ENVIRONMENT

The latency concept for the simulation of subsystems with widely different time constants interconnected through transmission lines, as in the example of Fig. 4, can be "naturally" adapted to the PC-cluster concept of Fig. 7. Assuming, for example, that in the system of Fig. 4, Δt_{slow} is two times larger than Δt_{fast}, then two PCs are sufficient to solve the network in real-time (instead of the three PCs that would be needed for equal Δt's across the network). The way this works as follows. At $t = \Delta t_{fast}$ the first PC solves the fast part of the network, while the second PC solves the slow one subsystem. At $t = 2 \cdot \Delta t_{fast} = \Delta t_{slow}$, the first PC still solve the fast area, but the second PC now solves the slow two subsystem. At $t = 3 \cdot \Delta t_{fast}$, we go back to $t = \Delta t_{fast}$ case, and so on. The generalization of the outlined integration of Latency with the distributed PC-cluster simulator is currently under development and more details of this work will be reported in future publications.

VI. CONCLUSIONS

This paper describes the application of latency for the simulation of electric circuits with widely different subnetwork time constants. The main motivation for exploring the latency characteristics of certain networks is to allow the achievement of real-time simulation in applications where the time requirements may become extremely demanding. In this case the partition of subnetworks according to their time constants can considerably reduce the hardware requirements for real-time simulation. Results are presented in the paper with lumped, as well as distributed parameter networks, showing the validity of latency exploitation.

The paper also presents the implementation of a distributed hardware architecture for real-time simulation, showing the enhancement of simulation time per solution step when compared to the single PC real-time simulator. A proposal for combining the advantages achieved with latency exploitation and the distributed hardware architecture has also been presented.

The ideas presented in this paper combining the Latency concept with a distributed PC-cluster architecture are just few steps advancing the potential of a fully "organic" simulator (the OVNI simulator) which is conceived to be capable of integrating a diversity of solutions techniques (including different integration rules and different Δt's) in its separate subsystem components, and then bringing all this solutions together in a *simultaneous* whole network solution within the constrains of real-time solutions.

VII. ACKNOWLEDGMENTS

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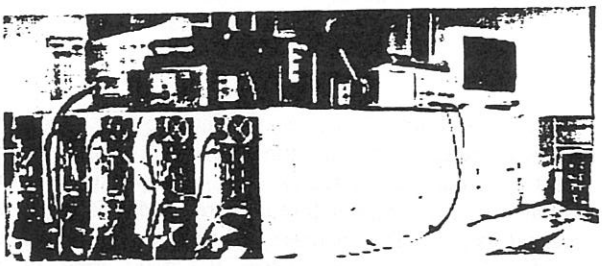

Figure 9: Rear and Front view of a PC-cluster at UBC's Real-Time Lab

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