Flicker Frequency Changing Effects with A TSC Applied To A Woodchip Mill

K.A.Walshe, *Member, IEEE, MIEE*

Abstract--The efficacy of any flicker compensator ("SVC") depends on the way that the SVC modifies the flicker spectrum of the load. With increasing attention being paid to smaller fluctuating loads, the TSC has a strong economic attraction but suffers from a limited bandwidth plus the bad habit of magnifying the higher flicker frequency components. These characteristics are dependent on the step size of the TSC and the characteristics of the fluctuating load.

This paper reports EMTP-ATP analysis used to size a TSC for a wood chip mill using a 3.3kV, 2.1MVA induction motor powered chipper fed from the end of an extended 132/66/11 kV transmission system and experiences fault 10 levels of 175 MVA (maximum) to 54MVA (normal minimum) at the 11kV bus. The original saturated reactor SVC installed in the 1970's is now over rated for present day duties due to network and plant changes. In addition there are now ongoing concerns about maintenance and cost of losses. Changes to electricity supply contracts also created pressure to control power factor as well as voltage flicker. The paper reports a series of ATP studies and site measurements aimed at establishing what compensation is required today and fixing the step size of a TSC so as to maximise the Flicker Reduction Factor achieved.

Keywords: ATP, TSC, flicker, flicker meter

I. Introduction

The SEFE Woodchip mill is located on the far south coast of New South Wales (Australia). It was originally commissioned in 1976 . At that time the site employed both debarking and chipping machines as well as substantial power consuming ship loading systems. The region is characterised by a coastal dairy industry surrounded by dense forests and a steep escarpment leading to the alpine regions of the Snowy Mountains. In the intervening years tourism and "life style change" has seen a rapid growth in consumers sensitive to voltage flicker. The Woodchip mill is thus located far removed from other heavy industries and exposed as the sole producer of flicker.

Electricity power supply is via a radial system originating at a bulk transmission point in Canberra some 300 km distant. Loadflow studies determined that an SVC was required to enable the site to function on the public network [1]. The original SVC employed a slope corrected treble tripler saturated reactor and associated shunt capacitor bank of approximately 14MVAr capacity. Because this SVC served a dual role of supporting the local MV network and suppressing flicker it was located in the local Utilities substation.

In the intervening years the site has changed to using regrowth timber which is of smaller diameter compared to the original logs used, has ceased using the debarker and changed its ship loading systems. The remaining fluctuating load is a 2MVA, 24pole 3.3kV wound rotor induction motor.

A particular characteristic of this motor is the relatively low power factor at full load which makes the kW, kVAr swings in normal operation quite different to a "normal motor".

Concurrent with the changes at the Mill, the power system had developed by

- extending the 132kV system,
- experienced vigorous load growth in the region
- started to experience maintenance problems with tap changers associated with the Edrom substation, and
- needed to take a further 11kV circuit out of the Edrom substation

Finally billing complications brought about by the introduction of electricity market brought attention onto the dual role of the Edrom SVC in suppressing flicker and supporting the Utilities network.

It was therefore required to evaluate all the changes that had taken place in order to determine the optimum strategy for the site. After a preliminary review of the situation it was agreed that system tests using the largest diameter logs anticipated to be used in the future should be carried to determine the need or otherwise for the SVC.

II. System Studies

A. Chipper Motor Data

The chipper motor is a Toshiba wound rotor 24 pole 3.3kV induction motor with the following Test Data:

No-load test:

50 Hz, 3300V, 189.2 amps 36.6 kW

= 1.0814 MVA, 36.6kW, 1.0808 MVAr lagging.

Calculated (by manufacturer) Load Conditions:

100% load, 362.1amps, 95.7% eff, 0.753 PF lagging,

slip 0.94% = 2.0697 MVA, 1.558 MW, 1.362 MVAr

Thus the worst case swing to be expected from this machine excluding overload is 1.5214 MW, 0.282 MVAr.

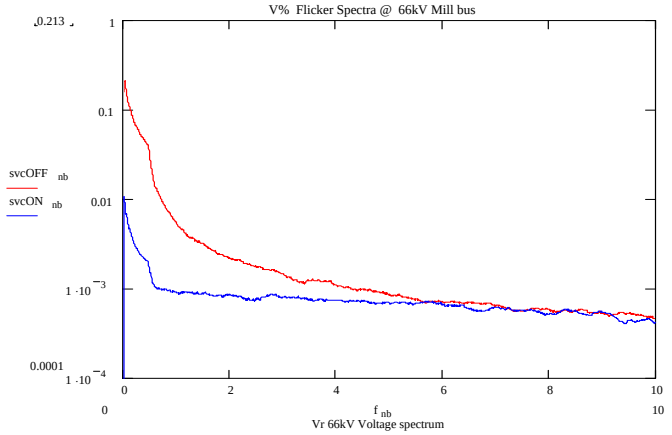
This work was carried out at the joint request of the SEFE Pty Ltd. mill and Country Energy, the electricity utility

K. A. Walshe is the Principal of Power Quality Technologies Pty Ltd. 9/330 Wattle Street, Ultimo NSW 2007, Australia (kwalshe@powerquality.com.au)

Presented at the International Conference on Power Systems Transients (IPST'05) in Montreal, Canada on June 19-23, 2005
Paper No. IPST05 - 061

B. *Field tests*

Field tests were carried out using logs representative of the largest / hardest likely to be used in the future. Measurements were made at the Mill 66kV busbar and also at Pambula a remote township deemed to be particularly sensitive by the Utility.



Upper trace – SVC OFF, Lower trace – Saturated reactor SVC ON

Fig. 1 Flicker frequency with SR SVC ON and OFF.

The measurement system comprised secondary "clamp" type CTs on the protection circuits and the bus PT signal. These were captured using an attenuator and anti-alising filter feeding a LabView based virtual instrument which captured the cycle by cycle *rms* values of the signals plus the full waveform over the last second of the recording period using a 5kHz sampling rate.

Post processing of the data was carried out using MathCad. Flicker spectra shown in Fig. 1 were calculated by taking the cycle by cycle *rms* signals over a 100 second period which corresponded to approximately 20 logs, suppressing the mean value, taking a FFT of the resulting signal then scaling to "% of the mean *rms* value". Finally a moving average of the FFT components was taken to generate a smooth curve.

This process was repeated for the cases of having the present SVC both On and OFF.

The effectiveness of the saturated reactor SVC at frequencies up to 6 Hz is readily seen. The SVC OFF curve shows that effective flicker suppression of this load requires that any replacement SVC is able to be most effective up to about 4 Hz.

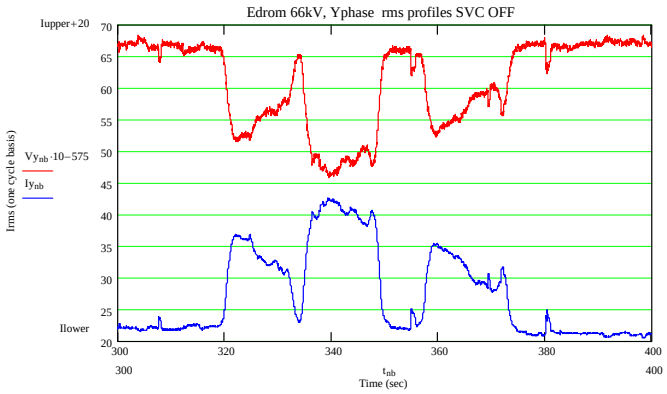
Fig. 2 shows an example of the 66kV *rms* voltage and current values with the present SVC OFF.

TABLE I
THREE PHASE BOLTED FAULT - MVA - ANSI/IEEE

Bus Name	SteadyState AC-Comp	Bus Name	SteadyState AC-Comp
CAN330	7492.5	BEGA66	197.5
CAN132	3433.4	PAMBULA	128.8
COOMA132	575.3	EDEN66	64.0
COOMA66	347.6	EDROM66	51.0
BEGA132	248.0	MILL11	35.1

TABLE II - dV/dP AND dV/dQ BY LOADFLOW

Case	*dVsite11*	*dVsite66*	*dVpam66*
Base	0	0	0
+1.0 MW	-1.24085	-1.03705	-0.31902
+1.0 MVAr	-2.55312	-1.65898	-0.70364
+1.+j1. MVA	-3.82075	-2.08897	-1.02713



Upper trace - 66kV Mill voltage scaled [V*10. -575]

Lower trace - 66kV line current for entire site.

Fig. 2 66kV bus Waveforms SVC OFF.

C. *Preliminary Loadflow and FaultLevel*

A very good insight to the behaviour of a network to incremental changes in P(MW) and Q(MVAr) can be obtained by carrying out a loadflow to establish tap settings then freezing the taps and recalculating voltage profiles for +1.MW, +1.MAVr and 1.+j1. MVA loads.

The load sensitivity coefficients & fault levels for the system (no outages) are :

D. *IEC Flicker Meter*

Kendal and others [2, 3] had by the early 1970's established that human perception of light flicker arising from the effect of voltage fluctuations on incandescent lighting was very sensitive to the shape of the fluctuation waveform i.e. both the amplitude and the phase of the sub-harmonic components that made up the fluctuation waveform had to be considered. These researchers had shown that ramped voltage changes had a far lower propensity to cause flicker than step changes.

Early attempts to use thyristor switched capacitors as flicker compensators had not proven very satisfactory[1]. This result can almost be predetermined as the TSC changes what are normally ramped voltage changes in a larger number of smaller step voltage changes.

Many approaches were used to try to predict and define flicker e.g. the 10Hz equivalent wave used in Japan and the IEC flicker meter developed in Europe.

One of the tasks of this simulation is to determine which TSC step size gives best results in terms of the residual flicker voltage as a function of the step size thus the IEC flicker meter was modelled in ATP.

[1] This comment is based on the author's knowledge of a failed attempt to use a TSC on a small arc-furnace in Melbourne and the subtle change in the way TSCs were promoted during the 1970's see for example [4]

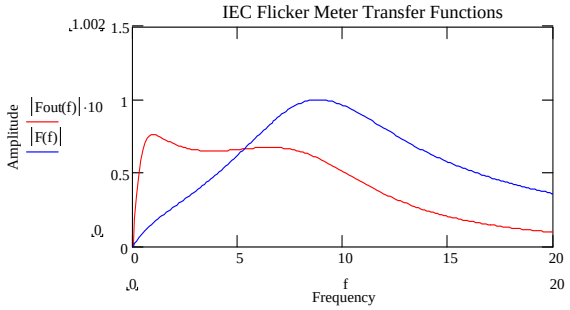
The IEC Flicker Meter is a very complex tool relying short and medium time statistical assessment of the waveform. This is not feasible in a short time domain simulation and so the stages to the output of Block 4 in AS/NZS 4376:1996 (which gives the functional and design specification for the IEC Flicker Meter) were implemented in TACS.

The frequency response of the circuit was tested to Table 1 of AS 4376:1996. It was found that the circuit was very accurate at the peak sensitivity of 8.8Hz but errors within the tolerance (+/- 10%) permitted by the Standard occurred at other frequencies. This is interesting given that the Standard prescribes the transfer functions to be used.

The output was also integrated for 60 seconds of run time to indicate the short time flicker severity. This signal was scaled to give a value of Unity for the 8.8Hz sine wave test voltage prescribed in the Standard. This gives a measure of the short term flicker "dose" and is similar in concept to the 10Hz equivalent flicker voltage used by Japanese Utilities.

E. Flicker Frequency Changing Effects of SVCs

1) Sinusoidal Fluctuation, Ideal SVC



Flicker weighting filter
Light curve - non-linear human eye response to flicker
Dark curve - basic 8.8Hz weighting curve (*10.0)

Fig. 3 Frequency Response in IEEE Flicker meter.

The action of a compensator can be viewed as producing a complimentary fluctuation waveform to that being produced by the load (rolling mill, mine winder etc) and the aim is that the sum of these two fluctuations should be less than the load fluctuation. There will be both a time lag, a scaling factor and possibly a hard limit on the compensator's contribution. This can be modelled as below:

giving

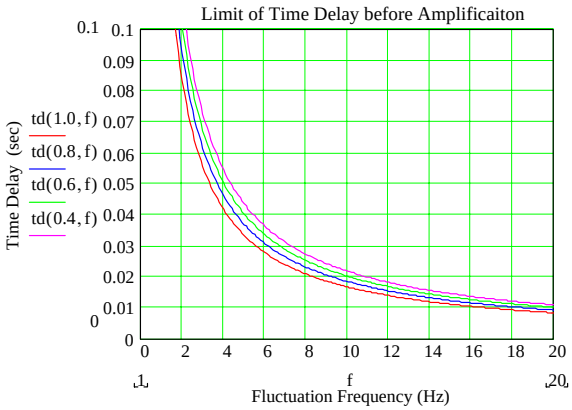
$$Qsvc = e^{-s\cdot t}\cdot k\cdot F(Q)$$

In phasor diagram terms the Compensator fluctuation lags the load fluctuation by an angle that varies with the delay. The limiting case for effectiveness of the compensator is when the net fluctuation is the same magnitude as the uncompensated fluctuation. Application of simple geometry gives:

$$Td(Qsvc) = \cos^{-1}\left(\frac{Qsvc}{2\cdot Qload}\right)\cdot\frac{1}{2\cdot\pi}\cdot\frac{1}{f}$$

where f = fluctuation frequency

and from this it follows that the maximum delay in compensation before amplification of a sinusoidal fluctuation is as given in the Fig. 4.



The curves are for 100%, 80% ..40% compensation.
On the graph the 40% curve is the upper most curve.

Fig. 4 Limit of time delay before amplification of sinewave flicker.

Since the critical frequency range for visual perception is 8 ~ 9 Hz it may be concluded that a compensator with an inherent delay (control + switching delays) of more than 20msec (50Hz system) will amplify the fluctuations.

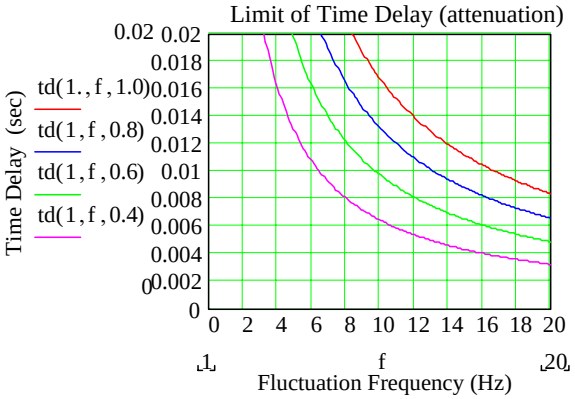
Next consider the agree of attenuation required. Define

$$M = \frac{Compensated\_Fluctuation}{Uncompensated\_Fluctuation}$$

and by simple geometry it follows that

$$Td(k, f, M) = \cos^{-1}\left(\frac{1}{2\cdot k}\cdot(k^2 - M^2 + 1)\right)\cdot\frac{1}{2\cdot\pi}\cdot\frac{1}{f}$$

giving the result opposite from which it can be seen that for any reasonable degree of suppression of sinusoidal fluctuations the time delay must be no more than half a cycle at 50Hz.



The curves are for flicker reduction to 100%, 80% ..40% of original and with Qsvc = Qload. On the graph the 100% curve is the upper most curve.

Fig.5 Limit of time delay for specified degree of sinewave flicker attenuation.

2) Square-wave fluctuations

When considering square-wave fluctuations the above simple analysis cannot be used due to the presence of multiple frequencies in the flicker component of the waveform plus the important influence of the relative phase of each frequency (waveshape is a major determinant of the severity of flicker).

The method adopted next is to use the TACS portion of ATP to model the compensation and to measure the fluctuation using the short time transfer functions of the IEC Flicker

meter. Since the compensator model works entirely at flicker frequencies, the first stage of the IEC meter, which demodulates the input waveform, is omitted. The simulation is allowed to run for 5.0 seconds and the results were taken over the last 1.0 second to allow the IEC flicker meter model to settle down. The flicker waveform was a square wave of +/-1 volt modulating a 100V crest 50 Hz sine wave.

The variations in the harmonic content of the compensated bus waveform can be related to the phase shift represented by the pure delay. Note how

- the modulation by 3 Hz has produced a series of odd harmonics of that frequency,
- the effect of a pure delay in the compensator can nearly double the flicker for certain combinations of delay time and flicker frequency, and
- a compensator that is "not quite fast enough" may be less useful than a very slow compensator

This last observation explains why early attempts to compensate electric arc furnaces ("EAF") using synchronous machines gave a modest reduction in flicker whilst attempts to use a TSC generally resulted in making the flicker a lot worse.

F. Dimensioning of a TSC

With the knowledge of the manner in which both pure time delay associated with thyristor switching and the delays associated with signal processing, an ATP + TACS model of the power system back to the Canberra 330kV supply point, the Woodchip drive and a multi-step TSC was developed using an open loop control based on the dV/dP and dV/dQ response of the Mill busbar. Once the dV/dP and dV/dQ characteristics of the system are determined, a value for the overall power factor of the chipper motor plus TSC required to limit the voltage swings to a predetermined amount can be calculated. For this study a target of zero voltage fluctuation was used in order to maintain existing performance.

Transmission lines were modelled as 3 phase mutually coupled (inductive and capacitive) circuits by using symmetrical component data from Country Energy and hence working back to the equivalent balanced line. An immediate consequence of this is that the line model is perfectly balanced and thus unbalance does not arise unless introduced directly by an unbalanced load model. When using such a model, dq0 transform based control systems are not subject to the ripple in their outputs which occurs when voltage and current unbalance is present.

The chipper motor was modelled as a "type 3" Universal Machine using the data supplied by Toshiba to derive a double cage induction motor model. This was done rather than using the wound rotor model because this latter model is restricted to one coil on each of the D and Q axis; by allowing the data fitting program to define 4 rotor coils gave greater ability to fit the motor's performance data into the available mathematical model. Starting performance on the multi-step resistor grid was checked using a wound rotor motor model but was not considered for flicker performance evaluation.

Chipper dynamics were modelled by a random time variation of the mechanical torque of the shaft load placed on the motor; i.e. it was a close to reality model in that it allows the inertia of the motor and chipper disk to influence the electrical response of the motor.

$$Torque\,(t) = 1 + 0.75 \cdot Random\,(t)$$

where *Random(t)* is evaluated every 1.0 second.

A multi step Thyristor Switched Capacitor with star connected capacitors, series detuning reactors and a thyristor / diode switch complete with it's own firing control to minimise switching disturbances was included in the model. Finally a control system was implemented in TACS to control the number of capacitor steps to be switched. These controls comprised a 3 phase calculation of kW and kVAr, smoothing with a 10msec first order lag, determination of Qtsc and resolution into numbers of steps to energise. Switching of capacitors was restricted to periods when the stored charge and the running system voltage where within 7% of each other.

The TSC was connected at 3.3 kV but in practice would be on the secondary side of a step down transformer to optimise the capacitor and thyristor / diode switch ratings. A 1.2 MVAr fixed capacitor was connected to the 3.3kV busbar.

TABLE III
EFFECT OF DELAY ON COMPENSATION OF SQUARE WAVE MODULATION

Harmonic Content [Hz]		**Compensated bus voltage with SVC delayed by stated msec. (pure delay); Input has 3.0Hz squarewave (10V) modulation.**						
Mains sideband	Flicker Freq.	Input signal	2.5	5.0	7.5	10.	15.	20.
47.	3	6.373	4.675	8.638	11.44	12.69	10.14	2.305
41.	9	2.123	1.368	2.57	3.507	4.084	3.961	2.253
35.	15	1.274	0.7051	1.343	1.880	2.275	2.537	2.053
29.	21	0.9101	0.4197	0.809	1.156	1.443	1.783	1.761
23.	27	0.7079	0.2603	0.506	0.735	0.940	1.253	1.406
17.	33	0.5793	0.1582	0.310	0.455	0.593	0.834	1.017
11.	39	0.4903	0.0870	0.171	0.186	0.334	0.487	0.627
5.	45	0.425	0.0344	0.068	0.101	0.134	0.199	0.264
Flicker severity expressed as "per unit" of input signal			0.0933	1.001	2.857	3.858	1.002	0.5269

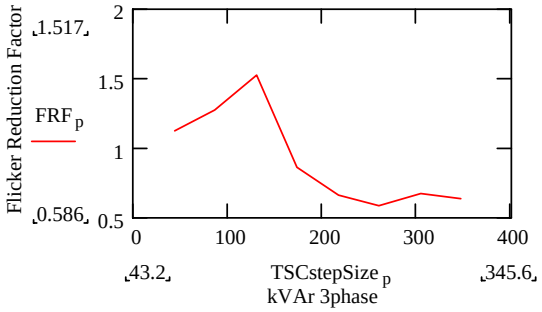
NB the flicker severity as measured by the IEC flicker meter rises to 2.959 at 30msec before falling to 1.590 at 40 msec i.e. there once the delay exceeds 5.0 msec the flicker severity after compensation varies between 3.0 and 0.5

Load disturbances associated with wood chipping are random in nature. Examination of chart recorder records made by the site maintenance manager suggested that a maximum torque of the order of 1.75 pu may occur. To model this a fixed torque of 100% plus a random torque of up to 75% of the full load torque of the motor was applied to the UM3 motor model every 1.0 seconds. This produced line current waveforms and 66kV voltage flicker spectra that were visually similar to samples collected by the mill staff.

Flicker severity was assessed using a TACS model of the IEC flicker meter previously described.

The size of the TSC step was varied using the $Parameter function such that Capacitor step size = 48kVAr * (study number), i.e. ranges from 48 to 384 kVAr in steps of 48kVAr.

Fig. 6 shows that there is an optimum TSC step size of around 120 kVAr if just flicker dose is used as the criterion. Including economics into the equation would suggest 12 steps of 150 kVAr or preferably a binary scheme of 4 stages based on a unity rating of 87 kVAr.

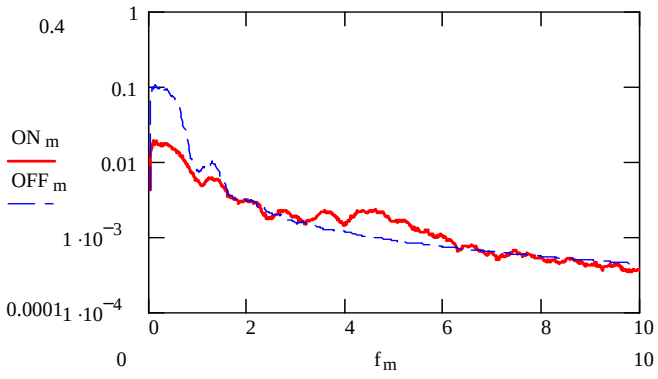


NB a flicker reduction factor <1.00 means flicker is made worse

Fig. 6 Flicker Reduction Factor as a function of TSC step size.

The reason that the smaller steps give a high flicker dose is partially due to them occasionally running out of range but also due to the fact that they move voltage flicker into the band of maximum sensitivity centered at 8.8 Hz.

Flicker frequency spectra for the 66kV busbar at the Mill were calculated for the best step size of TSC and the case of no TSC (to compare with the earlier site recordings). Fig. 7 shows that the frequency response of this TSC is little better than 2 Hz and includes a band from 3 Hz to 6 Hz were the flicker is magnified.



No TSC case - Thin line (dash), With optimum TSC – heavy solid line
Scale is "% of 50Hz voltage"

Fig. 7 Flicker Spectra Mill 66kV busbar (by ATP).

III. Discussion

In the early days of SVC technology, equipment kVAr (MVAr) ratings were determined by reference to the type of application (arc-furnace, rolling mill, mine winder etc) and a single value parameter would be calculated by essentially steady state methods, usually load flow. This method contained an implicit knowledge of and weighting for the frequency spectrum of the fluctuating load and the dynamic performance of the SVC. The performance parameter was based on experience.

This system gave a clear measurement performance under contractual conditions e.g. the short circuit voltage depression of an electric arc-furnace was easily measured with and without the SVC. Likewise the peak voltage depression during a mine winder cycle was readily measured.

With the introduction of power electronic SVCs and also flicker meters the situation became far less clear – predicting the reading of a flicker meter when a particular fluctuating load was connected was not at all straight forward and commercially dangerous.

The case study reported in this paper gives an account of the analysis undertaken to determine if a TSC could be used to replace an aging and now substantially over rated Saturated Reactor installation. It would have been very easy to determine the dynamic range required using loadflow techniques and then install a TSC that was sized for lowest capital cost based on that dynamic range. Had this been done the step size would have exceeded 200kVAr and the flicker dose experienced would have been more than double that for an optimally dimensioned TSC.

By utilising the many features of ATP it proved possible to identify the TSC step size which would give the greatest attenuation of flicker as measured by an IEC flicker meter.

During the course of the study it became very evident that characterisation of a load with a random component presents a major challenge since the study stands or falls on the validity of that part of the model. In this study the parameters defining the random load where adjusted until the flicker spectra "as measured" and "as computed by ATP" exhibited good similarity. With the benefit of hind-sight, site measurements of motor torque should have also been attempted.

The flicker frequency changing effect of the TSC was amply demonstrated; choice of a non-optimum step size would have seriously reduced the efficacy of the TSC. Even so the chosen TSC size moves flicker energy from the sub 2Hz region into the dangerous 4Hz and upwards region. It is only by making a substantial reduction of flicker energy below 2Hz that this latter increase can be tolerated.

The use of ATP

- enabled the optimum step size to be determined,
- provided the mill owner with the justification for the additional expenditure required
- allowed control strategies to be investigated, and
- provided the information necessary to convince potential TSC suppliers that close investigation of their

control strategies would be a major part of the tender analysis process.

IV. Acknowledgment

The author gratefully acknowledge the contributions of M. Woods (SEFE), C. Hackney and C. Halliday (Country Energy) in providing data and facilitating site tests. Toshiba International (Australia) located original works tests data for the chipper motor without which the study would have been very speculative.

V. References

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VI. Biographies

Keith Walshe (M'1997) was born in Derby, UK in 1944. He graduated with the IEE PartIII qualification from Portsmouth College of Technology in 1966, M.Sc. from The University of Aston in Birmingham in 1970 and the Ph.D. from U.M.I.S.T. in 1974. He has worked in electricity distribution, consulting, teaching, TCR R&D, project engineering and now runs a specialist Power Quality consulting company in Sydney Australia. His special fields of interest included power quality analysis in the time domain and investigation of abnormal behavior of power equipment.

Dr Walshe is a Member of both the IEEE and IEE, a Visiting Professor at the University of Wollongong, a Visiting Fellow at the Australian National University and regularly conducts classes for the Electricity Supply Association of Australia on Harmonic Distortion, Filters and analysis via the University of Wollongong. He also developed and runs a final year and post graduate course in Power & Electronics at the ANU.