Controller Design for STATCOM using Multi-level Double Converter System

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Abstract-- Converters used in high power application, high frequency switching is not desirable to decrease the power loss. To reduce higher harmonics while keeping switching frequency the lowest, that is fundamental frequency, multilevel converter is attractive configuration. In this paper, we have investigated five level converter as an example of multilevel converters. First, we show the basic characteristic of 5 level converter, and we also show that the double converter configuration can conquer the difficulties in controlling dc voltage of the multi-level converter. Then, multi-level converter application for static var compensator (STATCOM) is shown. Fundamental frequency switching is employed to minimize the switching loss in the converter, while phase angle between the converter output voltage and the ac system voltage is controlled to keep the total dc capacitor voltage. Pulse-width control of one of double converter is used to keep the voltage balance between each dc capacitors. Phase angle is used to control reactive power output. Finally, we show the computer simulation research by using ATP program. Simulation results of ac voltage control transients show that the ac and the total dc voltage is converging to the reference value smoothly and quickly, and the voltage balance of the dc capacitor is kept at the same value with short disturbance.

Keywords: STATCOM, multi-level converter, voltage control.

I. INTRODUCTION

THE reduction of the cost, the losses and the harmonic generation is the consecutive objects for the high power converters. In high power application using GTO thyristors or IGBTs[3], high frequency switching should be avoided. To reduce higher harmonics while keeping switching frequency the lowest, that is fundamental frequency, multilevel converter is attractive configuration. Multilevel converter configuration can reduce higher harmonics without using transformers. Though ac reactor is necessary, it is less expensive than transformers of same rating. This means that some cost reduction is also expectable. This paper suggests the multi-level double converter system for STATCOM. The difficulties of using multi-level converter exists in the stable control of the dc capacitor voltage.

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II. MULTI-LEVEL CONVERTER WITH CLAMP DIODE

For high power application, series connection of switching device is usually unavoidable, since one set of switches (sometimes it is called valve), which must be turned on and off at the same instance, has to have larger voltage rating than single semiconductor switching device. Series connection requires the coincidence of the switching characteristics of switching devices to be connected. To compensate the difference of the switching characteristics, especially turn off speed, snubber capacitor of certain amount of capacitance is installed for each switching device in parallel. The energy stored in the capacitor is consumed in the resistor and becomes loss. Multilevel converter configuration can avoid series connection of the switching device in one valve and can omit the snubber[1,2,4].

In this paper, we have investigated five level converter as an example of multilevel converters.

First, we show the basic characteristics of 5 level converter, and we discuss about some limitations of switching timing of valves at each of 5 voltage level when it is operated at the fundamental switching frequency. Then we show the computer simulation research for the dc voltage controller using ATP program.

Figure 1 shows the circuit of 3 phase 5 level converter. Figure 2 shows the output voltage of the converter in U-phase, V-phase and U-V line-to-line voltage. Line-to-line voltage may have 9 levels at maximum and 7 levels at minimum depending on the pulse width of θ_1 and θ_2.

Usually, the voltage of dc capacitance must be kept constant. Ideally, the charge of dc capacitor is not changed as long as the real power output of the converter is controlled to be zero. However, the converter has the power loss inside itself and the power may be supplied from dc capacitor if the converter is controlled to the zero real power. Then, dc capacitor voltage is decreased to zero without charging from ac system. If charging occurs, usually the balance between each dc capacitor voltage is lost, since the amount of charging current is different between the dc capacitors.

One way to avoid this unbalance is to use multi-pulse PWM method. However this method cause large switching loss. The switching loss occurs each switching timing and it is proportional to the switching frequency. To minimize it, the best way is to use the fundamental ac system frequency for the switching frequency.

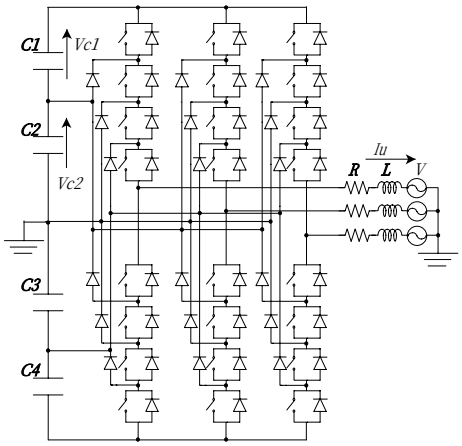


Fig.1 Circuit of 5 level converter

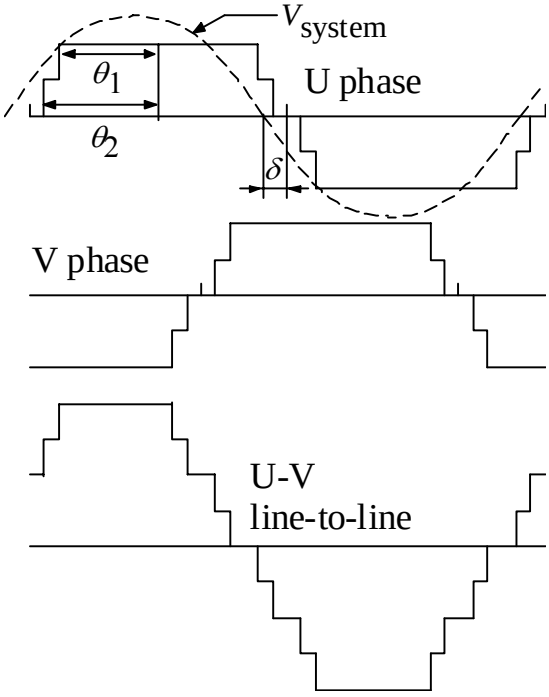


Fig.2 Output voltage of 5 level converter

We propose double converter configuration to keep the dc capacitor voltage balance. Figure 3 shows the double converter configuration of 5 level converter in one line diagram. Each dc capacitor has its own charging current from the converter A and discharging current from the converter B. The charging currents from the ac system for the dc capacitor C_{p1} and C_{p2} are described as follows.

$$I_{Cp2} = \frac{V_S}{X_S}\sin\theta_{p2}\sin\delta \quad , \quad I_{Cp1} = \frac{V_S}{X_S}\sin\theta_{p1}\sin\delta \,,$$

where $V_S = \frac{2\sqrt{6}}{\pi}V_C\left(\sin\theta_1 + \sin\theta_2\right)$, $X_S = 2\pi fL$.

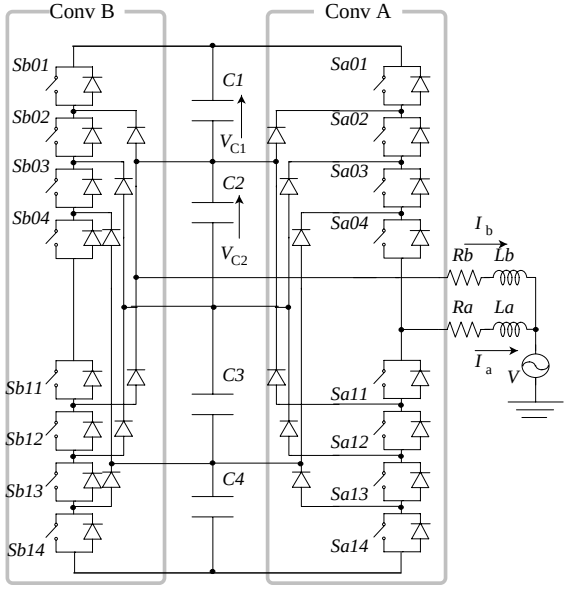


Fig.3 Double converter configuration of 5 level converter

The current from each converter can be controlled by the pulse width and can keep the dc voltage constant.

III. CONTROL SYSTEM FOR MULTI-LEVEL CONVERTER

Essentially, phase angle and pulse width are the control factor for the control of the multi-level converter. Pulse width is controlled independently for each voltage level. Total dc voltage and ac output voltage are controlled by the phase angle. Voltage balance between dc capacitors is controlled by the pulse width. Detail of the controller design are described in following sections.

A. Control of phase angle and pulse width

Figure 4 shows the control method of phase angle and pulse width of the converter.

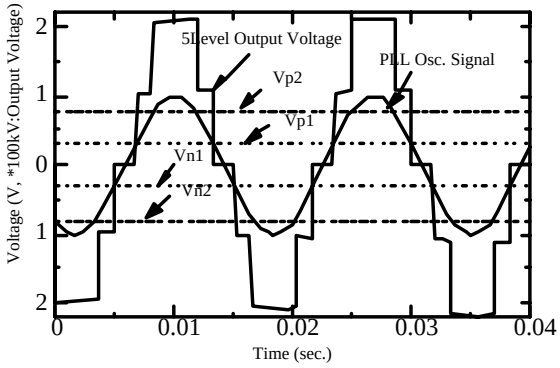


Fig.4 Control signal and output voltage of 5 level converter (PLL Osc. signal: Sine Wave Phase Shifted to AC system; Vp2, Vp1, Vn1, Vn2: Reference Voltage for Pulse Width)

PLL oscillation signal is synchronized to the ac system voltage and has the unity amplitude. Reference Voltage for Pulse Width (Vp2, Vp1, Vn1, Vn2) determines the pulse width of each voltage level. If sinusoidal PLL signal is larger than Vp2, then the highest dc voltage is output by switching the upper most 4 switches on. If sinusoidal PLL signal is smaller than Vp2 and larger than Vp1, then the second high dc voltage is output by switching the next 4 switches on. Similarly switching signals change. To control the real power, the phase between ac system voltage and the output fundamental voltage of the converter should be change. The sinusoidal PLL waveforms can be shifted by changing the oscillation frequency.

B. Total dc voltage controller using phase angle

Figure 5 shows the control system for the phase angle. By measuring the dc voltage and comparing it with the reference, carrier signal generator changes its oscillation frequency and works as a kind of the phase locked loop, using proportional control.

$$\frac{V_{dc}}{V_{dc,ref}} = \frac{4K_1 I_M A_1 / C}{s^2 + \left(4K_1 I_M A_1 / C\right)} = \frac{k\omega_n^2}{s^2 + 2\varsigma\omega_n s + \omega_n^2} \qquad ...(11)$$

where $A_1 = \sin\theta_1 + \sin\theta_2$, $I_M = \left(V_s V_r\right) / \left(X_S V_{dc}\right)$

Above equation has zero coefficient of "s" term in denominator. That is, this control loop cannot have damping. Therefore, current feedback loop with K_2, as shown in Figure 5, is added to increase the stability.

$$\frac{V_{dc}}{V_{dc,ref}} = \frac{4K_1 I_M / C}{s^2 + \left(4K_2 I_M\right)s + \left(4K_1 I_M / C\right)} \qquad ...(12)$$

K_1 is designed to be ω_n=10, and K_2 is designed to be ζ=1.0.

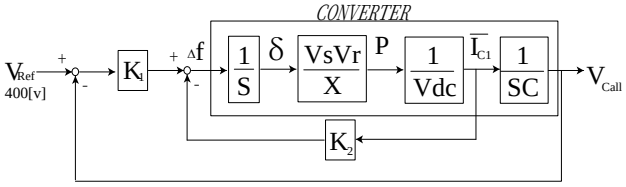


Fig.5 Control system for phase angle to keep total dc voltage

C. Voltage balance controller using pulse width

Figure 6 shows the voltage balance control system. Pulse width θ_1 and θ_2 are set to satisfy the following relation to keep the fundamental component of output ac voltage constant.

$$A_1 = \sin\theta_1 + \sin\theta_2 = const. \qquad ...(13)$$

When Vcp2>Vcp1, then θ_1 is increased and θ_2 is decreased correspondingly. The controller in Figure 6 is P-I type and the transfer function of the control loop is as follows.

$$\frac{V_{Cp1} - V_{Cp2}}{\Delta V_{C12,ref}} = \frac{\left(K_4 I_\theta / C\right)s + \left(K_5 I_\theta / C\right)}{s^2 + \left(K_4 I_\theta / C\right)s + \left(K_5 I_\theta / C\right)} \qquad ...(14)$$

where $I_\theta = \frac{V_{ac}}{X_S}\frac{3}{2\pi}\left(\cos\theta_1 - \cos\theta_2\right)$,

$\theta_1 = \theta_{p1} = \theta_{n1}$, $\theta_2 = \theta_{p2} = \theta_{n2}$

K_4 is designed to be ω_n=16.7, and K_5 is designed to be ζ=1.3. First order filter with time constant T_c=0.05 [sec] is added in the loop to prevent the resonance with ac reactor and dc capacitor. One problem occurs in this control loop. That is the charging current is affected by the phase difference δ between the converter ac voltage and the system voltage. It is caused by the real power, flowing into the converter, expressed as following equation.

$$P_r = \frac{V_s V_r}{X_{ac}}\sin\delta = \frac{V_s}{X_{ac}}\left\{\frac{2\sqrt{6}}{\pi}V_C\left(\sin\theta_1 + \sin\theta_2\right)\right\}\sin\delta \qquad ...(15)$$

Above equation means the direction of charging and discharging is changed by the sign of δ. And at the same time the gain of the loop is also changed by the amount of δ. Following coefficient is introduced to the controller to minimize the effect of δ, since $\sin\delta$ is approximated when δ is small.

$$\delta/(\delta^2+k)$$

Here, k is the small constant to keep the denominator non-zero. This also decreases the sensitivity of the control when δ is small. Then the control is not effective as seen from (15). Coefficient k is set to be 0.05.

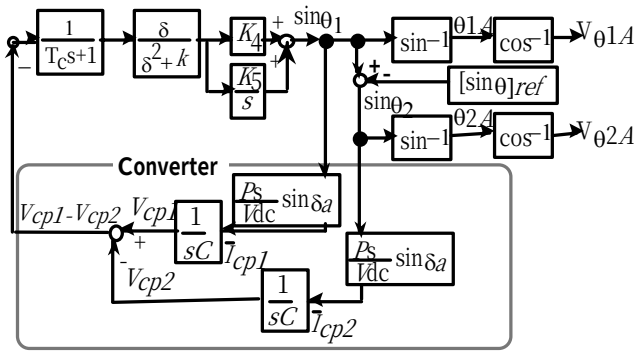


Fig.6 Control system for pulse width to keep voltage balance

D. Voltage controller using phase difference

Figure 7 shows the phasor diagram of reactive power control system using phase angle control δ_B. It is geographically noticed that the reactive current I_s is controlled by changing δ_B. If δ_B becomes smaller, then δ_A becomes smaller automatically because of dc voltage control.

Integration controller shown in following equation is used. Gain K_{delta} is set to be 0.2 [rad. /(sec.kV)].

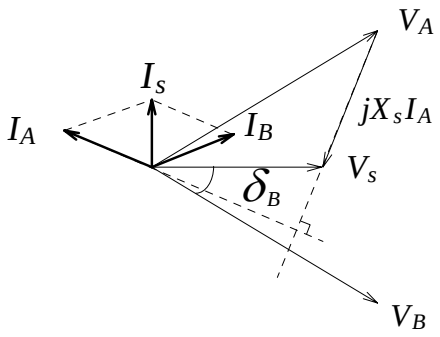


Fig.7 Phasor diagram of reactive power control system using phase angle control

$$\delta_B = \frac{K_{delta}}{s}\left(V_{REF} - V_S\right) + \delta_{B0} \qquad \text{……(24)}$$

IV. SIMULATION MODEL

Computer simulation has been performed to certify the validity of control system by using ATP (Alternative Transient Program).

Table 1 and 2 show the circuit parameters and initial pulse widths used for simulation.

TABLE 1 CIRCUIT PARAMETERS OF SIMULATION SETTING

	Value	Initial condition
C	1000[μF]	100[kV]
R	1[Ω]	
L	0.1[H]	0.0[kA]

TABLE 2 PULSE WIDTHS USED IN SIMULATION

	θ_1	θ_2
Converter A (initial value)	36 deg.	72 deg.
Converter B (constants)	36 deg.	72 deg.

One-line diagram of the 5-level double converter circuit is shown in Fig. 8. It shows the simplified model of the model shown in Figure 3 for the ATP simulation. Modes of operation are same for both models, since controlled switch and diode switch have the ideal switching characteristics. That means there is no forward voltage drop or no nonlinear transient of switch resistance. The circuit in Fig.8 also improves the simulation speed and numeric stability at the same time. Therefore, simulation results shown in next section have been performed using the model in Fig. 8.

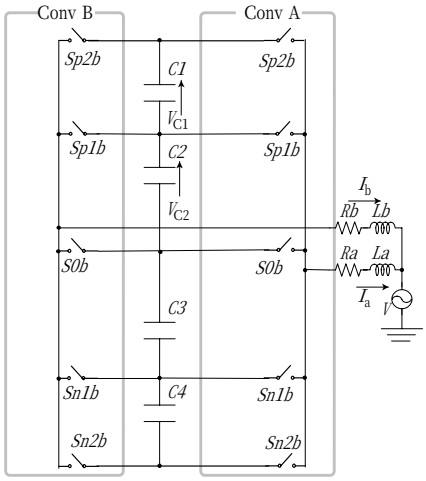


Fig.8 ATP simulation model of double converter circuit in one line diagram

Figure 9 shows the simulated system configuration in one line diagram. At the midpoint of the long transmission line, STATCOM using multi-level double converter is installed. 3 phase to ground (3LG) fault occurs near the receiving end at 2 second. The fault recovered at 2.4 second.

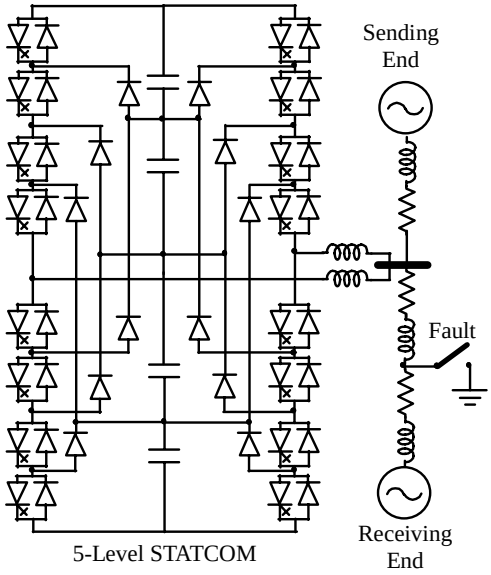
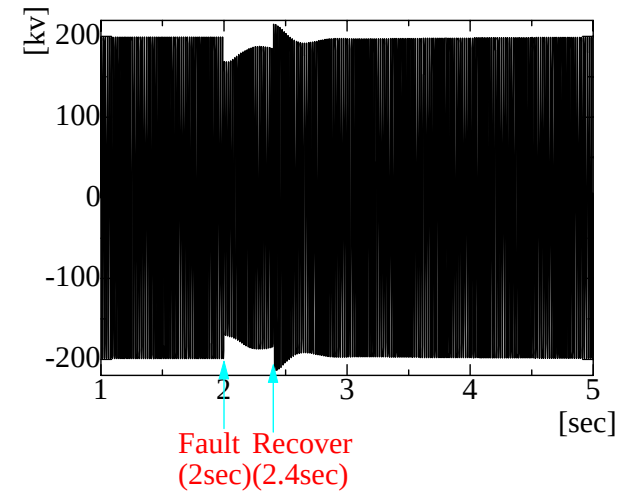
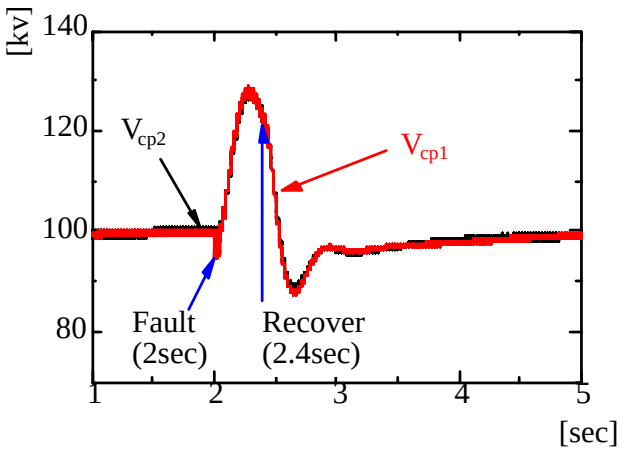


Fig.9 Simulation system with STATCOM installed at the mid-point of long ac transmission line in one line diagram



(a) AC system voltage at installation point



(b) DC capacitor voltage

Fig. 10 Simulation results when AC 3LG fault occurs at remote point

V. SIMULATION RESULTS

Figure 10 shows the simulation results when AC 3LG fault occurs in the ac system shown in Fig.9. AC voltage at the installation point of STATCOM is decreased when the fault occurs. STATCOM using 5-level double converter can recover voltage quickly. Then, dc capacitor voltage is disturbed. To compensate decreased ac system voltage, reactive current must be increased. Therefore, the phase angle δ_B is decreased as seen from the phasor diagram in Fig. 7. Decreasing δ_B means the decrease of output power from the converter B. This cause the charging current from the converter A exceeds the discharging current to the converter B for a while, and the increase of the dc voltage occurs. However the balance between each capacitor is kept well. Total dc voltage is also recovered to its reference value in the short time. Usually, large change of dc voltage is not desirable. However, in this case, the change of dc voltage works to suppress the change in ac voltage. Therefore we suggest to use the dc voltage change for ac voltage change suppression. In steady state operation, reactive power compensation is not required so much, then the phase difference between two converters is set to be certain amount to be able to increase or decrease reactive power. At the same time, dc capacitor voltage is also kept to be much smaller voltage than the rating of the switching device and the capacitor.

VI. CONCLUSIONS

We conclude that these simulation results indicate the good feasibility of multi-level double converter configuration with minimum loss. The controller for dc capacitor voltage balance works well. The controller for total dc voltage seems slower than expected. However, the change in total dc voltage works to suppress the voltage change caused by the disturbance of ac system, when the phase angle difference of two converter is used to control ac voltage.

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VIII. BIOGRAPHIES

Noriyuki Kimura (M'91) was born in Okayama Prefecture, Japan, on October 29, 1953.

He received the B.S., M.S. and Doctor of Engineering degrees in electrical engineering from Osaka University, Osaka, Japan, in 1976,1978 and 1993, respectively.

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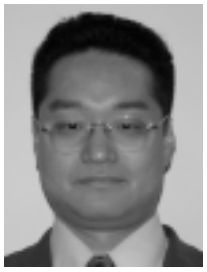

Toshimitsu Morizane (M'94) graduated from Tokyo University, Electrical Eng., in '90 and completed his M.E. program in '92. In '95, he completed his doctoral program, and received Dr. of Eng. from Tokyo University. Since '95 he has been with Osaka Institute of Technology. Currently, he is an associate professor at Osaka Institute of Technology. His research interests are in power electronics and electric machines. He is a member of IEEE and Japan Society for Power Electronics.

Katsunori Taniguchi (M'98) completed his M.E. program at Osaka Prefectural University in 1970, and completed his doctoral program in 1974. He was employed by Osaka Institute of Technology as research fellow, lecturer, associate professor. From 1988, he is professor of Osaka Institute of Technology. Dr. of Eng. His research interests are in PWM inverter/converter, power electronics and motor drive. He is a member of IEEE and Japan Society for Power Electronics.

Takanori Ohno (Nonmember) Takanori Oono was born in Kochi Prefecture on April 25, 1952. He was graduated from Department of Electrical Engineering, Kochi National College of Technology in '73. From '73, He has been with Kansai Power Electric Co.Inc. He is currently a researcher of the Power Engineering Research and Development Center of The Kansai Electric Power Co.Inc. His research interests are in power system analysis.

IX. APPENDIX

Summery of converter parameters are shown in Table A1.

TABLE A1 CONVERTER PARAMETERS

Parameters of Multi-level Converter		
C	1.00E-03	[F]
R	1.00	[ohm]
L	0.10	[H]
Vc	100.00	[kV]
θ_1	36.00	[deg.]
θ_2	72.00	[deg.]
$\sin(\theta_1)+\sin(\theta_2)$	1.54	
δ_A	0.10	[rad.]
δ_B	0.10	[rad.]
Vac=Vr	400.00	[kV]
Vs	415.63	[kV]
Xs	37.70	[ohm]
I_{cp1}	0.65	[kA]
I_{cp2}	1.05	[kA]
I_M	8.27	
A1	1.54	
Total DC-V control		
ω_n	10.00	
ζ	1.00	
K1	3.02E-03	
K2	1.83E-04	
Capacitor Voltage Balancer		
ω_n	16.70	
ζ	1.30	
I_θ	2.53E+00	
K4	1.10E-01	
K5	1.71E-02	