Real-time Simulation of a 48-Pulse GTO STATCOM Compensated Power System on a Dual-Xeon PC using RT-LAB

Christian Dufour, Jean Bélanger

Abstract--This paper reports on the real-time simulation of a 48-pulse GTO STATCOM static compensator with RT-LAB Electrical System Simulator using Linux PC-based, multi-processor technology. The power system has 3 buses and 3 transmission lines and is modeled with SimPowerSystems blockset for Simulink and specialized GTO models that provide an effective method to handle the large number of switches in the STATCOM. Using a 2.4 GHz Dual-Xeon PC running RedHawk™ Real-Time Linux®, the STATCOM and the power system are simulated in real-time with a time step of 36 μs. This paper demonstrates that modern and complex power electronic system controllers can be effectively tested and optimized using affordable and accurate real-time simulation technologies.

Keywords: Real-time simulation, power systems, switch simulation, STATCOM, distributed simulation, RT-LAB, Simulink.

I. INTRODUCTION

Testing, integration and validation of complex controlled systems have traditionally been made in a systematic way consisting of analyzing the behavior of individual components, mostly by simulation, before complete integration on analog simulators or real apparatus. In several cases, the integration was directly made with prototypes of the real equipment. The integration phase required extreme caution due to the power levels; a simple controller malfunction could damage the prototype or the real system, create project delays and even cause personal injuries.

With the increasing complexity and costs of projects, as well as the advances in computer science, it has become advantageous to make more complete and gradual approach during the course of system integration. An excellent way to achieve this goal is to use Hardware-in-the-Loop (HIL) digital simulation. In HIL simulation, an actual controller is connected in closed loop with a real-time virtual plant model of the apparatus it is meant to control. If the apparatus is correctly modeled (i.e. with correct transient and steady-state characteristics), the controller behaves as though it was connected to the real equipment. The controller can be tested for a wide range of parameters and operating conditions without any risk to the apparatus itself.

The authors are with Opal-RT Technologies , 1751 Richardson, Suite 2525 Montreal Qc H3K 1G6 ,www.opal-rt.com
christian.dufour@opal-rt.com jean.belanger@opal-rt.com

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This paper presents the RT-LAB HIL simulator along with a special software toolkit from Opal-RT which were used to perform a real-time simulation of a 48-pulse GTO STATCOM compensated power system on a dual-Xeon PC using RT-LAB.

II. CHALLENGES OF REAL-TIME SIMULATION

Testing electric system controllers with Hardware-in-the-Loop digital simulators is especially challenging as demonstrated in the points that follow.

A. Ability to achieve a very small time step with a power system containing multi-switch devices

Typically, a time step of about 50 μs is required to achieve a good precision to simulate transient phenomenon with frequency components up to 500 to 2000 Hz. The simulation of such transient frequency is important to evaluate the performance of the controller and its firing pulse units under normal, abnormal and fault conditions.

Achieving such a timer step can be problematic when trying to make the real-time simulation of multi-switch devices like static compensator or motor drives. The main challenge comes from the algorithmic problem resulting from switch state modifications. In nodal-based algorithm, a switch conduction change requires the re-triangularisation of the lower *scn*-row of the nodal admittance matrix, where *scn* is the total number of nodes connected to switches (in most implementations of the algorithm). In the state-space implementation of SimPowerSystems (SPS) [4], a switch position change requires the inversion of matrix of rank *ns*, where *ns* is the number of switches in topologically connected subsystem. ARTEMIS [3] plug-in for the SPS avoids this computational pitfall by making pre-computation of circuit's mode equations. ARTEMIS on-line matrix caching options enable the real-time simulation of cyclically switching circuits with very-large number of switches.

Such a small time step value is difficult to achieve with present computer technology because of inter-processors communication latency, especially between processors and I/O systems. DSPs or costly special hardware and computers are often required to achieve this small time step for complex power systems. It was however demonstrated that Off-the-Shelf PC-based simulators like RT-LAB [1] or others [14] can achieve time step value below 50μs for systems of moderate size up to 10-50 buses and power lines.

A time step of 50 μs may be adequate for typical power systems equipped with power electronic systems with switches commutating at the line frequency such as the current GTO-based STATCOM application. However, a time step value lower than 10 μs is necessary to accurately simulate small PWM power electronic systems with PWM carrier frequency up to 10 kHz. Opal-RT and Mitsubishi Electric Corporation recently reported that they achieved the Hardware-In-the-Loop simulation of a single PMSM motor with AC-link diode rectifier at a 10 μs time step [12]. A standard dual-Xeon shared-memory computer interfaced to a controller with reprogrammable FPGA I/O was used.

B. Prevent the generation of non-characteristic harmonics

The firing pulses generated by an actual controller connected to the simulator are asynchronous with the simulator itself. This means that turn-on and turn-off commands occur randomly between the simulator sampling times. If the simulator does not handle these asynchronous events correctly, it will introduce non-characteristic harmonics and non-linearities that do not exist in real life. This spurious noise can be modulated and fed back to the controller under tests which then leads to erroneous results and phenomena which are often difficult to distinguish from phenomena generated by a bad controller design. Several interpolation and compensation techniques have been successfully applied to solve these problems for well-known simulation packages[6]. This has also been demonstrated for applications such as large induction motor HIL simulator [11], fuel-cell hybrid electric vehicle HIL simulator [7][8][9], doubly fed induction motor for wind turbine applications [10] and onboard DC power system for vehicular applications [13] to name but a few.

C. Numerical stability and efficiency

Another challenge in making real-time simulation of electric circuits is that its elements are usually tightly coupled. As such there is no easy way to simulate the complete circuit by simple connection of the circuit sub-components because of causality problems. Relatively complex algorithms like EMTP [5] and state-space formalism of the SimPowerSystem blockset (SPS) for Simulink and ARTEMIS solve this causality problem. It happens that non-derivative fixed causality models can effectively describe most voltage source inverter applications. This enables us to avoid the numerical problem of having to invert or retriangularize large matrix in the real-time loop. This also enables the implementation of very effective interpolation methods that improve overall simulation accuracy.

D. Scalability

A simulator should be scalable in terms of computational power to enable the simulation of larger power systems as these are needed to analyze the interactions between several power electronic control systems and the power system itself. The simulator scalability is achieved by distributing the simulation execution over several processors as the simulated network becomes more complex. This is achieved by breaking up the network into several loosely linked networks taking advantage of transmission line delays and slowly varying state-variables. Special care must however be taken in the selection of the inter-processor communication system to prevent excessive communication delays, which limit the minimum time step achievable.

III. THE STATCOM DEVICE

The static compensator (STATCOM) is a device used to regulate voltage and improve dynamic stability of power systems. GTO-based STATCOM are multilevel line-commuted voltage-sourced inverters that are shunt-connected to a power system bus through a set of transformers.

Fig. 1 depicts the 3-level inverter-based STATCOM construction tested. The STATCOM is built with four 3-phase 3-level inverters coupled with four phase shifting transformers introducing phase shift of +/- 7.5°. This transformer arrangement neutralizes all odd harmonics up to the 45th harmonic, except for the 23rd and 25th harmonics (for a perfectly balanced network). Those two harmonics are minimized choosing an appropriate conduction angle for the three-level inverters (σ= 172.5°).

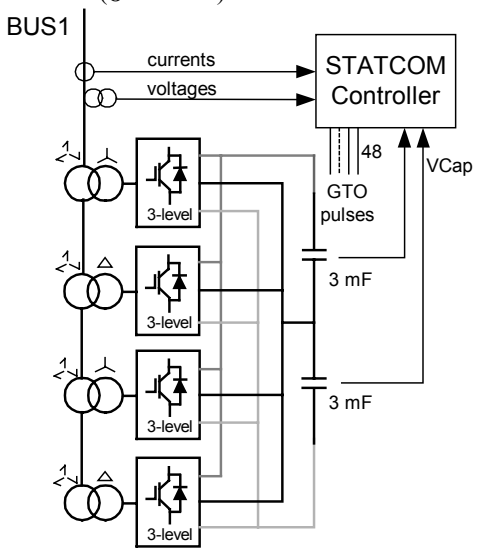

Fig. 1. STATCOM internal configuration

The STATCOM active and reactive power flow equations are governed by the well-known equations:

$$P = \{V_s V_b \sin(\delta)\} / X \qquad (1)$$

$$Q = \{V_s^2 - V_s V_b \cos(\delta)\} / X \qquad (2)$$

where *Vs* and *Vb* are respectively the positive sequence voltage amplitudes at the GTO-side of the STATCOM and bus-side, δ is the angle between the 2 voltages and *X* is the impedance of the STATCOM transformers. By controlling the amplitude and phase of the STATCOM generated voltage and with the knowledge of bus voltage and transformer impedance, one can control the active and reactive powers injected into the bus. By controlling the amplitude of the STATCOM-side voltage, one controls the reactive power

flow and the line voltage. The DC-link voltage in turn controls this voltage amplitude in the GTO-based STATCOM. So, to change the reactive power flow of the STATCOM, the controller must temporarily initiate an active power flow to the capacitor to change its voltage. This active power flow is controlled by shifting in time the GTO pulses and therefore STATCOM-side voltage.

The effect of a STATCOM device on a network can be viewed by a simple test on the 3-bus test network as depicted in Fig. 4. In the test, voltage sag of +- 4.5% is made by the 8500 MVA network equivalent source. Fig. 2 depicts the BUS1 voltage (the STATCOM point of connection) when the STATCOM is present (solid lines, all solvers) and when it is not present (dotted line). The voltage variation is attenuated by the STATCOM. Fig. 2 also shows the reactive power output of the STATCOM during the test run.

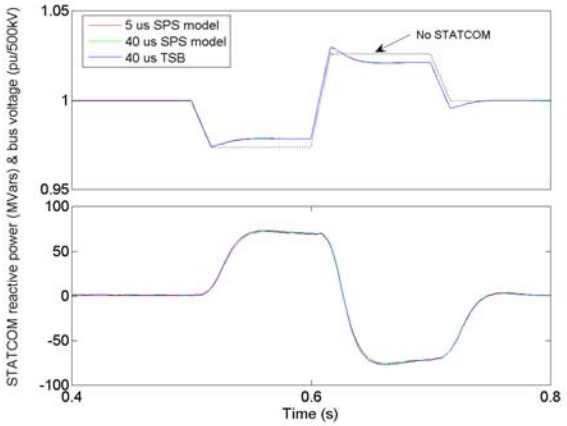

Fig. 2. STATCOM bus voltage with and without STATCOM during voltage sag

IV. THE RT-LAB REAL-TIME SIMULATOR

The RT-LAB Electrical System Simulator used for the real-time simulation of the STATCOM compensated power system is depicted in Fig. 3. It is made up of a console PC running Windows XP for result visualization and on-line parameter control and a dual-Xeon shared-memory PC running at 2.4 GHz under RedHawk RT-Linux operating system (QNX operating system can also be used) .

The real-time model tasks separation of the STATCOM compensated power system is depicted in Fig. 3. The computational tasks are distributed as follows: CPU1 of the dual-CPU computer handles the internal STATCOM controller equation (for the fully numerical simulations explained in this paper) while the CPU2 computes the STATCOM model, BUS2 and BUS3 equations as well as the transmission line propagation equations. BUS2 and BUS3 equations can be placed on a different CPU than the STATCOM (by virtue of the ARTEMIS decoupling line models) but it happened that the controller is the biggest computational task of all. In the case of HIL testing with real external controllers, the CPU in charge of the STATCOM model also controls the FPGA I/O card that reads GTO gate signals generated by the real controllers and generates the voltage and current analog signals needed by the controller. Digital signal generation and sampling are both obtained using 10 ns resolution. The Opal FPGA card, built around the Xilinx Virtex-II Pro also controls fast 16-bit D/A and A/D converters.

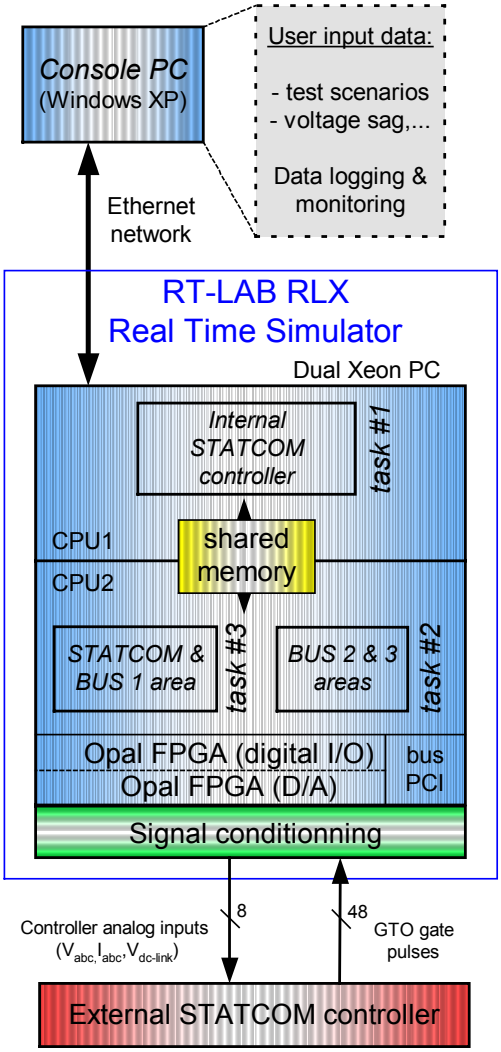

Fig. 3. The RT-LAB simulator and STATCOM system task separation

A Windows console is used to set-up various test scenarios or evaluate controller performance for different system disturbances, operating conditions and system/controller parameters.

If necessary, the computational tasks can be distributed across several PCs to decrease the simulation time step or to simulate more complex systems. Inter-computer communication systems supported by RT-LAB are FireWire 800-Mbits/s as well as SignalWire™ , which is an FPGA-based fast serial communication link capable of delivering up to 1.25 Gbit/s transfer rates, with a latency of 200 ns. With SignalWire links one can run distributed simulations of larger networks on PC-clusters at sample times as low as 10-20 μs. InfiniBand® adaptor and switches (10 Gbits/s full duplex per adaptor) are also supported for large clusters.

V. STATCOM & TEST NETWORK DESCRIPTION

The STATCOM compensated power system is depicted in Fig. 4. This power system has 3 buses and 3 power lines and the STATCOM device is connected to BUS1. The network is also made up of 3 ideal inductive sources.

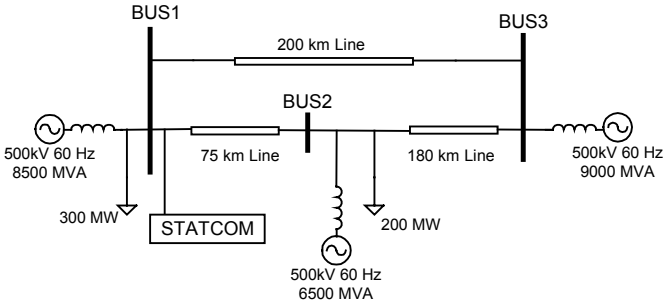

Fig. 4. STATCOM test network

VI. THE TIME-STAMPED BRIDGE MODELS

The STATCOM model uses special GTO models called Time-Stamped Bridges and part of the RT-Events library from Opal-RT Technologies. Time-Stamped Bridges (TSB) use a real-time interpolation technique and assume continuous load conduction. Similar to what can be found in EMTP and SimPowerSystems, switches are modeled with two conduction states with ON resistance and voltage offset.

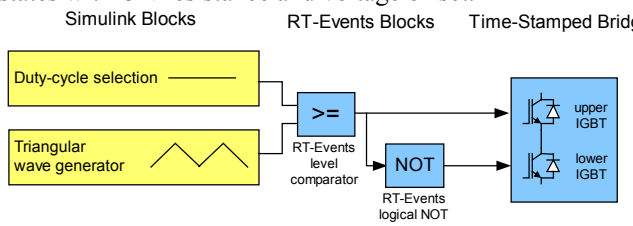

Fig. 5. Simulink blocks, RT-Events logical blocks and Time Stamped Bridge interconnection (PWM generation example).

The TSB can model GTO, MOSFET, IGBT and IGCT legs accurately including dead time effects as low as 1 μs, which is much lower than typical simulation sample times[12]. The GTO models connect directly to gate signals coming from Digital Inputs (in HIL mode) or to RT-Events blocks if the interpolated gate signals are generated from within Simulink (Fig. 5).

VII. VALIDATION TESTS

In this section, we validate the Time-Stamped Bridges (TSB) model by comparing the STATCOM network response against a conventional fixed step method GTO models, namely SimPowerSystems (SPS), running at a very small time step (5 μs). The validation is made at a time step of 40 μs, near the expected sampling time on the real-time simulator. The internal controller running with 40 μs sample time is used in all cases including the reference 5 μs runs.

As the main usage of the real-time simulator is to interface it to a real controller, the voltages and currents at the STATCOM controller connection points are of prime interest for this validation.

A. 3-phase fault to ground at BUS3

This test makes a 3-phase to ground fault at BUS3 for 5 cycles. For all practical purposes, Fig. 6 shows that the 40-μs TSB simulation has the same precision than the SPS at 5μs. For all simulation runs, the fault causes an 18% over-voltage and 100% over-current.

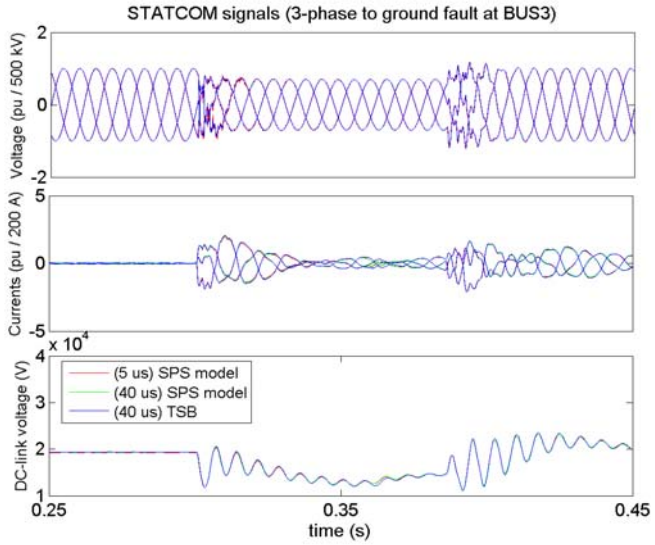

Fig. 6. STATCOM signals during 5-cycle 3-phase fault.

B. Single phase to ground fault au BUS1

This test makes a single-phase-to-ground fault at BUS1 for 5 cycles. This time, some differences appear between the 5 μs reference run vs. TSB and SPS runs at 40 μs.

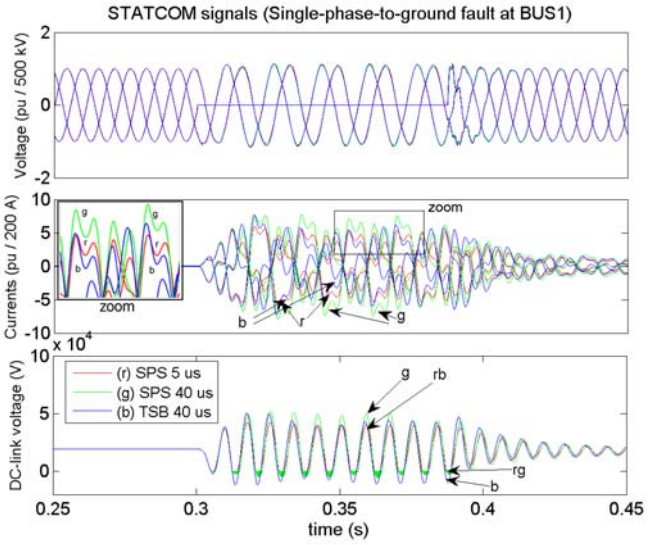

Fig. 7. STATCOM signals: 5-cycle phase-to-ground fault au BUS1

The simulation results are shown in Fig. 7 The peak currents in TSB run are in average 20% lower than reference while the 40 μs SPS currents are 40% higher than reference. The DC-link capacitor voltage has over 100% over-voltage during the fault and shows some slight errors for both 40 μs runs vs. reference one. The various ARTEMIS solvers had no effects on this error. A lower time step could improve the precision with all solvers tested.

C. Harmonic analysis of STATCOM currents

The impact of interpolation in fixed step simulation can be observed in the frequency domain [6]. In this test, the 8500 MVA source was lowered in amplitude to set the STATCOM output to 0.7 PU of current. The steady-state current was then analyzed in the frequency domain with a FFT. In Fig. 8, the expected 23rd and 25th harmonics are present in the FFT but there are spurious harmonics at 260 Hz and 380 Hz that do not correspond to any harmonic number (note however the 120 Hz difference). Changing the time step to 30 μs or 35 μs does not affect the 23rd and 25th harmonics but causes the spurious ones to shift in frequency, always below 1 kHz, in a behaviour not fully understood by the authors. Fig. 8 shows that the TSB interpolation reduces the amplitude of those non-characteristic harmonics with equal time step (25 μs). A 7 μs time step makes the spurious harmonics disappears.

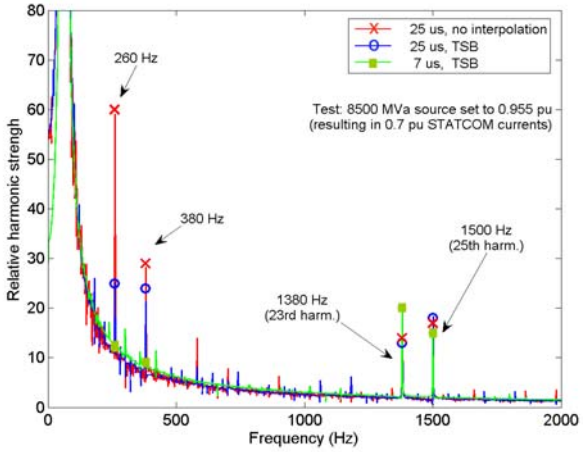

Fig. 8. Frequency spectrum of STATCOM current

D. Test on the Numerical precision of Time-Stamped Bridges

Fig. 9 shows the 2nd harmonic component that is present at DC-link capacitor in steady state. This component is generated by the controller Park conversion. With Time-Stamped Bridges, this component is attenuated by comparison to SimPowerSystems conventional fixed-step simulation with the same time step. In the figure, one can observe that the simulation with SPS at 50 μs (trace *b*) has a larger amplitude and jitter than a simulation with SPS and TSB-modelled STATCOM (trace *c*) at 50 μs. The same can be said when the simulation time step is lowered to 25 μs. Simulations with a 5 μs second time step for both the controller and the system result in a similar DC-link oscillation than the 25 μs run with TSB. The low frequency jitter of the non-compensated simulations probably has a similar cause than the STATCOM current spurious harmonics found in the previous test (Section C) .

The interpolation benefit of the TSB is more obvious in PWM applications [9][6][13][12][8] because there is much more commutations per unit of time (and therefore fixed step time framing errors) occurring in those applications than in the GTO-based STATCOM where each GTO commutes at the line frequency. The main advantage of the TSB for the STATCOM simulation is it computation performance as discussed in the next section.

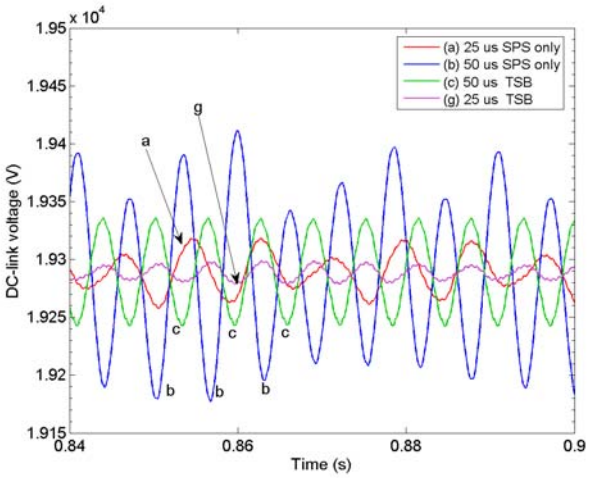

Fig. 9. DC-link in steady-state with 120Hz component

VIII. REAL-TIME COMPUTATIONAL PERFORMANCE

The STATCOM network has been simulated on a dual-Xeon shared-memory PC running RT-LAB 7.1 under the RedHawk RT-Linux operating system.

TABLE I
HARD REAL-TIME COMPUTATIONAL SPEED ON DUAL-XEON 2.4 GHZ

SimPowerSystems (with ARTEMIS) network + Time Stamped Bridge for STATCOM switches	36 μs
SimPowerSystems only	340 μs

In Table 1 the results show us that the simulation of the TSB-modelled STATCOM switches with SimPowerSystems (with ARTEMIS) modelled power network is about 10 times faster than if the entire system, including the STATCOM switches, is modelled with SimPowerSystems. No I/O were used in the test. Recent advances by Opal-RT on reconfigurable FPGA-based I/O technologies considerably reduce the I/O impact on timing. [12][9].

The TSB-modelled STATCOM network takes only 21 μs to execute. The numerical controller is the most demanding task of the system, taking 25 μs to execute; replacing it by an HIL controller can reduce the timing. Computational spikes due to a rank-36 (3 switches per IGBT legs in SPS algorithm) matrix inversion, that occurs when a switch conduction state is modified, prevent the use of SimPowerSystems from achieving real-time simulation. Nodal based methods may prove better at this task as they would require re-triangularisation of the lower 15 rows (number of nodes connected to GTOs in the model) of the admittance matrix for most nodal algorithm implementations.

A. Parameter optimization batch testing with TestManager

This 10-fold increase in computing speed can be used to make system parameters optimisation in batch testing (with switched system, this acceleration factor can reach 1000 when compared with variable-step solver based software package like Simplorer). For example, batch testing can be used to

investigate the influence of the DC-link capacitor value, which has an important effect on fault (A-B BUS3) currents values. The maximum phase-to-phase fault current was automatically scanned with regards to the DC-link capacitor values. Fig. 10 shows that the over current is diminished with a 1 mF capacitor instead of the 3 mF SimPowerSystems demo value.

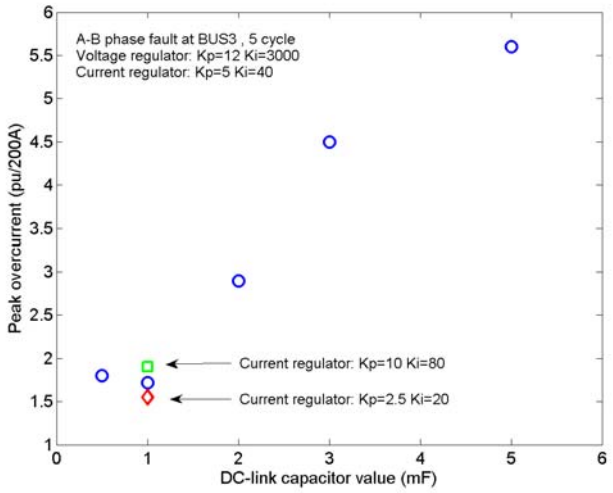

Fig. 10. Effect of DC-link capacitor value on phase-to-phase fault over-current

Considering the infinite number of fault types and component parameters in a typical power system, this kind of batch testing optimisation is best made with proper test managing and archiving software like TestManager from Opal-RT or TestStand from National Instruments in conjunction with RT-LAB as simulation accelerator.

IX. Conclusions

We have demonstrated the ability of RT-LAB to simulate a small network with 48-pulse GTO-based STATCOM. The STATCOM is modelled with Time Stamped Bridges models. These interpolating bridge models have the main advantage of avoiding the computational burden related to switch conduction change found in the nodal method of EMTP or state-space approach of SimPowerSystems. Several validation tests, such as faults, were conducted to validate the accuracy of the proposed method. The most severe validation test (phase-to-ground fault at the STATCOM) had a precision compatible with controller HIL testing.

The suggested interpolating bridge models were also demonstrated to improve the fidelity of the simulation in the frequency domain by diminishing the creation of non-characteristic harmonics by the fixed step simulation process. The real-time simulation of the complete STATCOM system with TSB-modelled switches was made at 36 μs on the RT-LAB platform, which is sufficient for the controller performance testing. Decreasing the time step to about 20 μs by using faster 3.8-GHz processors and a third processor to simulate the controller could increase the simulation precision.

Distributing the network tasks on a larger PC-cluster would enable us to increase the simulation accuracy by lowering the time step. A distributed network can also be used to simulate much more complex power electronic systems with time step ranging between 20 μs and 40 μs, depending on the processor number and speed used.

X. References

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XI. Biographies

Christian Dufour is a Simulation Software Specialist at Opal-RT Technologies. In 2000 he received his Ph.D. degree from Laval University, Quebec. In 1992 he began working on the development of IREQ real-time simulators as well as the MathWorks' SimPowerSystems blockset. His current research interests are mainly focused on numerical techniques related to real-time simulation of power systems and motor drives.

Jean Bélanger is the president, CEO and founder of Opal-RT Technologies, Inc. He is a specialist in real-time simulations, with more than 25 years of experience in the field, including many years as part of the simulation division of Hydro-Quebec where he helped developed the world's first 735 kV power transmission systems. He received his M.Sc. from Laval University, Quebec. In 2001, Mr. Bélanger became a fellow of the Canadian Academy of Engineering in recognition of his outstanding professional achievements.