PC-Cluster-Based Real-Time Simulation of an 8-synchronous machine network with HVDC link using RT-LAB and TestDrive

Christian Dufour, Jean-Nicolas Paquin, Vincent Lapointe, Jean Bélanger, Loic Schoen

Abstract—In this paper, we detail the real-time simulation results of a medium-sized network composed of 8 synchronous machines and an HVDC link. The model is composed of two Kundur-like 4 machines networks connected together with a 12-pulse HVDC link.

The complete network is modeled with SimPowerSystems with ARTEMIS real-time plug-in and is simulated in real-time on a RT-LAB InfiniBand PC-cluster composed of 3 dual-CPU dual-core Opteron PCs.

The network model includes the HVDC control and protection systems as well as the synchronous machine regulators and power stabilizers. It also includes typical fault simulation capability like HVDC DC faults, thyristor misfires and AC faults. This model is excellent to study the complex interactions between an HVDC link and AC network under normal and transient conditions.

The real-time simulation is controlled and monitored with a TestDrive interface from Opal-RT. This interface, based on LabView, permits easy monitoring and control of the complete system and enables Python-based scripting for automated tests. The proposed simulator can be interfaced with external equipments and controllers by direct reconfiguration of a FPGA I/O card with Xilinx System Generator blockset.

Keywords: real-time simulator, power system stability, HVDC link, FACTS devices, FPGA-based I/O, SimPowerSystems, Xilinx System Generator.

I. Introduction

TO reduce risk during the control development phase and before final system commissioning, it is now common and mandatory practice to test, under steady-state and transient operating conditions, power grid systems such as high-voltage direct current (HVDC) networks, static VAR compensators (SVCs), static compensators (STATCOMs) and other FACTS devices [1][2][3][13]. Hardware-in-the-loop (HIL) testing, where a controller is connected to a real-time simulator in a closed loop, is first performed with a prototype controller and, after that, with the real production controller. Several thousand systematic and random tests are often required to verify performance under various operating conditions and to detect instabilities. An HVDC link will also be a source of concerns for the electro-mechanical stability of the network it is connected to. A fault on an HVDC network will induce power flow fluctuations and the proper choice of power system stabilizers is important[4].

Another important aspect is the choice of simulation software used for this kind of study. RTDS and HYPERSIM are examples of real-time simulators based on EMTP algorithms. EMTP[5] is a widely used power system simulation software that has a proven track record of accuracy, while SimPowerSystems (SPS) is a rather new simulation package that has been demonstrated to be as accurate as EMTP.

Recently, there have been important efforts to make real-time power grid simulators based on Simulink and SPS. Simulink has emerged as a worldwide standard for scientific computing and it is only natural to extend it to real-time simulation. The major advantage of using a Simulink-based real-time simulator is that it enables the user to make its complete model design in Simulink and using all its toolboxes. On the other hand, one of the drawbacks of SPS and Simulink is that it offers so much flexibility with regards to models and solvers that inexperienced users may not know how to use the best options. For example, using variable time step solvers can be tricky and results in very long simulation times, especially when PWM converters are present. SPS is also designed to be a general-purpose electric simulation program and is not optimized for hard-real-time simulation performance. ARTEMIS real-time plug-in to SPS solves these problems by making the necessary optimizations.

This paper presents such an SPS-based real-time power system simulator called RT-LAB RTeGrid and its usage to study an 8-synchronous machines network with 12-pulse single-pole HVDC link. The network will be simulated in real-time using a cluster of PC (dual-core dual-Opteron) connected with an InfiniBand switch.

The objective of this paper is to demonstrate a real-time power system simulator with the following characteristics:

- **Scalability**: the use of an ultra-fast InfiniBand switch permits the clustering of a large number of PCs, virtually eliminating hardware limits on the size of power network that can be simulated

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- **Full Simulink integration**: the simulator only requires Simulink from initial off-line test to HIL simulation. Even the I/O can be reconfigured by the user with Xilinx System Generator for Simulink, which is now supported in RT-LAB
- **SimPowerSystems real-time customization**: the RTeGrid simulator comes with special toolboxes, namely ARTEMIS and RteDrive, to optimize SPS algorithms for real-time simulation usage.
- **Variety of user interfaces and automated test technology**. The TestDrive interface provides a fully reconfigurable user interface with on-the-fly signal selection and Python-based scripting capabilities for automated testing. The RT-LAB API can also be interfaced with most third party GUIs like NI and Altia.
- **Commercial-Of-The-Shelf paradigm**: RT-LAB hardware is mostly based on COTS components (standard PCs, InifiniBand switch, etc..) to benefit from rapid advancements in technology and limit upgrade costs. Real-time operating systems are also COTS-type namely QNX and RedHawk-Linux.

II. REAL-TIME GRID SIMULATOR DESCRIPTION

A. Real-time simulation tools and algorithms

The RT-LAB RTeGrid real-time simulator from Opal-RT Technologies uses a set of Opal-RT tools especially designed to optimize real-time performance of electric system and drive applications. These tools work with MathWorks Simulink software and with Simulink toolboxes like the SimPowerSystems (SPS) block set. These tools include:

1- **ARTEMIS**, a real-time enabler for SPS;

2- **RTeDrive**, a specialized block set for the simulation of power inverters;

3- **RT-Events**, a block set to design simulation models for firing pulse units; and

4- **Xilinx System Generator (XSG)**: RT-LAB now support XSG to allow users to fully simulate and program custom FPGA applications on the I/O cards

1) ARTEMIS: The main algorithm used in the RT-LAB Power Grid Simulator is the Opal-RT ARTEMIS plug-in for SPS. ARTEMIS enables real-time simulation for SPS models by pre-calculating system equations, provides a set of special discrete solvers to improve discretization stability, and facilitates network equation decoupling. The main solvers of ARTEMIS are based on L-stable approximations of the matrix exponential. L-stability is an extension of A-stability in which most numerical oscillations are naturally suppressed[7][8][9].

ARTEMIS comes with a library of decoupling elements to help parallelize network state-space equations. This decoupling can be natural, as with Bergeron traveling-wave power lines that have inherent delays built into their model. The decoupling can also be artificially added to a model by substituting transformer secondary inductance with a stubline having a propagation time equal to a single time step and with the same total series line inductance..

2) RTeDrive: Voltage source inverters are best modeled using a specialized blockset from Opal-RT called RTeDrive. This blockset includes special interpolating inverter models for IGBTs, MOSFETs, and GTOs. It is used to very effectively and precisely model most types of voltage inverter-based systems, like IGBT drive systems and IGBT/GTO/MOSFET-based power systems like STATCOMs[6][10].

3) RT-Events: For high-frequency devices like PWM modulators, the RT-Events blockset provides a way to make accurate, fixed-time-stepped, Simulink-based simulations. High-frequency PWM modulators for electric devices typically run with kHz-range carriers. This is problematic in a fixed-step simulation scheme because a zero-crossing event cannot be accurately determined. To compute such events and to obtain accurate simulation results, RT-Events uses interpolation methods similar to those used with RTeDrive.

4) Xilinx System Generator (XSG): This blockset enables users to fully simulate and program an Opal-RT FPGA card without any knowledge of VHDL languages. The RT-LAB XSG environment provides the user with easy-to-use XSG blocks to connect FPGA logic to the various I/Os of an Opal-RT FPGA card. Complex applications like a PMSM drives can also be implemented on the FPGA using XSG[11].

B. Real-time simulation hardware

The RTeGrid simulator used in this paper is based on RT-LAB, a real-time simulation platform from Opal-RT Technologies.[12][14][16] The RT-LAB runs almost entirely on commercial-off-the-shelf hardware. The only exception, because of the extreme I/O requirements for electric drives and system applications, is the Opal-RT FPGA-based I/O card, which is now user programmable with XSG. RT-LAB supports distributed simulation through shared memory with multi-CPU, multi-Core, AMD- or Intel-based systems and with PC clusters with FireWire and InfiniBand communication links. RT-LAB currently supports the InfiniPath adapter from PathScale. InfiniPath is an InfiniBand-compatible adapter used for PC cluster communication and has a 0-byte-half-trip latency as low as 1.3 microseconds.

Opal-RT FPGA I/O cards feature 10 ns digital I/O, 1 microsecond D/A converters, and 2-microsecond A/D converters. The support of Xilinx System Generator (XSG) blockset in RT-LAB enables users to fully customize I/Os for Opal-RT FPGA cards. RT-LAB also support more than 50 third-party I/O boards from companies like Acromag, DDC, Kronton, Measurement Computing, National Instruments, Quanser and Sensoray.

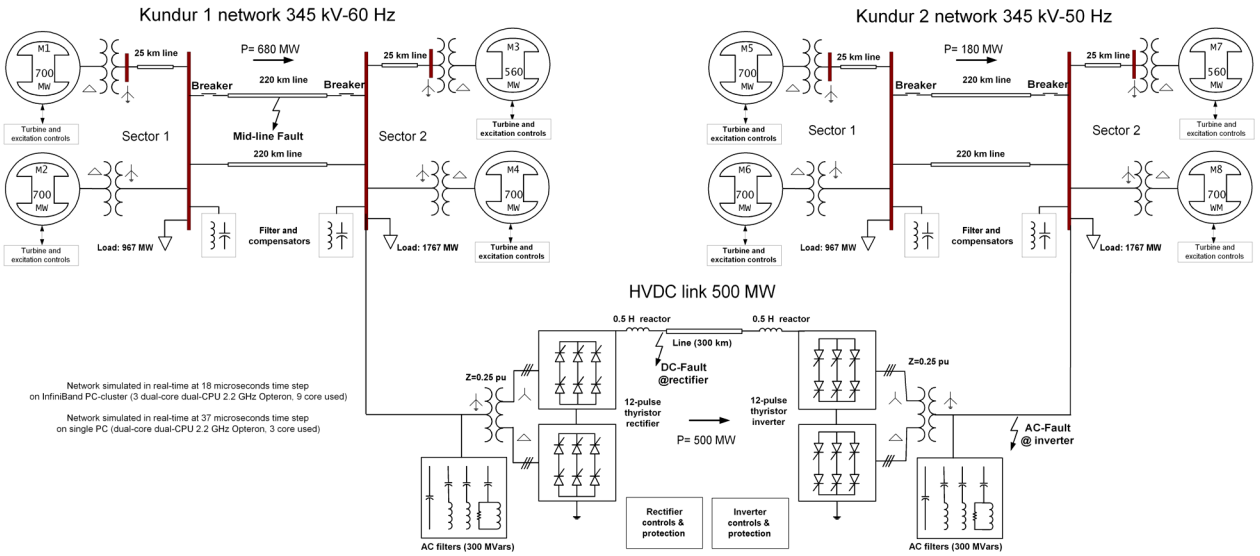

Fig. 1. Eight-synchronous machine network with 12-pulse single-pole HVDC link

III. TESTS

In this section, we show the results of tests done with the real-time simulator on the 8-synchronous machine HVDC system depicted in Fig. 1. The entire network is composed of 3 parts: two Kundur-like 4-machine networks with complete alternator models with mechanical part (tandem-compound steam prime mover system, speed regulator, steam turbine and shaft) and excitation systems (IEEE type 1 synchronous machine voltage regulator) and a 12-pulse HVDC link with filters and various controllers. The Kundur models also include power system stabilizers. Both the Kundur and HVDC models are freely inspired from available SPS demo models[15].

The following tests have been performed: 1) Mid-line 3-phase fault on the Kundur 1 network and 2) HVDC rectifier DC fault. Both tests are applied from the power system steady state operating point.

A. Test 1: Mid-line 3-phase fault on Kundur 1 network

In this test, we apply a 3-phase fault at the mid-point of one of the 2 inter-sector transmission lines, which causes, 8 cycles later, the line breakers opening. The fault is cleared 0.2 sec after it is applied and the line is reconnected again 5 sec. after the beginning of the fault.

The fault does not cause instability of the Kundur networks. As expected, the fault has a much more important impact on the Kundur 1 network as seen by observing the machine angles (Fig. 2). On Fig. 3, one can observe that the Kundur 1 voltage always stays above 0.6 pu and therefore the DC-link voltage stay above the HVDC controller Voltage Dependant Current Order Limiter's (VDCOL) DC voltage threshold (0.6 pu). The DC current reference is therefore kept to its nominal value of 1 pu. Moreover, Fig. 4 shows that the DC current and voltage are shortly disturbed and so the DC power is quickly reestablished without commutation failures.

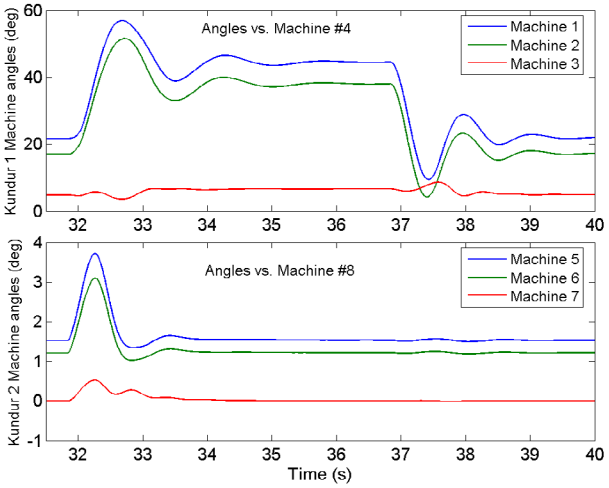

Fig. 2. Kundur 1 & 2 machine rotor angles during Test 1.

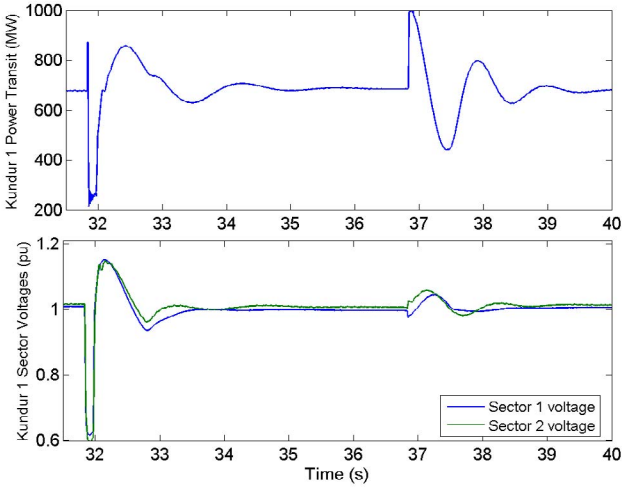

Fig. 3. Kundur 1 power transit and sector voltages during Test 1

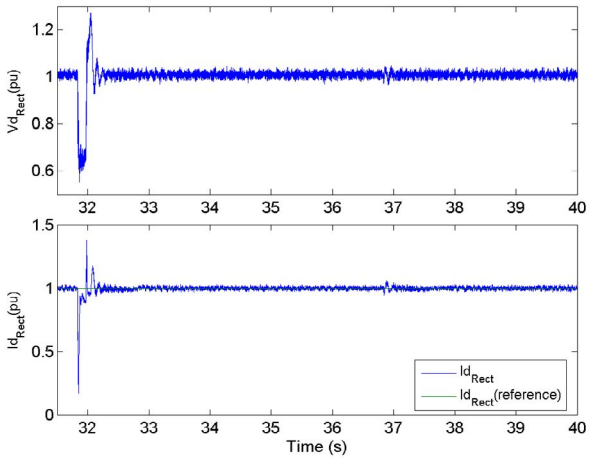

Fig. 4. DC-link current and voltage during Test 1

B. Test 2: Rectifier-side HVDC DC-fault

In this test, a DC-fault is applied to the DC-link at the HVDC rectifier-side. Basically, during a DC-fault, the HVDC controllers try to lower the power transit to manage the fault clearance then reestablish the HVDC link's nominal conditions. Several problematic can be studied here like AC-bus over-voltage that can cause HVDC transformer saturation, inducing harmonics and VCO problems. DC-link current amplitude is also under investigation during this test.

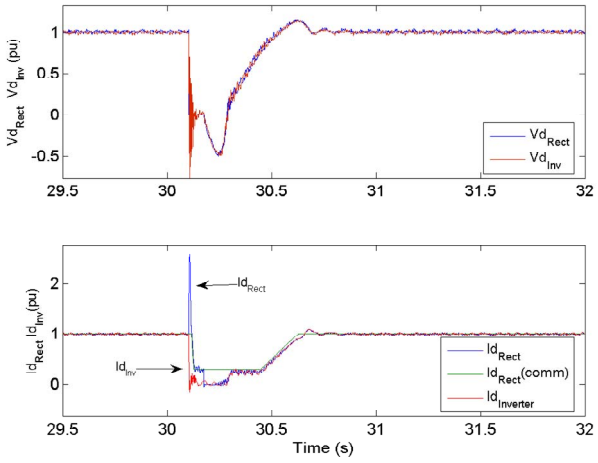

Fig. 5. HVDC link voltages and currents during Test 2

As shown on Fig. 5 and Fig. 6, the DC fault causes the DC voltage to instantly drop to 0 pu and therefore leads the rectifier side DC current to the minimum reference value given by the VDCOL(0.3 pu). This quasi-instant lowering of the current reference also helps limit the maximum rectifier side transient DC current to 2.5 pu. Shortly after, when the DC-fault is detected, the HVDC rectifier-firing angle is forced to its maximum value, which leads it in inverter operation. Consequently, the DC line voltage becomes negative causing the rectifier side DC current to collapse. The power transit is then reestablished by control actions.

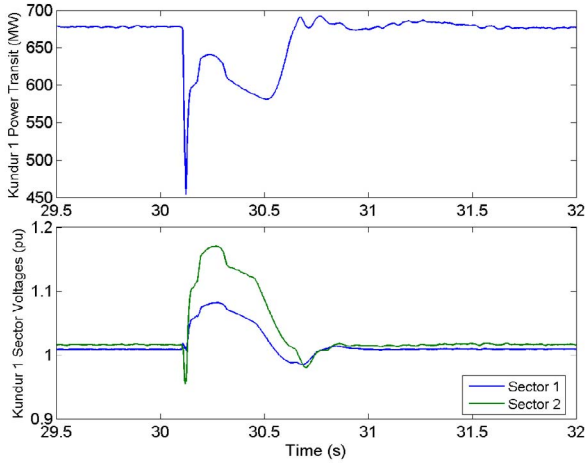

Fig. 6. Kundur 1 power transit and sector voltages during Test 2

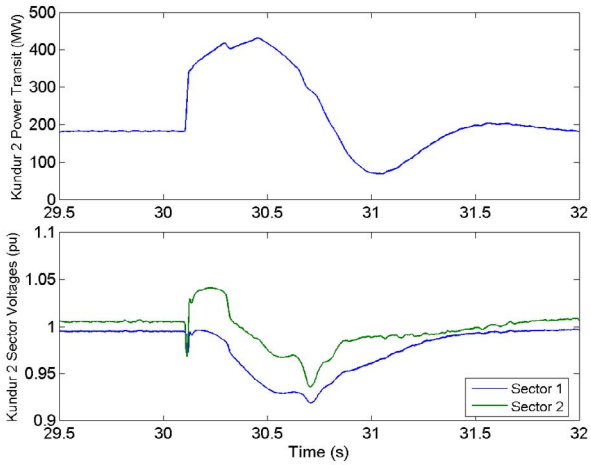

Fig. 7. Kundur 2 power transit and sector voltages during Test 2

IV. Real-Time Simulation Performance

The real-time simulation of the 8-machine HVDC network has been performed on an RTeGrid simulator composed of 3 dual-core dual CPUs Opteron 2.2 GHz PCs (12 cores in total) connected with the InfiniBand switch. For the test, the 8-machine HVDC system was decomposed into 9 computing tasks running in parallel: each sector of the Kundur networks (4 tasks), each side of the HVDC link including the filter (2 tasks) and both Kundur and HVDC controllers (3 tasks). Table 1 shows that the complete systems runs in a hard real-time step of 18 microseconds (without I/O). In comparison, the same model runs 800 times slower on a Windows-based PC in regular Simulink simulation.

Table 1 Simulation Results Summary

RTeGrid **hard real-time** simulation time step on InfiniBand Cluster (3 Dual-core dual-CPU Opteron 2.2 GHz, 9 core used only)	18 μs
RTeGrid simulation acceleration factor vs. Windows-based **offline** simulation of Simulink/SPS (Pentium 4, 3 GHz, 1.2 GB RAM	800

V. TESTDRIVE GRAPHICAL INTERFACE

The graphical interface of a real-time simulator is also very important. Simulink interfaces (scopes, dials, etc.) can quickly become inadequate on complex problems like power grid tests. For example, in repetitive fault tests, it is desirable to have the display of certain data triggered on faults. TestDrive software from Opal-RT has an interface based on LabVIEW software from National Instruments and can also be scripted using Python. TestDrive uses the LabVIEW runtime engine, enables users to build on-the-fly LabVIEW displays and controls panels by virtually wiring real-time simulation signals to graphical displays. TestDrive also has built-in display triggering capability that enables the display of complex waveforms in real-time and the synchronization of those waveforms to specific events like a fault or control signal step.

For controlling and monitoring real-time simulations, the TestDrive interface has the following advantages over standard Simulink:

- Easy, point-and-click dynamic selection of signals to view
- Synchronous display of data on triggered events
- Easy management of multiple windows for control signals and acquisition data
- Built-in Python scripting tool for designing test suites
- Ability to use advanced graphical features of LabVIEW

Fig. 8 shows the main TestDrive interface window in which the real-time simulation signals are displayed in the right part of the window. The figure shows the interface in its signal selection mode. In this mode, all signals coming from the real-time simulation are listed in the middle part of the window. The user can select a signal by simply clicking on it and assigning it to one of the scopes on the right side of the window.

The left of the TestDrive interface displays a list of available display/control panels (e.g., scopes) for signals. The **HVDC Control** (Fig. 9) is an example of dialog boxes to control the fault and test signals (AC faults, DC faults, and small signals perturbations).

An important aspect of convivial fault study simulations is the ability to synchronize the simulation results on the fault itself so that the display does not "move". This enables a user to vary simulation parameters (e.g., network impedance) and dynamically observe the effect of varying these parameters (e.g., DC-link recovery time, modes, etc.)

The infinite test possibilities, contingencies, and network configurations possible require effective test managing software for optimization and Monte Carlo studies. Opal-RT's TestManager or National Instruments' TestStand can be used to design test suites and generate test reports automatically. Similarly, the top-left part of the TestDrive interface contains controls to launch Python-based scripts acting on the real-time simulation process. The TestDrive scripting language uses Python aliases to simplify the programming for the user. For example, the following lines implement a hypothetical loop on a **Ki_RectVoltage** variable:

```
for value in range(10,10,1000):
    Set("Ki_RectVoltage",value)
    Log("Setting Integral Gain of Rectifier
        voltage regulator to %f" % value)
Wait(1000)
```

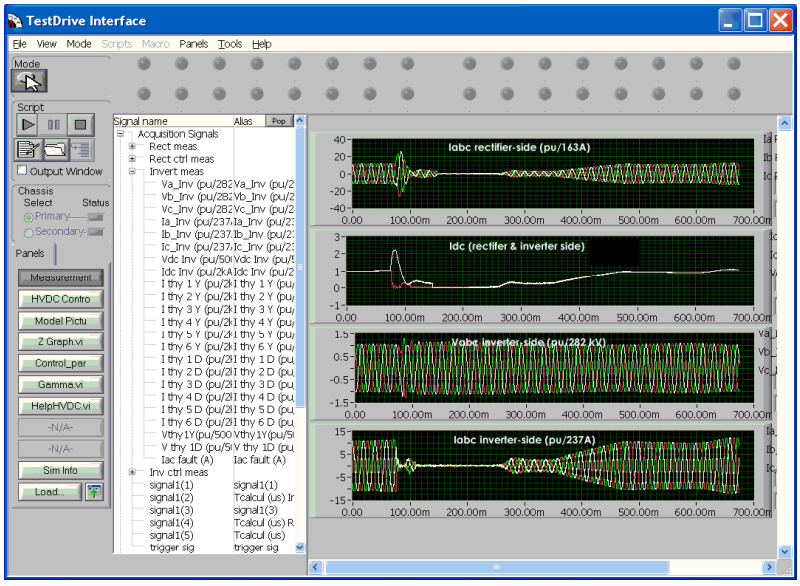

Fig. 8. Main TestDrive panel in signal assignment mode

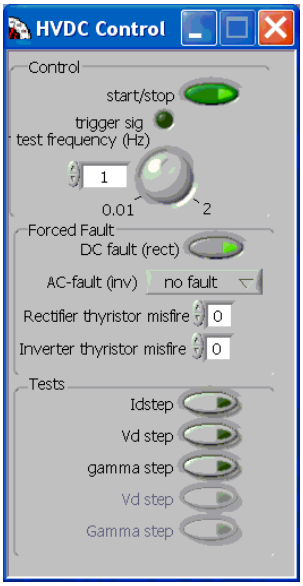

Fig. 9. User controls for fault control

VI. Conclusions

This paper presented a power system simulator based on Simulink and using COTS technologies like standard InfiniBand switch, cluster of AMD/Intel-based PCs and real-time QNX/RT-Linux OS.

The paper demonstrated the capacity of the RT-LAB RTeGrid simulator to achieve real-time simulation of an 8-synchronous machine system with 12-pulse HVDC link at a **hard real time step of 18 microseconds** (without I/O) and **offline acceleration factor above 800**. The model was decoupled into 9 tasks running in parallel on the InfiniBand-connected 3-Opteron-based PCs cluster.

The same model can also be executed at a time step of 37 microseconds on one (1) dual-core dual-CPU Opteron 2.2 GHz PC. Depending on the speed and precision requirements, this can be a acceptable lower cost alternative than the PC cluster solution.

The paper also demonstrated that power system of arbitrary size can be simulated with the InfiniBand-based RTeGrid simulator. Work is going on to improve some aspects of the simulator with regards to the challenges of large power network simulation with regards to task separation ,signal management and user interface.

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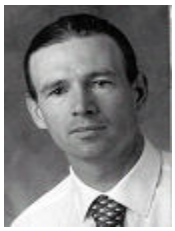
VIII. Biographies



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Jean-Nicolas Paquin is an Application Engineer at Opal-RT Technologies since 2007. He received his M.Eng. degree in 2006 from École de Technologie Supérieure (ÉTS) in Montreal, Canada. His professional interests include the simulation and study of HVDC control and protection systems and model development and validation using SimPowerSystems and EMTP-RV

Vincent Lapointe is a simulation software specialist at Opal-RT Technologies. He received his MScA degree from Laval University, Québec, in 2000. Since 1997, he has worked in the development of the real-time simulator RT-LAB and the main developer of the RT-Events blockset.

Jean Bélanger is the president, CEO and founder of Opal-RT Technologies, Inc. He is a specialist in real-time simulations, with more than 25 years of experience in the field, including many years as part of the simulation division of Hydro-Quebec where he helped developed the world's first 735 kV power transmission systems. He received his M.Sc. from Laval University, Quebec. Since 2001, Mr. Bélanger is a fellow of the Canadian Academy of Engineering.

Loïc Schoen is Software Specialist at Opal-RT Technologies. In 1998, he received his Engineer diploma from the FIUPSO, Orsay, France. He is a specialist in real-time software and the team leader for the RT-LAB program.