FPGA Implementation of a Modified Two-Layer Network Equivalent for Real-Time Simulation of Electromagnetic Transients

Mahmoud Matar and Reza Iravani

***Abstract*--This paper presents an implementation methodology for the modified two-layer network equivalent (M-TLNE), proposed in [1], in a FPGA-based real-time power system simulator. The developed implementation method exploits the intrinsic FPGA parallel structure to reduce the computational time which is of significance for statistical analysis and real-time simulation of electromagnetic transients. The proposed implementation methodology indicates that a computational time, in the nanoseconds range, is achievable.**

A Detailed application of the M-TLNE, involving a three-phase external system with multiple transmission lines, is presented to verify the validity and effectiveness of the proposed implementation methodology.

***Keywords*: External systems, network equivalents, vector fitting, Field Programmable Gate Arrays (FPGA).**

I. Introduction

REAL-TIME electromagnetic transient simulations are primarily required for testing a physical control/protection platform in a closed loop condition. To close the loop, the simulator must be able to accept input data from the device under test and to incorporate this information into the ongoing simulation run. The system's equations need to be solved fast enough, so that the outputs are available before the arrival of the next sample.

Recent development and ongoing advances in microelectronics promise the Field Programmable Gate Array (FPGA) as a new but well established technology to realize real-time simulator for large, interconnected power systems. One FPGA chip (or a group of FPGA chips) can provide the hardware base to carry out series, parallel and/or hybrid processing to solve the system equations. The use of FPGA exploits the flexibility of processor-based simulators and the high speed of the Application Specific Integrated Circuit (ASIC) structure for real-time simulation. The FPGA environment provides a very efficient structure for implementation of mathematical operations, especially multiplications. Hardware multipliers can be implemented in parallel to allow simultaneous evaluation of the products. The FPGA structure also has the advantage of flexible word-size. Therefore the desired precision, at no extra resource cost, can be achieved. Thus, implementing the system equations on a FPGA chip and taking advantage of its parallel structure can provide a very short execution time [2]-[4]. Moreover, the fact that recent FPGA chips have large number of high speed I/Os makes them well suited to real-time simulation applications as they facilitate their interface with the physical control/protection platform under test.

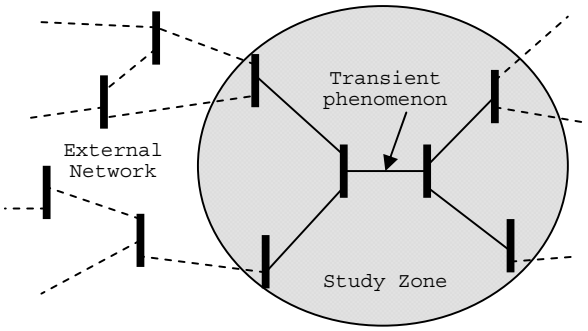

Fig. 1. Partitioning a power system into a study zone and an external zone (multi-port interface)

Electromagnetic transient simulations require detailed modeling of the system under study. However modeling the entire system in detail is impractical in terms of the required computing resources and computational time. This is one of the main bottlenecks for real-time simulations. A common practice to reduce the complexity of the power system being simulated is to divide the system into (i) the study zone and (ii) the external zone, Figure 1. The transient phenomenon of interest occurs and primarily experienced in the study zone. The study zone comprises those power system apparatus that have primary influence or are highly affected by the transient phenomenon. The study zone has to be modeled in details with adequate degree of accuracy.

The external zone represents the remainder of the power system and its components have secondary impact on the transient phenomenon. Therefore, the external zone can be represented by a frequency-dependant equivalent model within the frequency range of interest [5]-[7]. The interaction between the external zone and the study zone are either

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through a single-port or a multi-port interface.

Several approaches have been developed to generate an approximated equivalent to the external system. These approaches can be classified into two main groups: (i) the frequency dependant network equivalent (FDNE) and (ii) the two-layer network equivalent (TLNE). The FDNE realizes the external system with an equivalent RLC network or with a rational function representation of the driving point admittance in either "s" or "z" domain [8]-[12]. The TLNE realizes the external system with a set of simplified transmission line models (surface region) and a low-order rational function (deep region) [13], [14].

For large interconnected external systems with many transmission lines, the admittance frequency response has multiple resonance frequencies. Thus, its approximation with the FDNE results in a high-order rational function. On the other hand, the TLNE provides a simpler equivalent; as the set of simplified transmission lines in the surface layer approximate the admittance frequency response in the whole frequency spectrum and the low-order rational function in the deep region compensates the discrepancy between the system exact frequency response and the response of the surface layer.

The main focus of this paper is on the external equivalents. This paper presents applications of a generalized methodology for implementation of the Modified TLNE (M-TLNE) [1] in a FPGA-based real-time simulator. The developed implementation method allows real-time simulation with a simulation time-step of less than 50 ns.

II. Modified Two-Layer Network Equivalent (M-TLNE)

The M-TLNE is similar to the original TLNE in the sense that the equivalent is composed of a surface layer and deep region. However, the M-TLNE offers a lower order equivalent than the original TLNE. This is achieved by having a simpler surface layer.

Since the surface layer of a TLNE is composed of transmission lines. Thus, in order to simplify the surface layer of the TLNE, it is required to adopt a simpler transmission line model to represent the transmission lines in the surface layer. At the same time the frequency dependence of the transmission line and its distributed nature, has to be accounted for.

A transmission line is characterized by two frequency dependant functions; a propagation function *Hp* and a characteristic impedance *Zc* [15]-[17]. The propagation function H_p defines the relationship between the reflected wave at one end of the line and the incident wave at the other end. H_p can be decomposed into a delay component, H_o, and a shaping component, H_{sh}. Both the shaping function and the characteristic impedance are approximated with low-order rational functions.

One way to simplify the transmission line model in the surface region is by neglecting the frequency-dependence of the characteristic impedance. Thus, for time-domain simulations, Z_c is represented as a constant resistance rather than by a number of RC blocks that are used to model the frequency dependence of the characteristic impedance. The adverse impact of this simplification, which mainly shows up in the frequency response of the equivalent, approximately within 0-150Hz, is overcome by adding a first-order rational function to the input port of the M-TLNE.

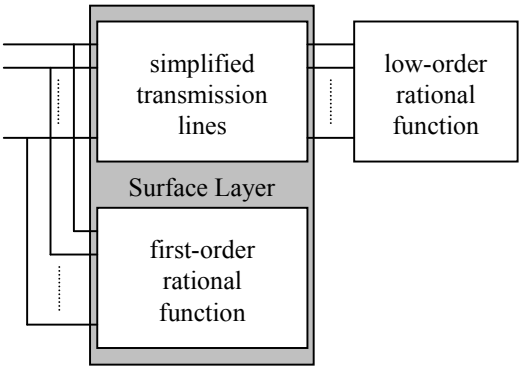

Fig. 2. Schematic of the proposed M-TLNE

The deep region of both the original TLNE and the M-TLNE for a given external system is the same. The deep region is approximated by a low-order rational function. One method to find the rational approximation for the deep region is by using Vector-Fitting (VF) [6].

The M-TLNE is constructed by combining the simplified surface layer with the deep region approximate model, Figure 2. An optimization process is then needed to fine tune the parameters of the equivalent to minimize the deviation between the frequency response of the original input admittance and that of the M-TLNE. The optimization has to be constrained to insure the passivity and stability of the equivalent. Details of fitting the M-TLNE are provided in [1]

III. Discrete Time-Domain Representation of M-TLNE

The time-domain model of the M-TLNE is obtained by replacing each component by its discrete time-domain model.

The time-domain model of a rational function can be obtained based on the bilinear transformation

$$s = \frac{2}{\Delta t}\left[\frac{1-z^{-1}}{1+z^{-1}}\right], \qquad (1)$$

where z^{-1} represents a one time-step delay in time-domain.
For each partial fraction of the rational function that has a real pole and a residue, the discrete time-domain representation is as shown in Figure 3 [18].

The value of the history current source I_h is update every simulation time-step according to the following equation

$$I_h(k) = v(k).G.\left[1-\frac{(p-\alpha)}{(p+\alpha)}\right] - \frac{p-\alpha}{p+\alpha} I_h(k-1) \qquad (2)$$

$$G = \frac{r}{\alpha + p}, \qquad \alpha = \frac{2}{\Delta t} \qquad (3)$$

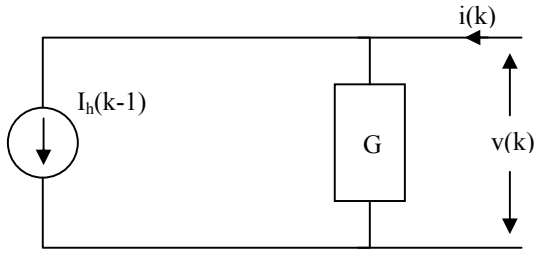

Fig. 3. Discrete-time circuit model of real partial fractions

For every two partial fractions of the rational function that have complex conjugate poles $(p' \pm jp'')$ and residues $(r' \pm jr'')$, the discrete time-domain representation is as shown in Figure 4. The values of the history current sources I_{1h} and I_{2h} are updated using the following equations [18]

$$I_{1h}(k) = Av(k) - B\left[I_{1h}(k-1) + I_{2h}(k-2)\right] \quad (4)$$

$$I_{2h}(k) = Cv(k) - D\left[I_{1h}(k-1) + I_{2h}(k-2)\right] \quad (5)$$

$$G = 2\frac{r'(\alpha + p') + p''r''}{\alpha^2 + 2p'\alpha + (p'^2 + p''^2)}, \quad \alpha = \frac{2}{\Delta t} \quad (6)$$

Where A, B, C and D are constants that are function of the complex conjugate poles $(p' \pm jp'')$ and residues $(r' \pm jr'')$.

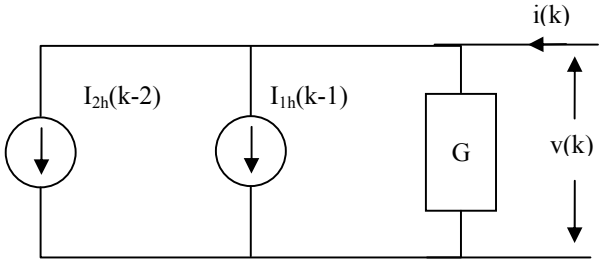

Fig. 4. Discrete-time circuit model of every two conjugate partial fractions

The time-domain transmission line model adopted in this work is based on the frequency-dependant transmission line model developed by J. Marti [17]. However, the model is simpler since in the M-TLNE the frequency dependence of the characteristic impedance is neglected and the characteristic impedance is modeled as a pure resistance.

The rational approximation of the shaping function is incorporated in the model using recursive convolution. The discrete-time circuit model for the frequency-dependent transmission line model is shown in Figure 5.

Where the value of the history current source I_m is updated using the following equations

$$\mathrm{I_m}(t) = \sum_{i=1}^{N} I_m^i(t) \quad (7)$$

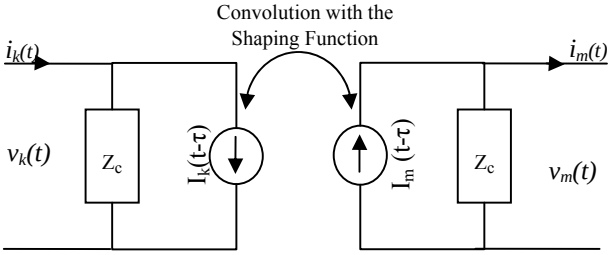

Fig. 5. Discrete-time circuit model for the frequency-dependent transmission line model

where

$$I_m^i(t) = E^i\left[I_{mh}(t) + I_{mh}(t-\Delta t)\right] - F^i I_m^i(t-\Delta t) \quad (8)$$

and

$$I_{mh}(t) = I_k(t-\tau) + \frac{2}{Z_c}V_k(t) \quad (9)$$

where E^i and F^i are constants that are function of the shaping function's poles and residues.

The value of the history current source I_k is updated in a similar manner as I_m using a similar set of equations.

Based on the discrete-time circuit model of each component, the M-TLNE is mathematically represented as [19]

$$Yv(t) = i(t) - I \quad (10)$$

Where *Y* is the nodal admittance matrix, *v(t)* is the vector of the node voltages, *i(t)* is the vector of current sources, and *I* is the vector of history current sources.

IV. FPGA Implementation of the M-TLNE

The philosophy behind the proposed FPGA implementation methodology is to efficiently exploit the FPGA parallel architecture and to fully utilize its inherent capability to support custom hardware designs that are tailored to the problem being solved. The proposed implementation approach is envisioned for a fixed, pre-specified simulation time-step regardless of the M-TLNE size.

The system of equations representing the M-TLNE in time-domain is analyzed to determine the dependencies between the equations and to identify the equations that can be processed in parallel. As can be seen from (2) to (10), during each simulation cycle the values of the history current sources are updated using the new voltages values calculated at that cycle. Thus we have flow-dependency between the current and voltage equations. But rather than that, the voltage equations are independent on each other. Also the equations used to update the values of the history current sources are independent on each other.

The first level of parallelism is determined from the dependency analysis. It is found that the voltage equations can be solved in parallel and also the equations used to update the values of the history current sources lend themselves well

towards parallel execution.

Each individual equation by its own comprises a number of primitive operations. These operations are mainly multiplications and additions. Inspection of each individual equation shows that the multiplications are independent from each other and can be done in parallel. Thus another level of parallelism at the level of primitive operations can be exploited.

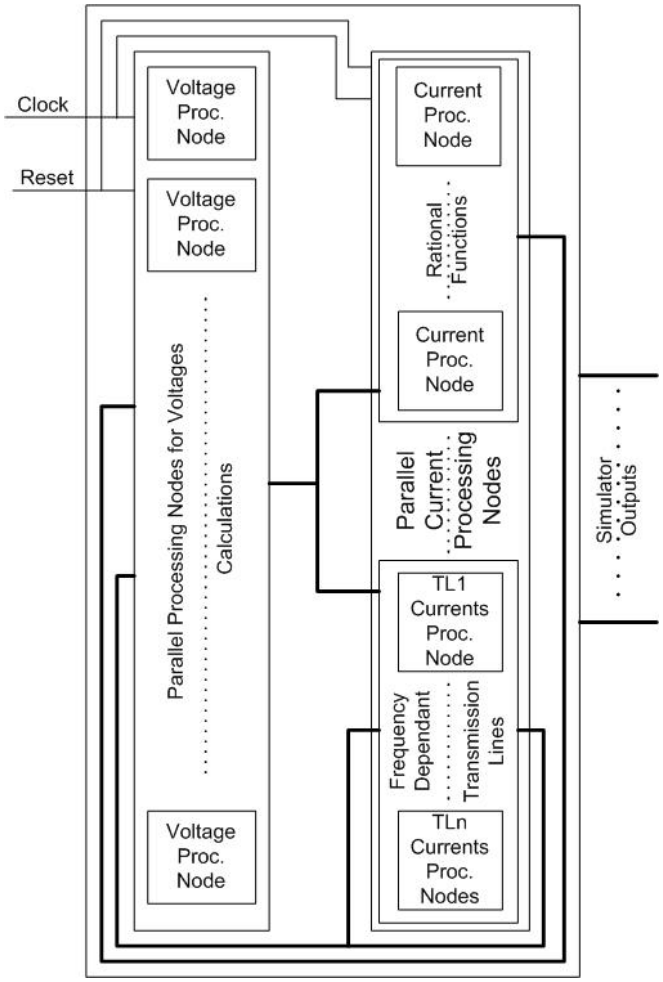

Fig. 6. Proposed implementation schematic of the M-TLNE in a FPGA chip

The proposed implementation methodology takes advantage of the FPGA configurable architecture and exploits all possible levels of parallelism. The design is based on implementing a number of processing nodes on the FPGA. Each processing node is a mapping of a single equation. Within each processing node, the primitive operations are mapped to hardware circuitry that performs that primitive operation. For example a multiplication operation is mapped to a hardware multiplier. The mapping of the primitive operations to hardware is done in such a way to exploit the independencies between operations, i.e. parallel hardware circuitry are implemented whenever possible as dictated by the equations.

Another very important issue that has to be taken care of is the communication between different processing nodes, as interprocessors communication time can impose addition overhead time that can limit the performance. In the proposed FPGA implementation, a unidirectional point-to-point static interconnection network is implemented such that the data can be transferred directly from the output register of one processing element to the input register of another processing element. The interconnection network is operated in a synchronous mode in which a single global clock controls the flow of data.

The whole design is controlled and synchronized by a global clock. With the transition of every clock pulse, all the processing nodes read their inputs and start computing the results of the assigned equations.

Fixed-point, rather than floating-point, calculations are adopted for the implementation. The floating-point calculation offers a wider range and a higher accuracy for numerical representation. However, the fixed-point calculation significantly enhances the speed of algorithm execution, and reduces the required hardware resources for implementation. The developed VHDL code is based on a fixed-point, 32-bit, signed Q11.20 representation, i.e. 11 bits for the integer part and 20 bits for the fractional part.

Figure 6 shows the proposed implementation schematic of the M-TLNE model in a FPGA chip. As shown in Figure 6 there are three main types of processing nodes, (i) voltage processing nodes, (ii) rational functions' current processing nodes and (iii) transmission lines' current processing nodes.

The voltage processing nodes are implemented to operate independently and in parallel with each other. Thus simultaneous voltage calculation is achieved at all nodes. Similarly, the current processing nodes are implemented in parallel to achieve simultaneous calculations of the history current sources. The current processing nodes –that are responsible for updating the history current sources of the transmission lines– utilize the FPGA's built in RAM blocks as storage arrays to account for the traveling times of transmission lines.

V. Validation

To validate the accuracy and the effectiveness of the proposed M-TLNE and its implementation on a FPGA, the M-TLNE equivalent of the three phase 41-bus system with 50 transmission lines, shown in Figure 7 [20], is first fitted and its admittance frequency response is compared with the admittance frequency response of the original system. Then the M-TLNE is implemented on a FPGA according to the proposed implementation methodology. The time-domain simulation results corresponding to an energization transient and to a three-phase to ground short circuit fault are compared with the corresponding results obtained from the simulation of the original network in the PSCAD/EMTDC environment.

The admittance frequency response of the original system is generated from PSCAD/EMTDC for frequencies up to 10 kHz at 1500 logarithmically distributed frequency points. The system model is first decoupled into a ground mode and two identical aerial modes. The M-TLNE is independently fitted

for the ground mode and the aerial mode.

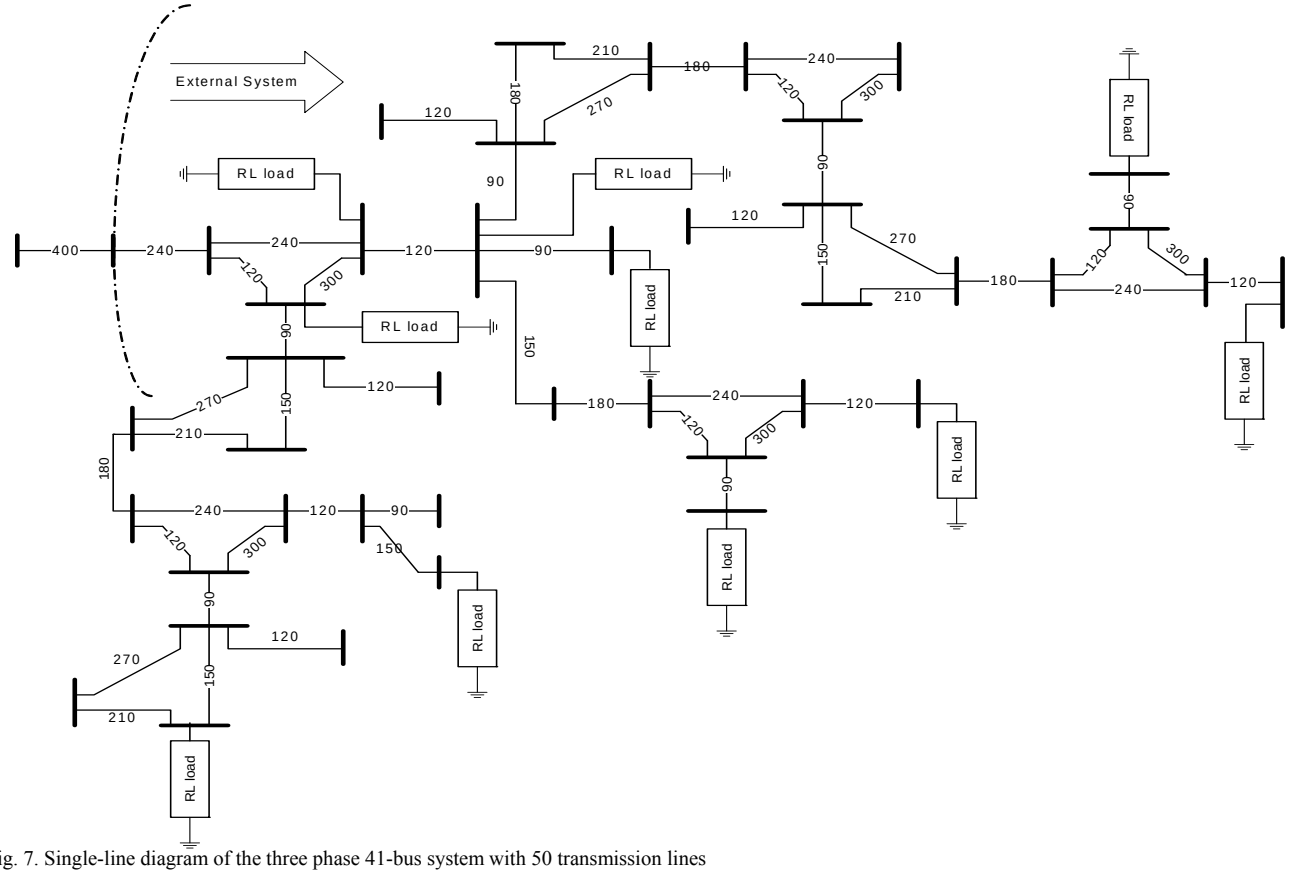

Fig. 7. Single-line diagram of the three phase 41-bus system with 50 transmission lines

The division of the external system into a surface layer and a deep region is based on engineering judgment. It depends on the topology of the external system, length of transmission lines, the frequency range of interest, and the complexity of the admittance frequency response.

For the aerial mode, the equivalent consists of a surface layer composed of 6 simplified transmission line models and one first-order rational function at the input port of the equivalent. Each transmission line is approximated with a 4^{th}-order shaping function (only real poles) and the characteristic impedance is represented by a fixed resistance. The deep region is approximated with a 4th-order rational function. The RMS error for the M-TLNE is approximately 3%. The order of the equivalent FDNE model corresponding to the same RMS error is 130.

For the ground mode, the M-TLNE consists of a surface layer composed of just one transmission line and one first-order rational function connected at the input port of the equivalent. The transmission line is approximated with a 4th-order shaping function (only real poles) and the characteristic impedance is represented by a fixed resistance. The deep region is approximated with a 12^{th}-order rational function. The RMS error for the M-TLNE is approximately 3%. The order of the equivalent FDNE model corresponding to the same RMS error is 40.

Figures 8, 9 and 10 compare the input admittance of the original system, obtained from PSCAD/EMTDC, and that of the M-TLNE. Figures 8, 9 and 10 show close agreements between the corresponding results. Moreover, the M-TLNE equivalent shows very high accuracy at low frequencies.

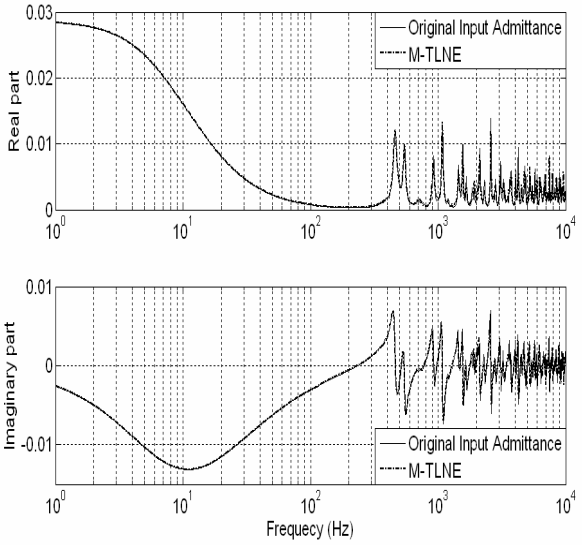

Fig. 8. Aerial mode input admittance

The M-TLNE is implemented and simulated based on the Quartus II, version 7.0 software tool. Quartus II is used for (i) design entry, (ii) functional/timing simulation of the design,

(iii) design synthesis, (iv) fitting the design on the target FPGA, and (v) programming the FPGA. The M-TLNE is implemented on an Altera Startix II EP2S180F1020C3 FPGA. Based on the Quartus II timing analyzer the calculation time per simulation time-step is 28.3 ns, i.e. a real-time operation is achieved since the calculation time per simulation time-step is less than the selected simulation time-step of 5 μs. The PSCAD computation time per simulation time-step, on an Intel 2.53 GHz Core2Due machine with 3 GB of memory, is 205 μs. Therefore, the developed M-TLNE along with the proposed FPGA implementation methodology offers approximately 7200X performance advantage over the conventional computer-based simulation platform.

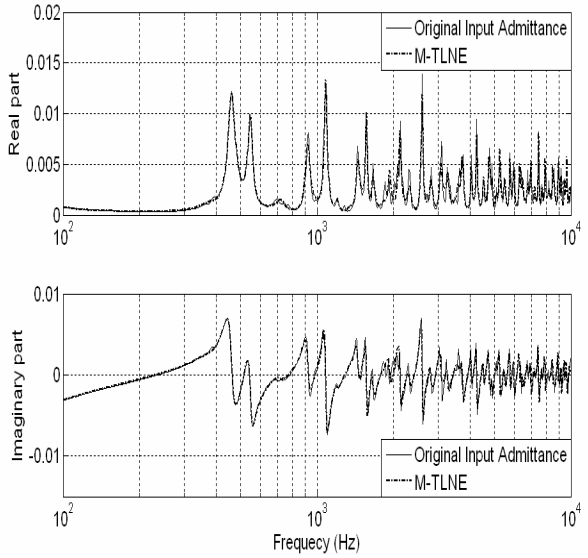

Fig. 9. Aerial mode input admittance (Zoomed)

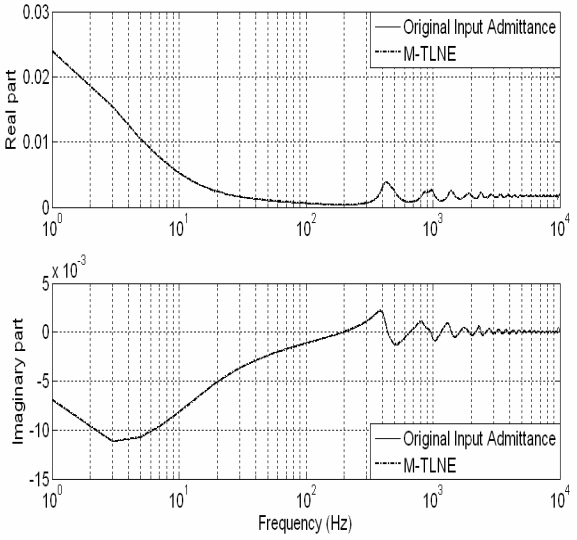

Fig. 10. Ground mode input admittance

The M-TLNE equivalent along with the study zone utilizes around 32% of the total logic and 100% of the DSP blocks of the selected FPGA chip and approximately 1% of the total on chip memory.

The three-phase system of Figure 7 is subjected to two transient scenarios: (i) a balanced 66 kV, 60 Hz energization scenario at the sending end of the transmission line located in the study zone and (ii) a three phase to ground fault at 80 ms that lasts for 25 ms.

Figure 11 shows the time-domain simulation results for the three-phase voltages, at the interface bus between the study zone and the external network, of both the original full system and the corresponding FPGA implementation of the M-TLNE. The time-domain simulation results for the original network are deduced from the PSCAD/EMTDC software tool.

Close agreement between the corresponding results of Figure 11, i.e. the small relative error of less than 4%, verifies accuracy of the proposed M-TLNE.

The error is defined based on the Euclidean norm as

$$error = \frac{\|a-b\|_2}{\|a\|_2} 100 \qquad (11)$$

Where “a” and “b” are the vectors associated with the voltages deduced from the PSCAD/EMTDC software tool and the simulation results of the FPGA-based simulator respectively.

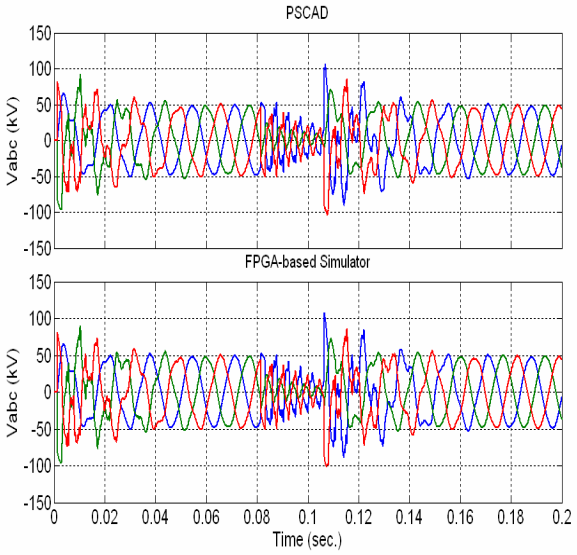

Fig. 11. Three-phase voltages obtained from PSCAD simulation of the original network and from the M-TLNE implementation on a FPGA-based simulator

The error between the PSCAD results and that of the FPGA-based simulator has two sources. Most of the error is mainly due to the discrepancy between the frequency response of the original network and the fitted M-TLNE equivalent. The other part of the error is due to the difference in numbers representation format. PSCAD uses floating-point representation for numbers whereas the FPGA-based simulator uses fixed-point representation. In the FPGA-based real-time simulator the coefficients of equations and the signal variables can only take discrete values within a specified

range. If desired, the error caused due to this number representation, i.e. the quantization error can be reduced by increasing the number of bits. However, this requires more resources from the FPGA. A compromise between the size and accuracy can be reached based on the desired accuracy.

VI. Conclusions

This paper presents an implementation methodology for the modified two-layer network equivalent (M-TLNE) in a FPGA-based power system simulator. The developed implementation method exploits all levels of parallelism and the intrinsic FPGA parallel structure to reduce the computational time.

The accuracy and computational efficiency of the proposed FPGA implementation methodology have been verified. The M-TLNE for a three phase 41-bus system with 50 transmission lines is fitted and implemented on an FPGA-based real-time simulator. The real-time simulation results are also compared with the off-line simulation results in the PSCAD/EMTDC environment. The study results conclude that:

- The M-TLNE – despite its simplicity – can accurately represent an external system for electromagnetic transients studies for the desired frequency bandwidth.
- The corresponding FPGA-based real-time simulator results and the off-line simulation results closely agree and confirm validity and accuracy of the proposed methodology.
- For the adopted FPGA environment, real-time simulation of the M-TLNE is achieved in 28.3 ns which is approximately 177 times less than the selected 5 μs simulation time-step.

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VIII. Biographies

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