Testing Firing Pulse Controls for a VSC-based HVDC Scheme with a Real Time Timestep < 3 µs

P.A. Forsyth, T.L. Maguire, D. Shearer, D. Rydmell

Abstract --The paper deals with the difficulties of testing firing pulse controls for a VSC-based HVDC scheme using a real time digital simulator. The main goal is to provide low latency, closed-loop interaction between the firing pulse controls and the simulator for PWM firing in the range of 1.6 kHz. The closed-loop setup is used to verify and improve the performance of the physical controls, so the simulator must provide an accurate representation of the actual VSC-based HVDC scheme for the full range of start-up, shut-down, steady state and transient operation.

The paper describes the difficulties encountered when attempting to test the actual firing pulse controls for a VSC-based HVDC link. The main difficulty resulted from the losses of the VSC converters in the simulation being higher than in the real system. To rectify the problem a new fixed topology 2-level VSC was implemented using stored matrices to represent the different states of the converter.

In the final implementation, the power system circuit was split into four subnetworks each running in real time with a timestep < 3 µs. The real time simulation showed that the VSC losses in the simulation could match those of the real system. Furthermore the real time simulation results showed an excellent correlation with the results of off-line simulation.

I. Introduction

As VSC-based converters become more common and widely applied, new tools and techniques are being developed to aid power engineers in their application. Off-line simulation programs are being enhanced and new models added for VSC-based schemes. Similarly, new models and techniques are being developed for real time simulators so they can be used in the development and testing of the control systems for VSC-based schemes. Unlike off-line simulation tools, real time simulators can be connected to the physical control system allowing the actual hardware implementation to be run in closed-loop with the simulated network. This is vital to prove the performance and functionality of the actual control and protection system before it is installed in the network. Fault scenarios and operating conditions that may be difficult or even impossible to induce on-site can be simulated in real time and precisely regulated to study the behavior of the control and protection system.

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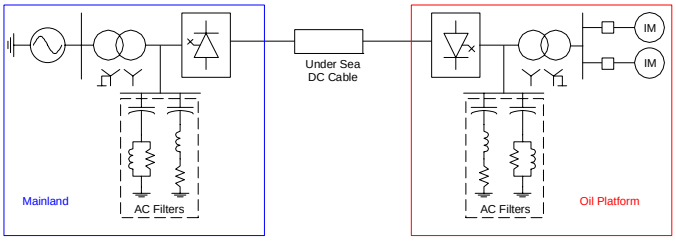

Fig. 1. VSC-based HVDC Scheme to Supply Power to Oil Platform Based Induction Motors

ABB AB in Ludvika, Sweden is a manufacturer of VSC-based HVDC schemes and has in the past used an analogue-hybrid real time simulator to perform Factory System Tests (FST) for the controls of VSC-based HVDC equipment. However for several years ABB has relied on the Real Time Digital Simulator (RTDS®) to perform FST for the controls of conventional HVDC schemes. The efficiencies and flexibility of the RTDS Simulator prompted ABB to evaluate its use for FST of VSC-based HVDC. This action was further reinforced by the fact that the RTDS Simulator already had been used for closed-loop control system testing of a 3-level STATCOM [1].

ABB evaluated the RTDS Simulator on a recent project to supply power to an offshore oil platform located approximately 300 km from the utility grid. HVDC transmission was chosen for the project because the new technology increased energy efficiency and decreased the impact on the environment since an offshore generating plant would no longer be needed.

A VSC-based HVDC scheme was required for the project because of the low short circuit ratio at the inverter. The platform's 78 MW load was also well suited to today's VSC technology. Furthermore the PWM firing of the VSC-based scheme allowed the physical size of the filters on the platform to be minimized with respect to a conventional thyristor based HVDC scheme.

The main electrical load on the platform is four induction motors. Starting the four large motors was a critical design aspect of the power supply to the platform. The large initial current and reactive power drawn during startup had to be adequately compensated through the response of the DC scheme or the motors would not start.

II. Simulation Challenges

The response time of the controls and the VSC switching frequency dictated a simulation timestep in the range of 1-3 µs and a maximum input to output latency of ~ 6 µs to properly represent the expected system dynamics. Recent developments in the RTDS Simulator allow special subnetworks to be simulated with timesteps in the required range.

The original technique developed on the RTDS Simulator for VSC simulations allows user configurable converters, but relies on a timestep in the range of 1-3 µs [2]. The key element of the technique was the method used to avoid the need for inverting or decomposing the admittance matrix. Instead of representing the valves as two state resistances (i.e. a small resistance in the on-state and large resistance in the off-state), they were represented as small inductances in the on-state and as small capacitances in the off-state [3]. By correctly choosing the resistance for the Dommel equivalent circuit, as shown in equation (1),

$$\frac{2L}{\Delta t} = \frac{\Delta t}{2C} = R \qquad (1)$$

only the value of the current injection is changed when switching between the on- and off-state. A damping resistor was included in series with the capacitor to avoid unrealistic switching transients. The damping resistance was accommodated by an adjustment to the value of C. The damping resistance along with the charging of the capacitor dictated the losses of the simulated VSC bridge. For this particular project the original VSC simulation technique resulted in converter losses in the range of 4-8% whereas the expected losses of the real system were < 2%.

Since the induction motor start up was very sensitive to the converter losses, a new model was developed to ensure the losses were representative of the actual VSC-based HVDC scheme.

III. Small Timestep Subnetwork

The small timestep subnetwork was developed for the RTDS Simulator to allow VSC-based schemes to be included in large scale network simulations running with an overall timestep in the range of 50 µs. The concept is to have the VSC schemes simulated with a small timestep (in the range of 1-3 µs) and numerically interfaced to the large scale simulation. Naturally the small timestep subnetworks require more hardware resources than when simulating components at 50 µs. The dual timestep approach optimizes the hardware resources by applying small timestep subnetworks only where a higher frequency representation is required. However in some instances, for example the project described herein, it is more effective to implement the entire circuit using multiple small timestep subnetworks.

To implement the small timestep subnetworks, considerable processing power is required. The RTDS Simulator utilizes IBM 750GX Power PC processors running at 1 GHz clock speed. While the clock speed of the 750GX is lower than other mainstream processors, the powerful RISC instruction set and short pipeline make it the best suited processor currently available for real time simulation.

Two 750GX processors were included on one Giga Processor Card (GPC), with direct communications link between the processors, so the combined power could be utilized for complex component models.

For simulations running with a timestep of 1-3 µs, a clock speed of 1 GHz allows a maximum of 1000-3000 instructions per timestep using one processor, or 2000-6000 instructions per timestep using two processors for the entire subnetwork. To provide accurate models to represent the network with so few instructions per timestep, the code must be highly optimized. The most efficient code possible was created by writing dedicated assembly language code specifically for the 750GX processor. Experience has shown that the direct assembly language code can easily be two times more efficient than code which was cross compiled from C.

IV. Subnetwork Splitting

As with any real time simulation technique, there is a finite limit to what can be simulated in a subnetwork and still maintain real time operation. Using the current processing platform and with the subnetworks running at a timestep of < 3 µs, the number of single-phase nodes must be kept below 30 and a reasonable number of elements (transformers, machines, etc.) must be maintained.

For this particular study, the network was split into four subnetworks, as illustrated by Fig 2. The subnetworks were linked by traveling wave cable models indicated by the red rectangles. The traveling wave models decoupled the overall network matrix and allowed the nodal equations for each subnetwork to be solved independently by separate processors. The travel time of the cables had to be at least one timestep long. However with a timestep of < 3 µs, the traveling wave models represented cables that could be as short as 200-300 meters.

Subnetwork #1 contained the network equivalent source, the converter transformer, AC filters and a new 2-level VSC component. The traveling wave cable model separating Subnetwork #1 and #2 represented a small portion of the undersea cable. The main portion of the undersea cable was represented in Subnetwork #2 by frequency dependent pi-sections. Subnetwork #3 represented another new 2-level VSC at the offshore station, the AC filters and the converter transformer. To balance the subnetworks and minimize the simulation timestep, the offshore induction machines were separated into Subnetwork #4. This meant a traveling wave cable model had to be added between the converter transformer and the induction machines. If the actual cable were shorter than the minimum length of the traveling wave cable model, the error could be minimized by including some of the converter transformer leakage in the cable model.

If it had been necessary to represent a larger AC network at

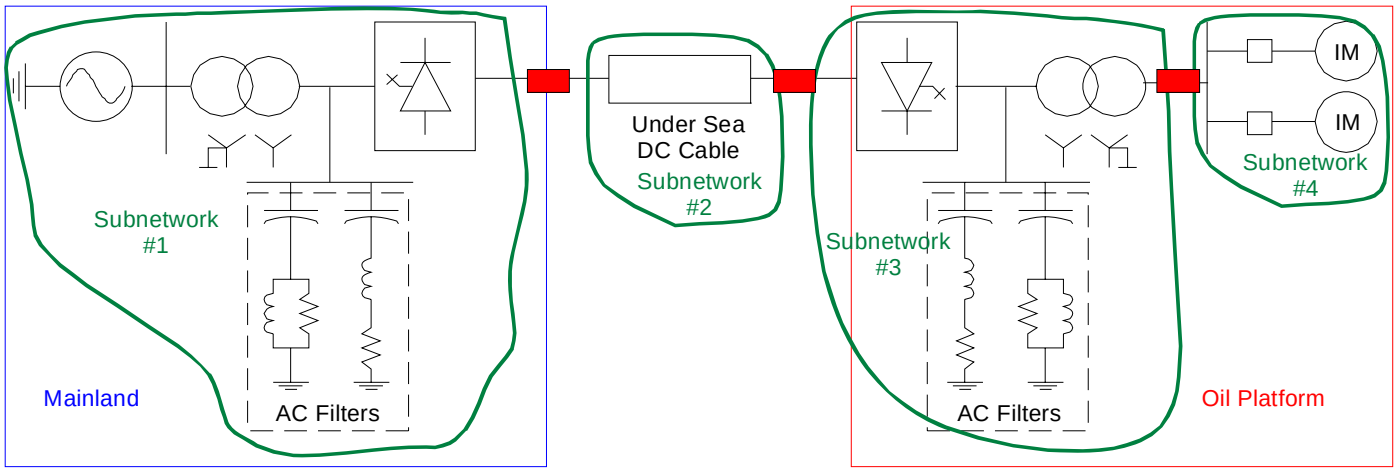

Fig. 2. Subnetwork splitting

the rectifier, it would have been possible to interface the circuit shown in Fig 1 and 2 with a large scale network simulation running with a timestep in the range of 50-70 µs.

The higher level controls for breaker controls, induction motor loading, etc. were also represented with a timestep in the range of 50-70 µs.

V. Low Loss Bridge

The problem of the high converter losses was solved through the development of a fixed topology, 2-level VSC bridge. The main advantage of the original VSC representation was that it allowed the bridge to be configured with individual components which was achieved by avoiding the need to invert (or decompose) the admittance matrix. However it was possible to develop a fixed topology, 2-level bridge using stored matrices to represent the different states of the converter admittance matrix.

The stored matrix approach has been used in the past for real time simulation of conventional HVDC valves and is well established. Pre-inverted matrices are stored in memory and selected based on the switching state of the converter. A significant disadvantage of the stored matrix approach is that it dictates a fixed converter topology. The memory storage requirements and the transition logic also become unwieldy for 3-level schemes. In addition the stored matrix approach required approximately 25% more computation than the original small timestep subnetwork approach (i.e. on-state represented as a small inductance and off-state represented as a small capacitance) which translates into a longer timestep.

Using the stored matrices, the valves are represented by a large resistance in the off-state and a small resistance in the on-state. The resistance values are directly defined by the user. Snubber circuits were included in the new model to damp possible switching transients. No switching losses are directly incurred due to the transition from the low resistance (on-state) to high resistance (off-state) or vice-versa. This allowed the overall losses of the new 2-level bridge to be manipulated through the choice of the snubber components.

The significant inductance (typically 5-10% of the converter rating) on the AC side of the converter and the capacitance on the DC side of the converter allow interfaces to the AC and DC networks with absolute stability and without significant error.

Even though the new VSC bridge component was implemented using the stored matrix approach, breakers and other switching components were still handled using the original small timestep subnetwork approach. This allowed the circuit topology outside the bridge to be user configured.

VI. Low Latency I/O

New techniques were applied to achieve a representative real time simulation with a timestep of < 3 µs. However to test the physical controls, I/O also had to be incorporated into the simulation and be serviced within the < 3 µs timestep.

Each subnetwork was assigned to either one or two processors depending on the number of elements included in the section. In this case the rectifier and inverter were located on different processors and different cards. The approach adopted through the design of the RTDS Simulator is to provide parallel data paths for communication from processors to I/O. The design allows each processor to communicate directly with a number of I/O modules.

The firing pulse input to the simulator is fed through the Giga Transceiver Digital Input (GTDI) card. The GTDI has 64 channels and provides optical isolation between the controls and the simulator. One GTDI card was used for each end of the HVDC link to provide direct communication to the processors simulating the respective converters.

The GTDI samples the digital input at a period of ~400 ns. In turn the processor reads the state of the firing pulse input at the start of every timestep and uses it in the calculation of the node voltages and branch currents. At the end of the timestep the analogue output is updated via the Giga Transceiver Analogue Output (GTAO) card. Therefore the maximum input to output latency is two small timesteps or in this case < 6 µs.

The GTAO also provides optical isolation between the simulator and the control system therefore maintaining

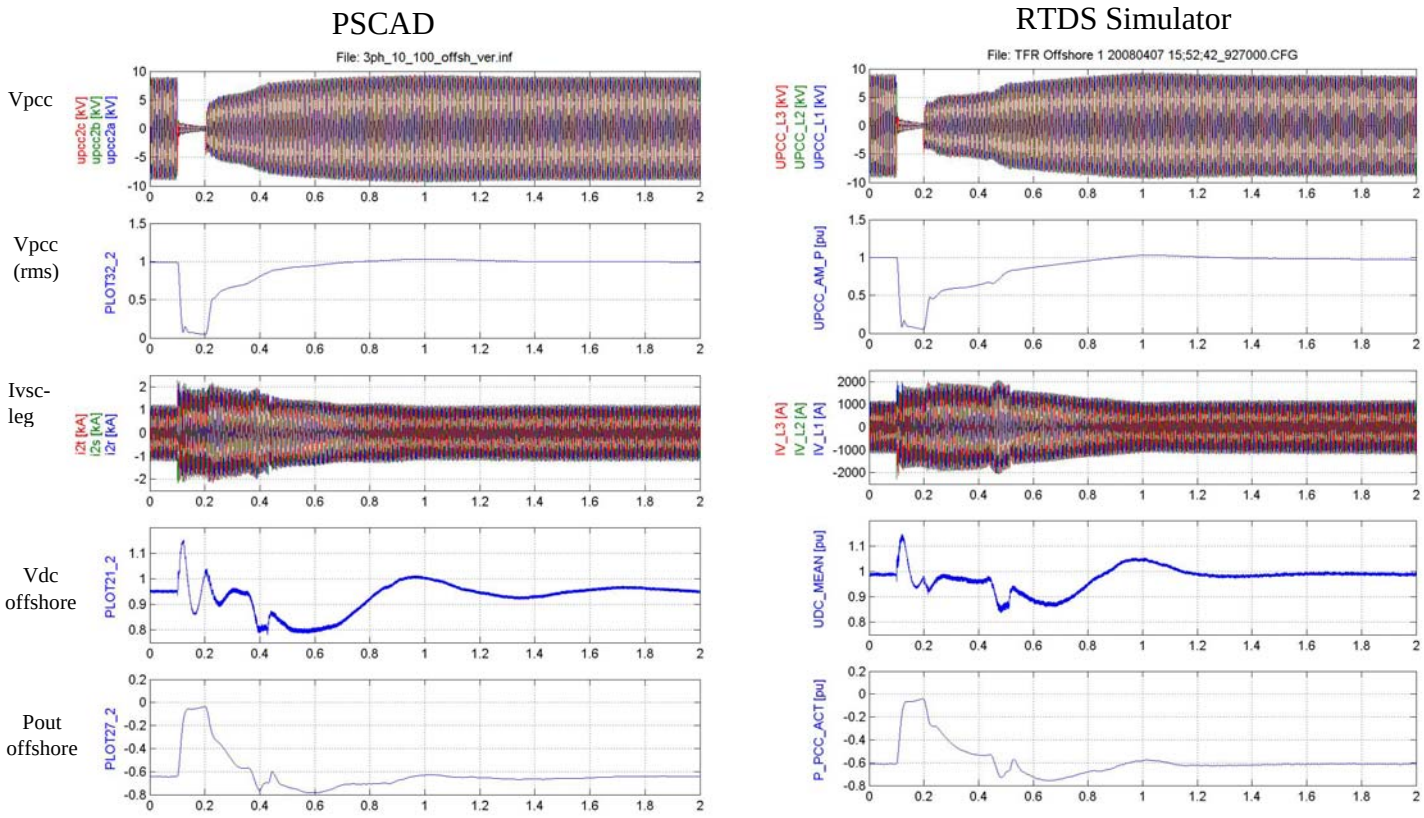

Fig 3: Comparison of simulation results from PSCAD and the RTDS Simulator

galvanic separation between the simulator and the control system. The GTAO has 12 channels with 16-bit digital to analogue converters to provide a large dynamic range. Two GTAO cards can be connected to each subnetwork processor so a maximum of 48 analogue outputs can be provided per subnetwork.

VII. Validation

In addition to the tests conducted using the RTDS Simulator, the controls are normally tuned during the Dynamic Performance Study performed with PSCAD/EMTDC. PSCAD/EMTDC is widely accepted as providing accurate representations of VSC-based schemes [4]. Results from both simulation tools are presented above in Fig 3 as validation of the real time results.

The first graph shows the instantaneous voltage at the point of common coupling on the mainland, followed by the RMS of the same signal. The third graph shows the instantaneous current in each leg of the VSC on the offshore station. The last graph shows the real power out of the offshore station.

Fig 3 shows the results for a 3-phase fault to ground at the offshore station lasting for 100 ms. The correlation of the results is excellent and the small variation in the results is attributable to a slight difference in the pre-fault condition and the manner in which the DC cable has been modeled.

VIII. Conclusions

The challenge presented in this paper was to perform closed-loop real time testing of a VSC-based HVDC scheme controller. Due to the response time of the controls and the VSC switching frequency, a simulation timestep in the range of 1-3 µs and a maximum input to output latency in the range of 6 µs was required to properly represent the system dynamics. The nature of the network being simulated demanded realistic representation of valve losses. Finally, closed-loop testing of the actual firing pulse controls could not be achieved without being able to exchange the necessary digital and analogue I/O signals between the controller and the simulator in real time.

The challenges of the real time simulation were overcome and the physical firing pulse controls were successfully tested using the RTDS Simulator. The flexibility of the RTDS Simulator to represent a wide range of components was key to the successful completion of the testing.

By applying the stored matrix approach to represent the different switching states, it was possible to create a fixed topology 2-level VSC bridge with switching losses that can be adjusted to match the real converter.

The techniques applied to model the VSC-based HVDC scheme with an overall timestep < 3 µs can be generally applied. Therefore very tightly coupled systems, with or without VSC, can be implemented using the subnetworks and an overall timestep in range of 1-3 µs.

Commissioning of the actual VSC land station has been completed ahead of schedule and it is presently operating as an SVC while waiting for the offshore platform to be completed. Currently ABB is using the same VSC converter model for FST testing of two other VSC-based HVDC converter projects. The projects are to connect offshore wind farms to very weak AC networks.

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X. Biographies

Paul Forsyth received his B.Sc. degree in Electrical Engineering from the University of Manitoba, Canada in 1988. After graduating he worked for several years in the area of reactive power compensation and HVDC at ABB Power Systems in Switzerland. He also worked for Haefely-Trench in both Germany and Switzerland before returning to Canada in 1995. Since that time he has been employed by RTDS Technologies where he currently holds the title of Marketing Manager / Simulator Specialist.

Trevor Maguire graduated from the University of Manitoba with B.Sc.EE, M.Sc.EE and Ph.D. degrees in 1975, 1986, and 1992 respectively.
Relevant employment experience includes time with Manitoba Hydro (1975-76), Manitoba HVDC Research Centre (1986-1994), and RTDS Technologies, Inc. (1994-present). He is a founding principal of RTDS Technologies, Inc. with a special interest in real time simulation model development and also real time simulation digital hardware development. He participated in creating the world's first commercial real time digital power system simulator.

David Shearer graduated from the University of Auckland, New Zealand with BE Electrical and Electronic in 1986. After graduating he worked for several years in the NZ Electricity Department. Following the NZ hybrid HVDC upgrade David began working with ABB in 1993. His current position is Manager of Models and Simulator development for ABB AB, HVDC.

Daniel Rydmell has completed a M. Sc degree from Mälardalens University in 2006 and B. Sc from Dalarnas University in 2003. Daniel began working for ABB, HVDC in 2006. He works with preparation and running of the simulators for Factory System Testing of control systems. His current job title is deputy technical officer for RTDS.