Converter Based Controlled Reactance for Damping Subsynchronous Resonance

Antonio C. Borré, Robson F. S. Dias, Antonio C. S. Lima, Edson H. Watanabe

***Abstract*—This works presents a methodology to synthesize a controlled reactance based on power electronics converter. One may understand this type of device as a *Converter Based Controlled Reactance* (CBCR) and there are several different types of controllers, but basically one main structure. As the converter performance may be affected by harmonic distortion in either voltage or current a PLL (*Phase-Locked Loop*) circuit is proposed to eliminate the effect of these distortions. The proposed CBCR can be used for reactive power compensation and to mitigate subsynchronous resonance.**

The work is divided in two main parts. First, the basic structure of the CBCR is presented and then the new control is tested using "*IEEE First Benchmark*" for subsynchronous resonance. All the simulations were carried out using PSCAD/EMTDC program.

***Keywords*—Controllable reactances, series compensation, subsynchronous resonance (SSR), PLL (Phase-Locked Loop).**

I. Introduction

Series reactive power compensation is a common procedure for increasing power transmission capability and stability conditions. Usually this can be achieved by means of series capacitor which adds a new resonance frequency to the line, normally below the grid frequency and has a very low damping factor. This type of phenomenon is commonly known as subsynchronous resonance (SSR). In some cases the SSR is not present, but electromechanical oscillations is, and this is normally in the frequency range of few Hz. To assure power reliability mitigative measures such as fast controllers, PSS (*Power System Stabilizer*) are needed. Another way to minimize power oscillations, turbine failures and sustained overvoltages during SSR or power oscillation is to include controlled reactance in series with the transmission line and this can be done by TCSC (*Thyristor Controlled Series Capacitor*) [1] and the SSSC (*Static Series Synchronous Compensator*) [2], which is based on *Voltage Source Converters* (VSC). The former has many examples of application in Power System throughout the world, however it has the disadvantage of including another resonance in the system while the latter is the main focus of the present work. Further details concerning TCSC and a possible way to have a simple and effective device using *Gate Controlled Switch* can be found in [3], [4].

One of the first papers dealing with synthesis of reactances using power electronics devices dates back to 1992, when the so called *Variable Active-Passive Reactance* (VAPAR) was presented [5], [6]. A few years later, in 1999, Hamill put forward a *Bootstrap Variable Inductance* (BVI) based on the concept of *bootstrapping* used in electronics devices [7], [8]. In 2004, Dranga *et al.* [9], [10] proposed to obtain a variable reactance from a comparison of magnetic fluxes. Later on, the same control scheme was named *Active Variable Inductance* [11], [12] (AVI). More recent works have focused on the concept of direct reactance synthesis DRS [13], [14]. All these control methodology can be grouped in a single converter topology. In the present work the series connection of Voltage Source Converters controlled to synthesize a controlled reactance is defined as *Converter Based Controlled Reactance* (CBCR).

This work is divided in two main parts, in the first the basic control principles of a CBCR are presented. A new control scheme for reactance synthesis based on a *Phase-Locked Loop* (PLL) circuit proposed in this paper is also presented. As it will be shown in the remainder of the paper a CBCR can be used to synthesize a inductive/capactive reactance including a negative inductor or capacitor. The PLL circuit adds robustness to the system as the effect of harmonic voltage/current in the converter control is reduced. To validate the proposed methodology several simulation cases are used and a comparison with previous results is shown [14]. An analysis of the CBCR for subsynchronous resonance (SSR) is also presented using the "*IEEE First Benchmark*" [15].

II. Basic Principles and Topologies of CBCR

The main circuit of a CBCR is basically a voltage source converter behind an inductance as shown in Fig. 1. The converter can be understood as a controlled voltage source capable of controlling both amplitude and phase of the voltage fundamental component, see Fig. 2a. In steady-state, CBCR depends only on the output voltage of the VSC ($\mathbf{U_{VSC}}$), shown in Fig. 2a.

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Assuming that $\mathbf{U_{VSC}}$ and Z_L are constant, the controlled impedance can be defined as (see Fig. 2b):

$$\mathbf{Z}_{CBCR} = \frac{\mathbf{U}_T\,\mathbf{Z}_L}{\mathbf{U}_T - \mathbf{U}_{VSC}}\,. \tag{1}$$

Thus by controlling the converter voltage a controlled impedance can be obtained. In fact, the aforementioned equivalent reactance differ only in the way that the converter voltage is controlled, i.e. with a distinct set of controllers: VAPAR, BVI, AVI or DRS. All these methodologies depend on the actual line voltage/current in the line and are affected by harmonic contents in either or both. To overcome this limitation the new control algorithm based on a PLL is proposed.

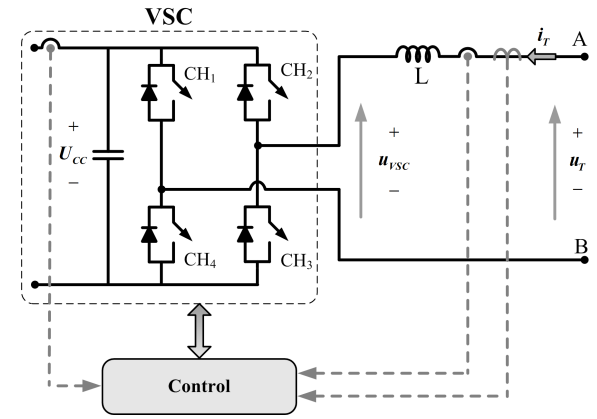


Figure 1: CBCR basic structure.

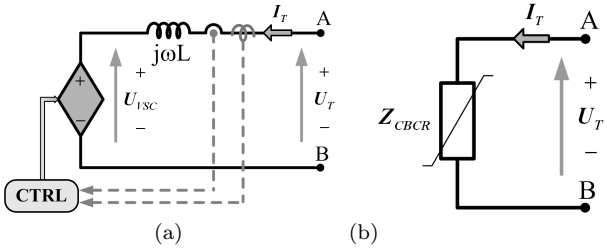


Figure 2: (a) Fundamental frequency model of CBCR and (b) equivalent controlled reactance as seen from the AB terminals.

III. A New Methodology for Reactance Synthesis

As mentioned, all the controllers previously used for the variable reactance synthesis are affected by variation in the input voltage/current. Thus converters operation is limited to scenarios with low voltage/current harmonic distortion. One possibility to overcome this limitation is to use a PLL circuit as proposed by Karimi-Ghartemani and Iravani [16], [17], shown in Fig. 3. In steady-state $y(t)$ represents the fundamental frequency component of the input $x(t)$. The angular frequency ω_0 represents the line base frequency.

This PLL not only tracks phase but also the input signal frequency. It has an additional control loop, that detects the fundamental frequency signal magnitude for the same signal. Dynamics response for this circuit is adjusted using parameters k_1, k_2 and k_3, where k_1 is the main responsible for amplitude detection, and k_2 and k_3 works for obtaining phase and frequency.

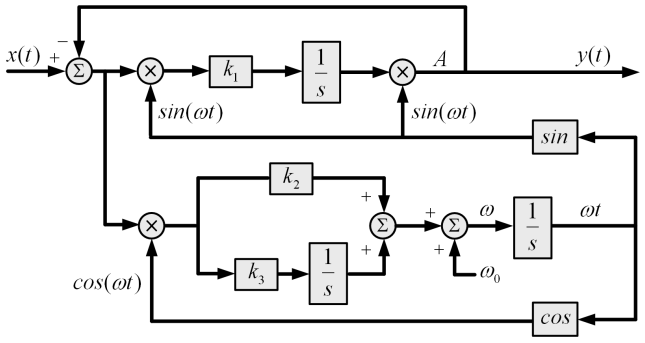


Figure 3: Structure of the Karimi PLL.

With this circuit one obtains the fundamental frequency components of the line current. For this paper, the three-level converter was chosen for synthesizing the controlled reactance, as show in Fig. 4a.

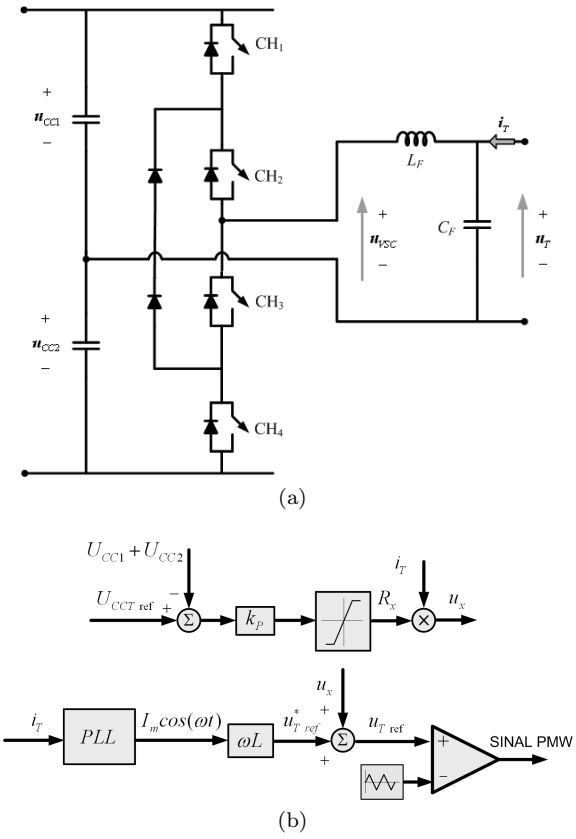


Figure 4: (a) Three-level converters and (b) control logic for converter controller.

Here also is proposed to use a three-level converter based on a *half-bridge* [18], [19], which allows a lower harmonic content in the output voltage and diminishes the stress on the semiconductor switches. The dc link voltage is controlled by u_x signal. The structure of the controller using a PLL circuit is shown in Fig. 4b, the reference

voltage is given by:

$$u^*_{Tref}(t) = \omega\, L\, I_m\, \cos(\omega\, t), \tag{2}$$

and ω is the fundamental angular frequency, L is the inductance to be synthesized by CBCR and I_m is the rms value of the current at the same frequency.

The reference voltage is obtained directly from the product of fundamental current component times ωL that is equivalent to the voltage drop across Z_{CBCR}, the synthesized equivalent reactance.

A test system using three single phase CBCR is used to evaluate the performance of the proposed control scheme when compared to DRS control. This system is depicted in Fig. 5. The parameters of the simulated system was taken from [14] and are given in Table I.

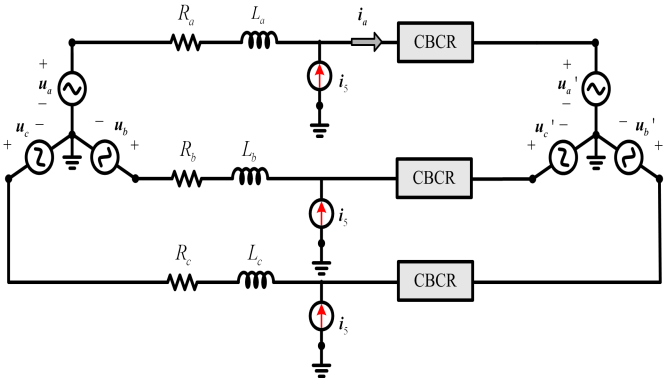


Figure 5: Simulated electrical system.

The current source in the aforementioned figure stands for a 5th order harmonic injection (with magnitude approximately equal to 10 % of the fundamental component). The goal is to assess the system performance under harmonic distortion. From $0 < t < 1$ s the converter have no control order, after $t = 1.0$ s the control order is to synthesize a - 0.16 H (negative) inductance per phase. The converters are controlled to operate only after $t = 1.0$ s.

TABLE I: Circuit parameters.

Inductance: L_a	0.488 H
Resistance: R_a	17.98 Ω
Virtual inductance	-0.16 H
Voltage system 1: u_a	175.0 V
Voltage system 2: $u_a^{'}$	247.5 V

Fig. 6 shows the converter output voltage and the line current for phase a and Fig. 7 shows the instantaneous power and the average power flow for the system, using DRS technique.

In this Fig. 6, it is clear that CBCR is not operating correctly as we can see that approximately the voltage fundamental frequency is in phase with the current fundamental frequency. In the DRS method, theoretically, the controls tries to synthesize a perfect reactance, however the overall frequency response does not allow this.

In Fig. 7, the large ripple on the instantaneous power is due to the presence of harmonic current. After $t = 1.0$ s, as the CBCR is synthesizing a negative reactance the transmitted power should increase. However due to the incorrect operation of the CBCR, this power decreases. It should be point out that the system cannot work properly with the harmonic content as the converter output voltage is heavily influenced by the 5th order harmonic in the current. DRS method synthesizes basically an equivalent reactance valid for a wide frequency spectrum, which is limited mainly by the converter frequency response.

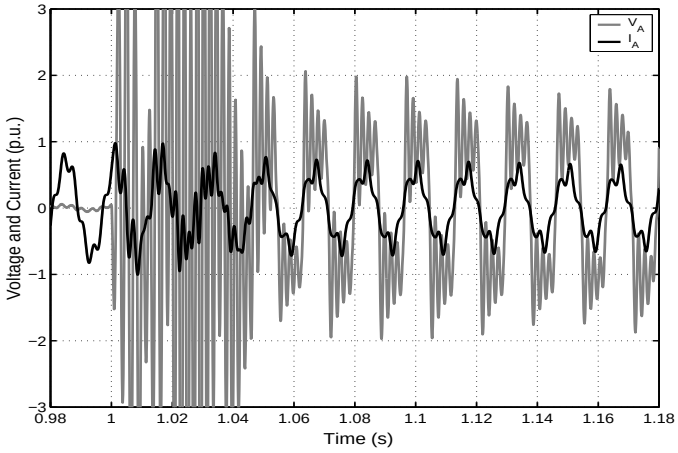


Figure 6: Voltage and line current using DRS method.

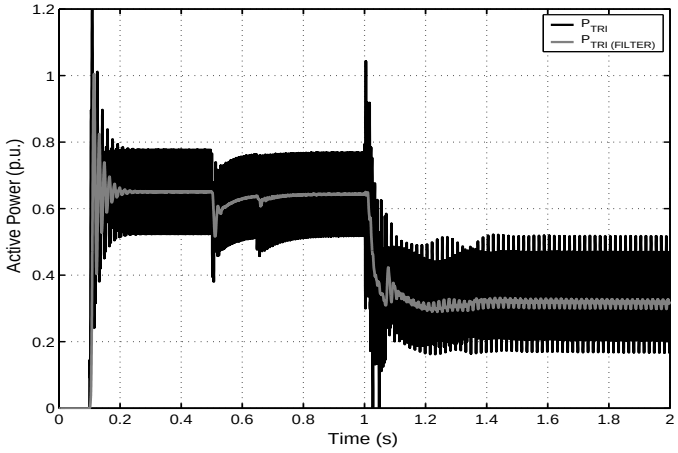


Figure 7: Active power transfer using DRS method.

Fig. 8 shows the converter voltage and current for phase a using the methodology based on PLL, proposed in this paper. Fig. 9 shows the instantaneous active power as well as the average power flow.

The harmonic content does not affect the overall CBCR performance as the PLL circuit provides robustness to the converters control scheme. The use of PLL force the synthesis of the reactance to be realized in a more narrow frequency band. In fact, the PLL used assures that the equivalent reactance is synthesized at the line frequency eliminating the effect of the distortions in the voltage.

IV. IEEE Benchmark Applied to Subsynchronous Resonance Studies

Series transmission lines compensations is recognized as an efficient and economic way for increasing the

transmitted power. However, in some cases, special attention must be taken to avoid instability and assure reliability.

When the system may present subsynchronous resonance (SSR), this compensation has to be carefully designed otherwise it may cause mechanical or electrical problems. In some cases, the incorrect compensation causes a poor damping in some electrical oscillations that can trigger protection systems or damage the equipment.

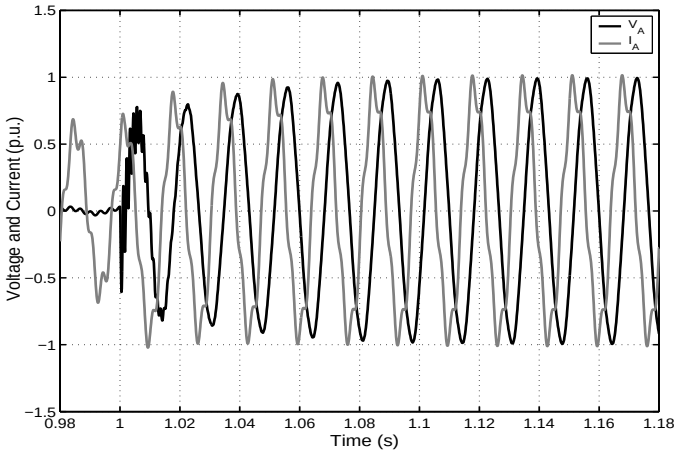


Figure 8: Voltage and line current using the proposed technique.

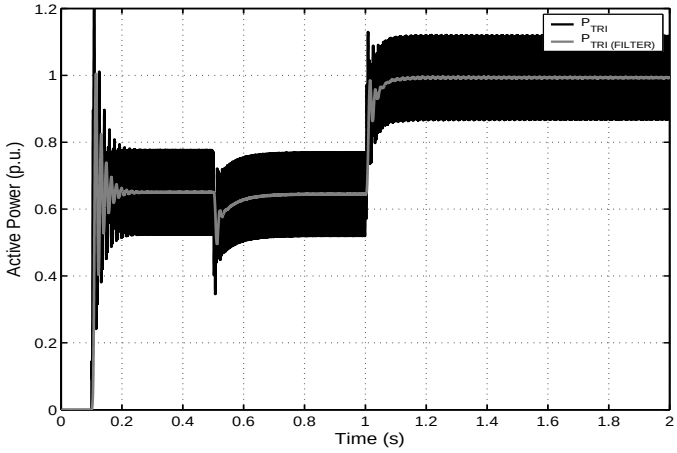


Figure 9: Active power transfer using the proposed technique.

This section presents some results related to transmission line series compensation. The results were obtained using the model referred as "*First Benchmark Model for Computer Simulation of Subsynchronous Resonance*" [15], [20], shown in Fig. 10.

In this model, the generation system is a 892.4 MVA synchronous generator connected to a infinite bus across a transmission line, equipped with capacitive series compensation. This generator is driven by four turbines (two in low pressure, one in medium pressure and one in high pressure), and has additionally rotor and exciter masses [20]. In t=2.5 s, a three-phase fault is applied. This fault is simulated by connecting $X_{fault} = 13.0\ \Omega$ between the three-phases and ground during 75 ms. In this simulation the capacitive series compensation is $X_c = 120.7\ \Omega$, which represents 75 % of the series reactance.

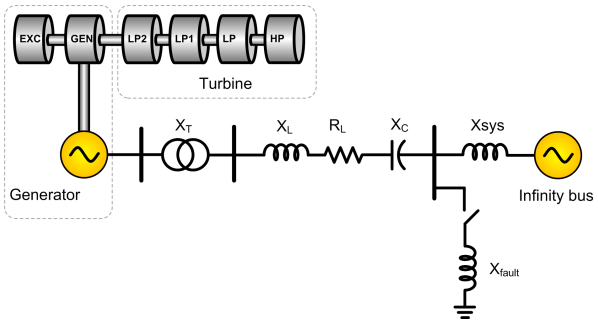


Figure 10: *IEEE First Benchmark* system using capacitive compensation.

The electrical torque and line current are shown in Fig. 11 and Fig. 12, respectively. Due to the series compensation after fault occurs there are low frequencies oscillations in both voltage and current.

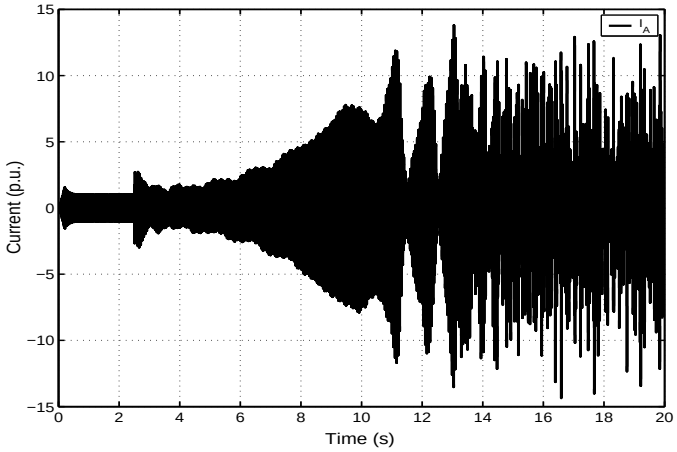


Figure 11: Line current using capacitive compensation.

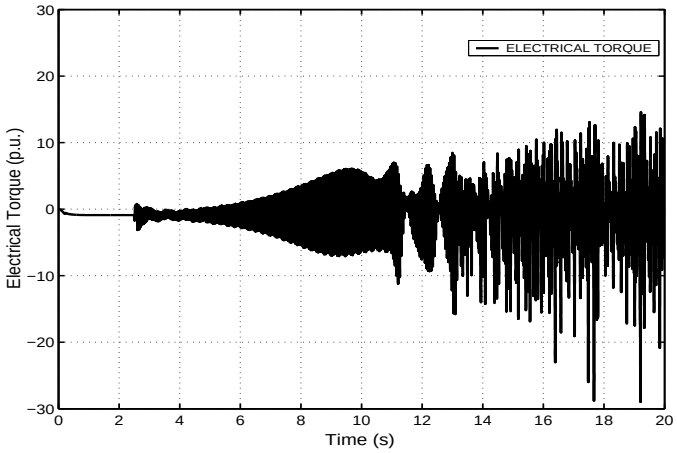


Figure 12: Generator electrical torque using capacitive compensation.

In order to analyze the ability of the CBCR to damp subsynchronous oscillations, the series capacitor bank was replaced by three single-phase CBCRs using the DRS

control, as shown in Fig. 13. In this simulation the CBCR was controlled as to emulate a negative reactance with magnitude equal to the reactance of the capacitor bank in the previous case.

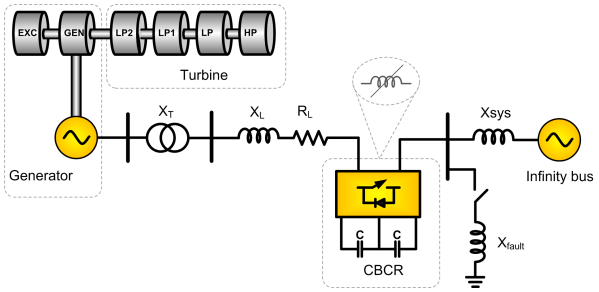


Figure 13: *IEEE First Benchmark* for subsynchronous resonance using the proposed technique.

The CBCR reactance order is the same as the capacitor reactance in the previous simulation. At $t = 2.5\ s$ the same three-phase fault is applied.

Fig. 14 shows the output voltage and current in converter terminals in phase a and Fig. 15 shows the machine electrical torque. The subsynchronous oscillations were mitigated using CBCR converter and the steady state is reached, as can be seen comparing Fig. 14 to Fig. 11. Fig. 14 shows that the line current is stable, however a low frequency oscillation at about 1.2 Hz appears. This oscillation is due the conventional electromechanical system. Possibly, this could be more damped by an specific power oscillation damping control like a PSS (*Power System Stabilizer*) which was not used here. During the transitory, the current in converter terminals is around 1.8 p.u. (as seen in Fig. 14b), making it necessary to overdesign the equipment or use protection mechanisms.

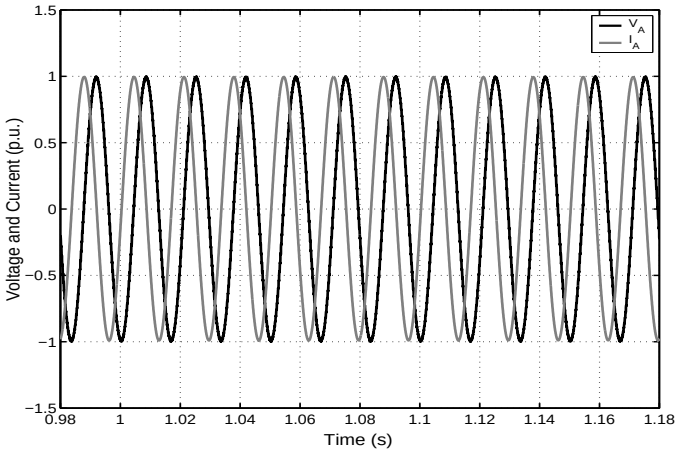
V. Conclusions

This work presented the basic principles for a CBCR. This controlled reactance can be used in transmission line series compensation while mitigating subsynchronous resonance. Previously proposed topologies are limited to configurations were there are low harmonic contents in the system voltage or in the line current. A simple case system was used to illustrate this limitation and a PLL circuit was proposed to allow CBCR operation in a highly distorted system.

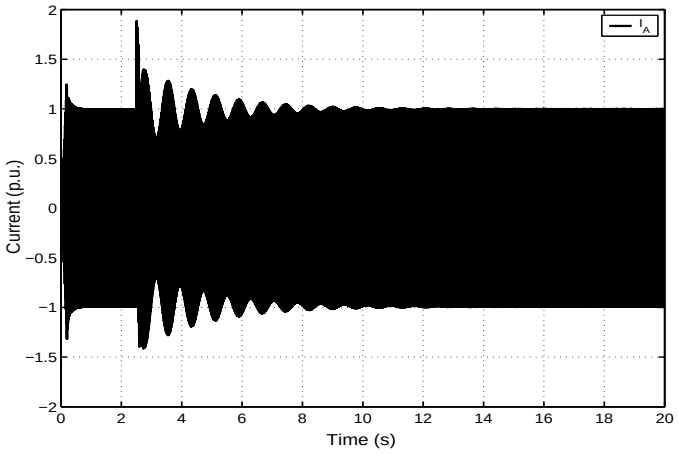
The proposed control scheme allows to synthesize a variable reactance which can be used for reactive power compensation as well as to mitigate subsynchronous resonance. It can bring operational flexibility allowing a continuous controllable compensation. The PLL circuit provides robustness as it allows the controller to be defined only as a function of the power frequency.

To assess the proposed CBCR methodology a simple system with a high content of fifth order harmonic was used. The results are compared with the same system but using a DRS control. Although both cases aim to synthesize the same reactance only the CBCR with PLL circuit was able to do so. Thus it may be used to increase power flow transmission in highly distorted systems. However, high distortion may not appear in steady-state, it may appear during transient and therefore, the proposed methodology may be more robust in these situation.

Finally, the proposed control strategy was applied to "*IEEE First Benchmark*" to mitigate subsynchronous resonance. It provided an adequate power damping eliminating low frequency oscillations in both voltage and current.



(a)



(b)

Figure 14: (a) Voltage and current waveform at converter output and (b) line current (phase a).

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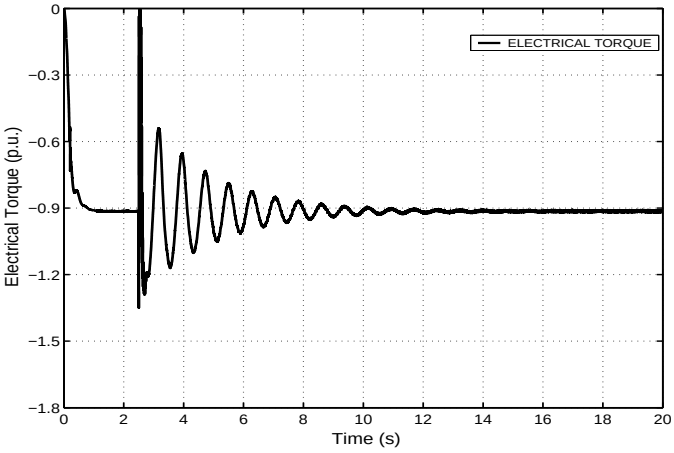

Figure 15: Generator electrical torque using the proposed technique.

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Dr.Watanabe is a member of the Institute of Electrical Engineers Japan, the Brazilian Society for Automatic Control and the Brazilian Power Electronics Society and is a Senior Member of the Power Electronics, Industry Applications and Power Engineering Societies of IEEE. He is also a member of CIGRÈ.