# Single-Phase Active Power Filter Design Using EMTP Simulation

Hye-Yeon Lee, Myong-Bo Shim, Ji-Heon Lee, and Byung-Moon Han\*

*Abstract*—This paper describes a low cost single-phase active power filter for the digital load, such as computers, communication devices, and automation devices. The developed active power filter consists of a half-bridge IGBT inverter and a simple controller with analog circuit to reduce the system cost. The operation of developed active power filter was verified through computer simulations with EMTP. The feasibility of hardware implementation was confirmed by building and testing a prototype. The developed active power filter can offer reduction of power loss and improvement of power quality.

*Keywords*: active power filter, half-bridge inverter, source voltage detection method.

# I. INTRODUCTION

**R**ECENTLY, many digital loads, such as computers, communication devices, and automation devices come into wide use. These devices have a rectifier for AC-DC power conversion, which generates harmonic current and consumes reactive power. The rectifier can be represented by a non-linear load when it is looked into from the source side. The harmonics generated from the non-linear load can be removed effectively by a single-phase active power filter [1]-[2].

Basically there are two methods to generate the compensating current in active power filter, the source voltage detection method and the load current detection method [3]. The load current detection method generates the compensating current directly from the measured load current. In the early days a notch filter or a band-pass filter was used to extract the reference signal from the load current. However, the phase delay of harmonic components brings about the performance degradation of active power filter.

The source voltage detection method generates the compensating current indirectly to make the source current sinusoidal and in phase with the source voltage [4]-[5]. The performance of PLL is very important to determine the performance of whole system. Also, the control stability is a key issue in the controller design [6].

In this research a low cost design of single-phase active

power filter was investigated because many digital loads come into wide use in office and even at home. So, cost reduction is a key point in design, considering installation at office or home. The active power filter was designed using one dual IGBT for inverter and an analog controller with operational amplifiers. Also, source voltage detection method is selected which requires one current sensor and two voltage sensors.

This paper describes a single-phase active power filter with low cost configuration using source voltage detection method. The operation of proposed system was verified through computer simulations with EMTP software, in which the controller is modeled using TACS. The performance of active power filter was confirmed by building and testing a prototype of 2kVA system.

## II. SINGLE-PHASE ACTIVE FILTER

The digital loads, such as computers, communication devices, and automation devices include a rectifier to convert the single-phase AC power to the DC power. The rectifier can be simply represented by the circuit shown in Fig. 1.



Fig. 1. Simplified rectifier circuit for digital load.

The waveforms of DC voltage and AC current are shown in Fig. 2. The DC filter capacitor is very effective to obtain a constant voltage at the DC side. However, it makes the input AC current distorted, in which many low order harmonics are involved. Therefore, the rectifier shows characteristic of nonlinear load.

The input AC current has frequency spectra shown in Fig. 3, using Fourier transform. The magnitude of 3rd, 5th, 7th, and 9th harmonics is respectively about 68%, 28%, 9%, and 7% to that of the fundamental component. These levels are very high compared with the level of higher order harmonics. So, in order to make the input AC current sinusoidal, these low order harmonics should be effectively removed. In this paper it is assumed that the active power filter removes the harmonics of  $3^{rd}$  to  $19^{th}$  order.

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Fig. 2. DC voltage, AC input current.



Fig. 3. Frequency characteristics of input AC current.

Fig. 4 shows the operational principle of active power filter which makes the source current sinusoidal by supplying a harmonic current to the non-linear load.

The input current through non linear load can be expressed by equation (1).

$$i_L(t) = \sum_{n=1}^{\infty} I_n \sin(n\omega t + \theta)$$
(1)

In order to make the source current sinusoidal, the harmonic components with higher order than the fundamental component should be removed by injecting same components from the active power filter.

The source current detection method requires three sensors for measuring the source voltage, the source current, and the DC voltage of active power filter. This method has a simple control structure, but requires a delicate design considering system stability.



Fig. 4. Operational principle of active power filter.

## III. PROPOSED ACTIVE POWER FILTER

Normally, single phase active power filter has low power rating and it is installed at the place close to the load. So, system reliability and low cost are key point in a single phase active power filter.

Fig.5 shows the configuration of a single phase active power filter with a controller which uses a source voltage detection method. The active power filter is designed as a half-bridge inverter using one dual IGBT. The controller has one current sensor for measuring the source current, and two voltage sensors for measuring the source voltage and the DC voltage of active power filter.



Fig. 5. Configuration of single-phase active power filter.

The source voltage is detected and sent to the unit sine wave generator for building the phase angle of reference source current. The DC voltage of active power filter is measured and compared with the reference value. The error is sent to the PI control for calculating the magnitude of reference source current.

The reference source current is compared with the measured source current to generate an error signal. The error signal is sent to the error amplifier for generating the reference voltage of inverter. The reference voltage is compared with the triangular carrier wave to generate the PWM gate pulse for inverter.

# IV. COMPUTER SIMULATION

Many simulations have been carried out to verify the operation and performance of proposed active power filter using EMTP software. Fig. 6 shows a simulation model for the proposed active power filter and the nonlinear load. The power circuit is modeled with voltage controlled switches and passive circuit elements. Major circuit parameters for the single phase active power filter are described in Table I.



Fig. 6. Power circuit for EMTP simulation.

 TABLE I

 CIRCUIT PARAMETERS FOR SIMULATION MODEL

Parameter	Values
Source voltage	110V, 60Hz
Non-linear Load	C=6880μF, R=10, 35Ω
DC capacitor	C=2000µF
Filter reactor	5mH
Switching freq.	6120Hz

Fig.7 shows the configuration of proposed controller which is designed using TACS program. This controller has same structure and operation sequence as described at the control blocks shown in Fig. 5. Major control parameters of the single-phase active power filter are described in Table II.



Fig. 7. Controller configuration for EMTP simulation.

	TABLEII				
PARAMETERS FOR SIMULATION CONTROLLER					
Reference Parameter	Values				
DC voltage	420V				
Кр	70				
Ki	876				
K1	1/120				
K2	-25				

Fig. 8 shows the simulation results based on the developed simulation model. Fig. 8(a) shows the source voltage, source current, and load current waveforms. The source current is very close to the sine wave because the active power filter

compensates the harmonics which are generated in the load. Fig. 8(b) shows the measured value of compensating current which follows the reference value accurately. It is confirmed that the current control is operated accurately. Fig. 8(c) shows the source current when the load changes from 10 to 35  $\Omega$ . The active power filter starts operation at 120ms. The load resistance is changed at 250ms and returned at 380ms. Fig. 8(d) shows the variation of DC voltage. It is confirmed that the DC voltage is maintained with constant value during load change.



(a) Source voltage V<sub>S</sub>, Source current I<sub>S</sub>, Load current I<sub>L</sub>.







## V. HARDWARE PROTOTYPE

A 2kVA hardware prototype shown in Fig. 9 was built and tested to confirm the simulation results and to verify the feasibility of hardware implementation. The prototype is connected with a mid point between the 110V power source and the diode rectifier with RC load. The switching element used in inverter has a rating of 600V/50A dual IGBT and the switching frequency is 8 KHz.



Fig. 9. Prototype single-phase active power filter.

Fig. 10 shows analog controller that was developed using OP Amp and digital logic circuit. This circuit consists of a sine generator, DC control, current control, triangular wave generator, and dead time generator. Sine generator is used for generating the reference value of source current, which is in phase with the source voltage.

The sine generator makes the inverter output current in phase with the source voltage, which offers power factor correction without separate control of power factor. It can generate a unit sine wave without regard to the magnitude change of source voltage.



Fig. 10. Circuit diagram for analog controller.

DC voltage control is required to determine the magnitude of source current. The DC voltage is normally measured by a commercial device AD210AN, which is rather expensive. In this research, a new DC voltage measuring circuit was developed to reduce the system cost. The developed circuit consists of a cheap DC voltage sensor and a differential amplifier using OP Amp.

The current control is to make the source current follows the reference value. So, it measures the source current using CT (current transformer) and compares it with the reference current obtained from the source voltage and the sine generator.

The triangular waveform generator makes the carrier wave for PWM pulse generation. It is designed using Schmitt trigger circuit and Integration circuit. The switching frequency is determined by adjusting the value of resistance.

$$f_0 = \frac{1}{4RC} \left(\frac{R_2}{R_1}\right)$$
(2)

The dead time compensator is needed to remove the short circuit state during inverter switching operation, which is very important in the voltage source inverter. In order to generate the dead time signal, a square wave is processed to get RC time constant. In this experiment the dead time is set to  $4\mu$ s.

Fig. 11 shows the experimental results using the prototype active power filter. Fig. 11(a) shows measured value of source voltage, source current and load current. As explained in the simulation results, the waveform of source current is close to sinusoidal by compensation with active power filter. Also, the phase of source current is almost in phase with the source voltage, which means that power factor is corrected. Fig. 11(b) shows the waveform of compensating current, which is injected by the active power filter.

Fig. 11(c) shows the expanded waveform of load current and its harmonic analysis results. The load current has low order harmonics which has rather high magnitude. Fig. 11(d) shows the expanded waveform of source current and its harmonic analysis results. It is confirmed that the harmonics generated by non-linear load can be removed by the active power filter. Fig. 11(e) shows the variation of source current during the load change from 35 to  $10\Omega$ . It is confirmed that the developed controller operates in stable manner without regard to the load variation.

# VI. CONCLUSION

This paper proposes a low cost single-phase active power filter for digital load, such as computers, communication devices, and automation equipment used at office and home. The proposed active power filter was designed using one dual IGBT for inverter and an analog controller with operational amplifiers.

The developed active power filter consists of a half-bridge IGBT inverter and a simple controller with analog circuit to reduce the system cost. The operation of developed active power filter was verified through computer simulations with EMTP. The feasibility of hardware implementation was confirmed building and testing a prototype.

The developed active power filter can offer reduction of

power loss and improvement of power quality. It can be easily produced using commercially available components.





# VII. APPENDIX

EMTP Code for Single-Phase Active Power Filter



```
C <\!\!\text{-Namexx} + \!\!<\!\!\text{In1--x} + \!\!<\!\!\text{In2--x} + \!\!<\!\!\text{In3--x} + \!\!<\!\!\text{In5--x} <\!\!\text{-GAIN} <\!\!\text{-FXLO} <\!\!\text{-FXHI} <\!\!\text{-NMLO} <\!\!\text{-NMHI}
  IMAG
           +IMA
                                                           1.0
С
88ISR
           = IMAG / 120 * SINR
С
C OUTPUT <-
                                                           <--T-START<--T--STOP
               ---M-
                   ----<----F-----P----
91VTP
                1.0
С
88ISM
           = VTP
C
C COMPARATOR
88DIS
          = (ISR - ISM) * (-25.0)
С
C <\!\!\text{-Namexx} + <\!\!\text{In1--x} + <\!\!\text{In2--x} + <\!\!\text{In3--x} + <\!\!\text{In4--x} + <\!\!\text{In5--x} <\!\!\text{-GAIN} <\!\!\text{-FXLO} <\!\!\text{-FXHI} <\!\!\text{-NMLO} <\!\!\text{-NMHI}
  VCONA +DIS
                                                           1.0 -10. +10.
С
C Switching frequency FS = 6120 Hz
C N : Multiple Number of Switching Frequency
88N
           = 51
C TRIANGULAR VOLTAGE GENERATION
          = SIN (N * WT.I)
88SIN1
           = COS (N * WT.I)
88COS1
88ANG1
           = ATAN(SIN1/COS1)
          = (-1.0 + 4.0 * ABS(ANG1)/PI) * 10.
88VTRI
С
C GATING SIGNAL GENERATION
98SIGA = VCONA.GT.VTRI
98SIGAP = .NOT. SIGA
C
C TACS OUTPUT
C BUS-1>BUS-2>BUS-3>BUS-4>BUS-5>BUS-6>BUS-7>BUS-8>BUS-9>BUS-0>
33SINR PHI VDCM VDCR DVDC DELV IMAG ISR ISM DIS
33VCONA VCONB VTRI SIGA SIGAP VT
                                             AAA
BLANK ENDIND TACS
С
С
==
___
С
             NETWORK SECTION
С
С
C SOURCE CONNECTION CIRCUIT
С
C Source Inductance
C BUS-1>BUS-2>BUS-3>BUS-4><----R<----C
        VTP
                               .032 3.2
  VS
C AC Line Connection
C BUS-1>BUS-2>BUS-3>BUS-4><----R<----C
                                                                                      I
C CPP VPD
                              1.0E-6
  CPP
        VPD
                               0.05 5.0
                                                                                      1
  CPN
         VND
                              1.0E-6
  CPN
                             1.0E-6
С
C NON-LINEAR LOAD MODELING
C Diode Conduction Losses
C BUS-1>BUS-2>BUS-3>BUS-4><----R<----C
                                                                                     I
  VPD D1
                             1.0E-3
                             1.0E-3
  VND D3
  NEGD D4
                              1.0E-3
  NEGD D2
                              1.0E-3
C RC Snubber Circuit
C BUS-1>BUS-2>BUS-3>BUS-4><
                                 ---R<
                                             -C
                                                                                     I
  VPD POSD
                                 33.
                                              1.0
  VND POSD
                                 33.
                                              1.0
VPD NEGD
                                33
                                            1.0
  VND NEGD
                                  33
                                              1.0
C DC Load & Filter Capacitor
C BUS-1>BUS-2>BUS-3>BUS-4><----R-
                                             --C
                                                                                     I
                                        -I <-
  POSD NEGD
                                  30.
                                                                                     3
  NEGD POSD
                                             6600
                                                                                     1
  POSD
                             1.0E + 8
  NEGD
                             1 0E+8
C
C ACTIVE FILTER CIRCUIT
C
C Filter Reactor
C BUS-1>BUS-2>BUS-3>BUS-4><----R<----C
                                                                                     I
  VPI VP
                                0.1 10.0
C AC Line Connection
C BUS-1>BUS-2>BUS-3>BUS-4><----R<----C
                                                                                     I
  NNNN VN
                              1.0E-6
C IGBT Conduction Losses
C BUS-1>BUS-2>BUS-3>BUS-4><----R<----C
                                                                                     I
  POSI Q1
                            1.0E-3
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C DC Filt	ter Capacito	r				
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POSI		1.	.0E+8			
NEGI		1	.0E+8			
NNNN	[		1.0E+8			
С						
BLANK	RECORD E	NDING BRA	ANCHES			
C						
C Current	t Measuring	Switch for Is				
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VD	CDD	100 E 2	0000	0.0		1
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V IN	CFN	100.E-3	9999.	0.0		
C	C 1 D1	D' 1 D'1				
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TID4	VPD					
HD2	VND					
С						
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C Model C -BUS1 13Q1	for 1-Phase >-BUS2><- VPI	PWM Voltag	ge Source Inv	erter >CLOSED<-	>-TACS> II	SIGA
C Model C -BUS1 13Q1 13Q2	for 1-Phase >-BUS2><- VPI NEGI	PWM Voltag	ge Source Inv	erter >CLOSED<-	>-TACS> II	SIGA SIGAP
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C Model C -BUS1: 13Q1 13Q2 C BLANK I C C BUS1-> 14VS C C AC VO C AC VO C AUS1-> 14VS C BLANK I C C C INITIA C BUS 2POSD 2N	for I-Phase >-BUS2><- VPI NEGI RECORD E ltage Source <i<amplitt 156. ENDING SC L CONDIT init-volta + 75 - 75 + 210. - - 210. &gt;BUS-2&gt;1 POSD</i<amplitt 	PWM Voltag NDING SWI e ide <frequence 60 DURCES ION ge&gt; 5. 5. 0. NDCurrent</frequence 	ge Source Invo ITCHES ey <t0 phi0< 0 90. &gt;CapVolta - 150.</t0 phi0< 	erter O=PhiO ge>	>-TACS> II <tstart<tsto -1.0</tstart<tsto 	SIGA SIGAP 19
C Model C -BUS1: 13Q1 13Q2 C BLANK I C C C C C - C C C - C C - C C - S - C - C C - S - S - 2	for I-Phase >BUS2><- VPI NEGI RECORD F Itage Source 156. ENDING SU L CONDIT >init-volta + 75 + 210. >BUS-2>1 POSD NNNN	PWM Voltag NDING SWI de <frequence OURCES ION ge&gt; 5. 6. 0. NDCurrent</frequence 	29 Source Invo TTCHES 20 90. CapVolta - 150. + 210.	erter O=PhiO ge>	>-TACS> II S <tstart<tsto -1.0</tstart<tsto 	SIGA SIGAP p
C Model C -BUS1: 13Q1 13Q2 C BLANK 1 C C BUS1-> 14VS C BUS1-> 14VS C INITIA C BUS> 2POSD 2NEGD 2NEGD 2NEGD 2NEGD 2NEGI 2NNNN 2NEGI 3NEGD 3NOSI	for 1-Phase >BUS2><- VPI NEGI RECORD E Itage Source (I <amplitition 156)<br="">ENDING SG L CONDIT &gt;init-volta + 75 - 210. &gt;BUS-2&gt; POSD NNNN NEGI</amplitition>	PWM Voltag NDING SW1 e ide <frequenc 60 DURCES ION ge&gt; 5. 5. 5. 6. 10. NDCurrent</frequenc 	<pre>ge Source Invo TTCHES :y<t0 phi0< 0 90. &gt;CapVolta - 150. + 210. + 210.</t0 phi0< </pre>	erter O=PhiO ge>	>-TACS> II <tstart<tstor -1.0</tstart<tstor 	SIGA SIGAP p
C Model C -BUSI: 13Q1 13Q2 C BLANK I C C BuSI-> 14VS C C SuSI-> 24050 2NEGD 2POSI 2NNNN 2NEGI C BUS-: 3NEGD 3POSI 3NNNN C	for I-Phase >-BUS2><- VPI NEGI RECORD F ltage Source <i<amplitu 156. ENDING SC L CONDIT  init-volta + 75 + 210. - POSD NNNN NEGI</i<amplitu 	PWM Voltag CNDING SWI e ide <frequence 60 DURCES ION ge&gt; 5. 5. 5. 5. 5. 5. 5. 5. 5. 5. 5. 5. 5.</frequence 	<pre>ge Source Invo TTCHES cy<t0 phi0< 0 90. &gt;CapVolta - 150. + 210. + 210.</t0 phi0< </pre>	erter >CLOSED<- 0=Phi0 ge>	>-TACS> II S <tstart<tsto -1.0</tstart<tsto 	SIGA SIGAP p
C Model C -BUS1: 13Q1 13Q2 C BLANK I C C BUS1-2 14VS C C AC VO C AC VO C BUS1-2 2POSD 2POSD 2POSD 2POSD 2POSD 2POSI 3NEGD 3POSI 3NENN C C OUTPPC	for I-Phase >-BUS2><- VPI NEGI RECORD E Itage Source <i<amplitt 156. ENDING SC L CONDIT init-volta + 75 - 75 + 210. - BUS-2&gt;1 POSD NNNN NEGI JT DATA</i<amplitt 	PWM Voltag NDING SWI e ide <frequence 60 DURCES ION ge&gt; 5. 5. 0. NDCurrent</frequence 	<pre>ge Source Invo TTCHES by<t0 phi0< 0 90. &gt;CapVolta - 150. + 210. + 210.</t0 phi0< </pre>	erter O=PhiO ge>	>-TACS> II <tstart<tsto -1.0</tstart<tsto 	SIGA SIGAP 17
C Model C -BUS1: 13Q1 13Q2 C BLANK I C C C C - C - C - C - C - C - C - C - C	for I-Phase >BUS2><- VPI NEGI RECORD E ltage Source <i<amplith 156. ENDING SU L CONDIT init-volta + 75 + 210. SUS-2&gt;- NNNN NEGI UT DATA &gt;BUS-2</i<amplith 	PWM Voltag NDING SWI de <frequence OURCES ION ge&gt; 5. 6. 0. INDCurrent US-3&gt;BUS-4</frequence 	<pre>ge Source Invo TTCHES by &lt; T0 phi0&lt;</pre>	erter O=PhiO ge>	>-TACS> II <tstart<tsto -1.0</tstart<tsto 	SIGA SIGAP p
C Model C -BUS1: 13Q1 13Q2 C BLANK I C C AC Vo C AC Vo C BUS1-5 2 C AC Vo C C SUS1-5 2 C C 2 NORT 2 NOT 2 NORT 2 NORT 2 NORT 2 NOT 2 NOT 2 NOT 2 NOT 2 NOT 2	for I-Phase >BUS2><- VPI NEGI RECORD E Itage Source (I <amplither 156. ENDING SU L CONDIT &gt;init-volta + 75 - 75 + 210. - 210. &gt;BUS-2&gt;1 POSD NNNN NEGI UT DATA &gt;BUS-2&gt;BUS-2&gt;BUS-2&gt;BUS-2&gt;BUS-2&gt;-BUS-2&gt;-BUS-2&gt;-BUS-2&gt;-BUS-2&gt;1 POSD</amplither 	PWM Voltag NDING SWI de <frequence OURCES ION ge&gt; 5. 6. 0. NDCurrent US-3&gt;BUS-4</frequence 	<pre>ge Source Inv. TTCHES :y<t0 phi0< 0 90. &gt;CapVolta - 150. + 210. + 210. + 210.</t0 phi0< </pre>	erter O=PhiO ge> S-6>	>-TACS> II <tstart<tsto -1.0</tstart<tsto 	SIGA SIGAP p
C Model C -BUS1: 13Q1 13Q2 C BLANK 1 C C AC Vo C BUS1-> 14VS C BLANK 1 C C INITIA C BUS: 2POSD 2NEGD 2NEGD 2NEGD 2NEGD 2NEGD 2NEGD 2NEGD 2NEGD 2NS1 3NEGD 3NEGD 3NEGD 3NEGD 3NEGD 3NEGD 2NS1 2NNNN C C BUS-1: VTP BLANK 1	for I-Phase >-BUS2><- VPI NEGI RECORD F ltage Source <i<amplitt 156. ENDING St L CONDIT &gt;init-volta + 7 75 + 210. - 210. &gt;BUS-22- POSD NNNN NEGI UT DATA &gt;BUS-2&gt;BI VS ENDING N</i<amplitt 	PWM Voltag CNDING SWI e ude <frequence ge="" ion="" ources=""> 5. 6. 100. UNDCurrent US-3&gt;BUS-4 ODE VOLT4</frequence>	<pre>ge Source Invo TTCHES by<t0 phi0< 0 90. CapVolta - 150. + 210. + 210. + 210. &gt;BUS-5&gt;BUS</t0 phi0< </pre>	erter 0=Phi0 ge> 5-6> Г	>-TACS> II <tstart<tsto -1.0</tstart<tsto 	SIGA SIGAP pp

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