Testing a Virtual Synchronous Generator in a Real Time Simulated Power System

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***Abstract*— In this paper the approach to test a real hardware Virtual Synchronous Generator (VSG) is presented. The purpose of a VSG is to substitute the rotational inertia of synchronous generators. The development of such a device starts in a pure simulation environment and extends to the practical realization of a VSG. Testing a real hardware VSG is a complicated matter since its place is within a power system. However, by replacing the power system with a real time simulated one, this complexity is reduced. The VSG then interacts with the simulation through a power interface. The advantages of such a laboratory test-setup are numerous and should prove beneficial to the further development of the VSG concept.**

***Keywords*: Virtual Synchronous Generator, Real-Time Digital Simulator, Power Interface.**

I. Introduction

FREQUENCY stability in power systems is secured mainly by the large rotational inertia of synchronous machines which, due to its counteracting nature, smoothes out the various disturbances. The increasing growth of small scale dispersed generation will cause the so-called inertia constant of the power system to decrease. This may result to the power system becoming instable [1]-[3]. A promising solution to such a development of events is the Virtual Synchronous Generator (VSG) [4]-[7]. Three distinctive components, namely a power processor, an energy storage device and the appropriate control algorithm, are brought together to replace the lost inertia with virtual inertia [4] as shown in Fig. 1.

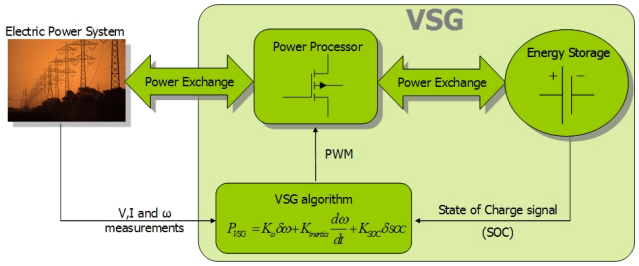

Fig. 1. The VSG Concept

A VSG algorithm has been developed and tested in a power system model in Matlab/Simulink [20] with promising results. This Matlab/simulink VSG algorithm is directly implemented on the Triphase® [8],[9] inverter system through a dedicated FPGA interface developed by Triphase®.

In order to test the hardware implemented VSG and study its effects within a power system, it is interfaced with a real time digital simulator from RTDS® [16].

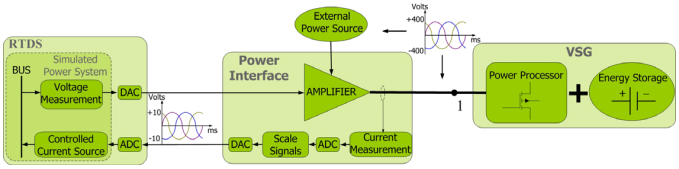

Fig. 2. RTDS and Power Interface and VSG in a closed loop

The RTDS® simulates power systems in real time and is often used in closed loop testing with real external hardware because of the Analogue to Digital and Digital to Analogue Converters (ADC, DAC) it is equipped with. Keeping in mind that these ADCs and DACs have a dynamic range of ±10V max rated at 5mA max and the Triphase® inverter system is rated at 16kVA, it is clear that a power interface has to come in between to make this union possible as it is shown in Fig. 2.

Such a power interface is available again from Triphase® and its main function is to replicate the voltage waveform of a bus in a network model to $400V_{LL}$ at terminal 1 in Fig. 2. The current flowing from/to the VSG is fed back to the RTDS, to load the bus in the network model with that current.

The simulated power system is a transfer from the Matlab/Simulink environment to RSCAD [17] format.

This paper demonstrates how this laboratory test setup is realized, explaining the control algorithms employed both for the power interface and the VSG. Finally both the results of the Matlab/Simulink simulations and the test setup are presented.

II. Approach

The VSG as a concept is fairly new and its role within a power system is currently under investigation. The VSG principle has been proven through Matlab/Simulink simulations and a chance is given to test a real hardware VSG. The operation of the real hardware VSG has been partly tested in [7] but not the effect it is purposed to have on a grid.

To better study and witness the effects of virtual inertia, the VSG should be tested within a power system of which the structure contains at least the basic characteristics such as generation/transmission facilities and loads [18]. In the real world this system, would be a power grid which comprises at least 2 Synchronous Generators each coupled to a turbine-

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governor configuration as it is illustrated in Fig. 3.

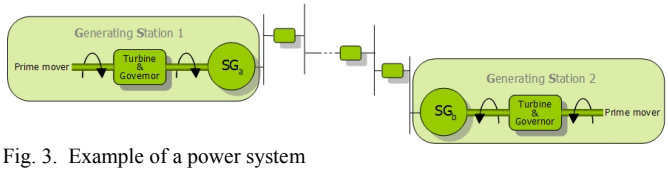

Fig. 3. Example of a power system

Having such a system available and to be able to repeat the tests in order to verify and optimize the performance of the VSG is fairly costly and the complexity of assembling and operating such a system forces us to find other solutions.

The above mentioned problems and concerns are put to rest since the employment of the RTDS allows for power system simulation in real time with the capability of repeatability of tests.

Another major advantage of using the RTDS is scalability of signals. Whereas the VSG implemented in the Triphase platform is rated at 16kVA, the simulated power system can be rated in the order of GWs.

A VSG acts on a power systems frequency by either injecting power to it or by absorbing power from it. This is done in a specified manner so as to emulate a synchronous machine's rotational inertia which will be explained later. In order for the power system to be influenced by this power injecting/absorbing action, the power system it self must have a droop characteristic that relates frequency to power. This droop characteristic is inherent to power generating stations (GS) [18] with a synchronous generator (SG) as the power generating stage which reflects to the rest of the power system.

It is well known from [18] that a frequency/power dependency exists and can be described by the following expression:

$$\Delta P = K_{pf} \Delta f \tag{1}$$

Note that $1/K_{pf}$ is often called droop and it is denoted by R.

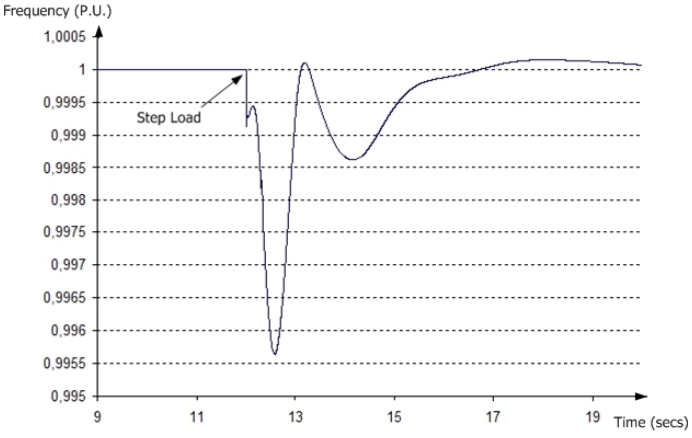

Fig. 4. Frequency slowly returning to steady state after a step load

Of course the total frequency behavior of the power system is defined by many factors with the most important being the controls inside the GS.

Fig. 4 gives an example of the frequency of a power system being in steady state until the moment a step load increases the demand for power. Due to (1) the frequency immediately drops and then the GS controls restore the balance by increasing the power output of the SG. A steady state is achieved after a noticeable amount of time due to the slow dynamics associated with GSs.

The objective of this paper is to prove that the real hardware VSG can decrease the size of these frequency deviations that are caused by load variations.

III. Description of the Test Setup

A. VSG

A VSG's ultimate role is to increase the inertia constant of a given power system. The total inertia constant J of an SG is defined by the equation of motion [19] in (2).

$$\frac{d\left(\frac{1}{2}J\omega^2\right)}{dt} = P_m - P_e \tag{2}$$

Here P_m is the mechanical power, P_e is the electric power and ω is the angular velocity of the rotor. Setting P_m-P_e=P_{VSG} and expanding (2), a basis is set for how a VSG should handle active power as shown by equation (3).

$$P_{VSG} = K_i \frac{d\omega}{dt} \tag{3}$$

Equation (3) indicates that power will be generated or absorbed by the VSG according to the positive or the negative rate of change of frequency (ROCOF). Clearly K_i acts as an amplifying constant and should be set as such, so that the VSG exchanges its maximum active power when the maximum defined ROCOF (1Hz/sec) occurs. K_i should also be negative in order to be counteracting to the direction of the rate of change and that in effect is how virtual inertia is emulated by a converter.

Nonetheless, since $d\omega/dt$ is by nature an error signal because the balance point is at zero, power will be exchanged only during the transient without guarantying that the frequency of the power system will return to the desired stable state i.e. 50Hz. In order to observe the above and have the VSG act accordingly, a frequency droop part should be added to (3) which becomes:

$$P_{VSG} = K_\omega \left(\omega - \omega_{ref}\right) + K_i \frac{d\omega}{dt} \tag{4}$$

In (4) the reference value of frequency i.e. 50Hz or 1 in per unit is always subtracted from the measured frequency. This creates an error signal whenever there is a frequency deviation within the power system. K_ω is chosen so that the P_{VSG} will equal the nominal power of the VSG when the frequency deviation is at its maximum (2.5Hz).

Examining (4) and with respect to Fig. 1, clearly indicates that power should flow in both directions, from energy storage device to power system or from power system to energy storage device. So in effect a VSG can either act as a load or as a generator dictated by the frequency disturbance and (4).

Normally a state of charge (SOC) part should be added to the control equation as it is demonstrated in Fig.1, to maintain the charge level of the storage device such as a battery, flywheel or supercapacitor, so that it will not be depleted or over charged. For the purpose of this test though and in order to reduce the complexity of the experiment, the energy storage device is assumed to have an infinite amount of charge. This is

achieved by employing a DC power supply with a resistor connected across its output as shown in Fig. 5.

Fig. 5. A DC power supply and resistor in parallel, emulates an energy storage device with infinite amount of charge. The resistor acts as an energy sink when power is send back to the energy storage device.

In Fig. 1 one of the components of the VSG is the power processor which stands in between the energy storage and the targeted power system. Since the power system is a three phase ac network and the energy storage is a dc device, the power processor must include two power conversion stages, namely a DC to DC stage and a DC to AC stage. Here, both DC to DC and DC to AC have bidirectional power handling capabilities.

The power processor [8] from Triphase fits the VSG description due to the layout of its power electronic components as it shown in Fig. 6.

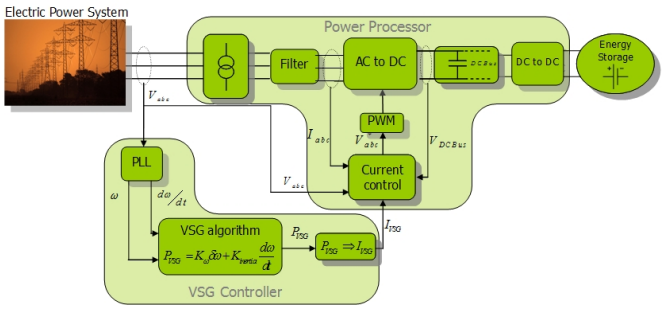

Fig. 6. Configuration of a VSG unit consisting of a power processor an energy storage device and a VSG controller.

Fig. 6 also illustrates the various control components that are indispensable to the VSG operation. The inputs of the VSG algorithm are ω and $d\omega/dt$ that derive from a phase locked loop (PLL) [21] which is locked to the electric power system voltage waveform. A power P_{VSG} signal is produced according to the magnitude of ω and $d\omega/dt$ which then has to be converted in to a current signal I_{VSG} to be fed into the 'current control' block. The 'current control' block takes into account and compensates for the filter and thus turns the ac output of the power processor in to a controlled current source.

B. RTDS

The RTDS simulates power systems in real-time, through a parallel processing architecture that is dedicated to that purpose.

The modular structure and technical details of the RTDS are explained in [12], [13] but a short technical description will be given in terms of performance that is relevant to the task at hand.

A RTDS assembly may consist of many racks which in their turn consist of communication and processor cards (circuit-boards). The processor cards and more specifically the Triple Processor Cards or 3PCs contain three processors A, B and C that share the same memory. Simulation components can be assigned to dedicated processors, as well as to the cards that accomodate the ADCs and DACs.

A plethora of ADCs and DACs is made available in order to interact with the simulated power system as well as monitor its status with external hardware. The particular ADCs and DACs that are of interest for this experiment are the Optical Analogue to Digital Converter cards or OADC and the Double fiber Digital to Analogue Converter cards or DDAC. The OADC is able to take a sample of an incoming analogue signal every 4μs (fastest) with a 16bit resolution. The DDAC can reconstruct the outgoing analogue signal at a 2.5μs (fastest) rate again with a 16bit resolution. The dynamic voltage range of both incoming and outgoing signals is ±10V, so the 16bits resolution in terms of voltage is 305μV. Each OADC card has 6 input channels and each DDAC has 12 output channels. This experiment requires only 3 input and 3 output channels.

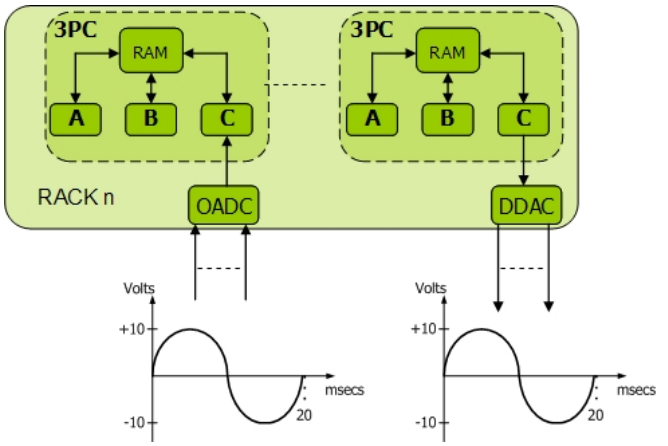

Fig. 7. Rack on RTDS: the OADC and DDAC are directly linked to the processors of the 3PC cards.

These conversion rates are the maximum available but the simulation time step is typically around 50μs for the 3PCs, which is more than adequate to sample or reconstruct a sinusoidal signal that oscillates around 50Hz. Making sure that the OADC and DDAC are assigned to different processors (Fig. 7) assures an almost simultaneous import and export of signals.

The RTDS has traditionally been used for testing power system protection devices [14] or for testing the operation of external hardware devices that control specific components in a power system [15].

For this experiment the RTDS is used somewhat differently. The power system has to be influenced by external hardware either by injecting power in the same way as a synchronous generator would or by absorbing power as a load would. This power injecting/absorbing action requires direct access to the simulated 3phase lines of a specific bus within the simulated power system.

RSCAD, the graphical user interface of RTDS, as with most power systems simulation software, has a power systems components library. Within this library a 'controlled current source' is available. This is a generic method of informing the simulated model that there is a power injecting/absorbing action occurring. The input signal of the 'controlled current source' specifies the amount of power being handled as well

as its direction. This 'controlled current source' can be driven directly by an incoming sampled input signal from the OADC card.

The block 'OADC analogue input' is directly linked to the OADC card. On the right hand side of Fig. 8, the 'DDAC analogue output' block is directly linked to the DDAC card.
It is established that the RTDS can export signals that are scaled versions of the measured voltages from nodes within the simulation.

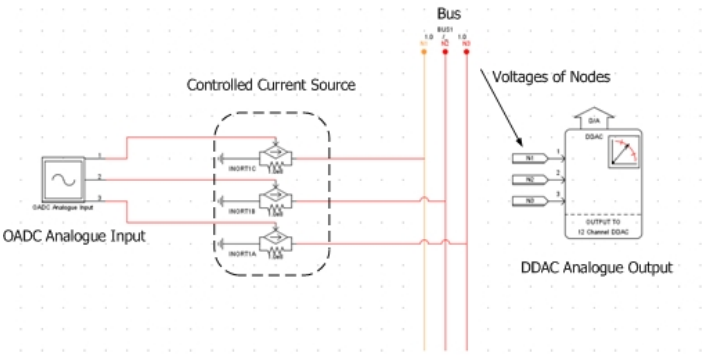

Fig. 8. Simple model in RSCAD

It is now possible to amplify these signals with the power interface and create a three phase ac grid at a convenient voltage level.

C. Power Interface

The power interface bridges the gap between the small, low power signal exchange capabilities of the RTDS and the high power needs of the VSG. It is equipped both with power electronics matching the power rating of the VSG at 16kVA as well as with ADCs and DACs. These ADCs [10] and DACs [11] are capable of handing incoming and outgoing analogue signals with a ±10V dynamic range; hence there is an immediate compatibility with the ADCs and DACs of the RTDS. The resolution is at 16 bits and the conversion time is around 40μs, enough to deconstruct and reconstruct a 20ms sine wave without noticeable latencies.

Referring to Fig. 2, voltages are measured at a BUS of interest within the simulated power system and exported as described earlier. The power interface receives the incoming signals from the RTDS and has the available energy, obtained from the laboratory power grid, to amplify these signals. As a result, a grid is created on one end of the power interfaces that has a voltage balance point of $400V_{LL}$ oscillating at the frequency of the incoming signals.

This amplification/grid creation procedure is made possible again due to the layout of the power electronic components of the Triphase platform. The layout is almost identical to the platform used for the VSG realization but instead of a DC to DC converter, there is another AC to DC. The scheme is depicted in Fig. 9.

The DCBus is common for both AC to DC and DC to AC converters that have bidirectional power handling capabilities. The DC to AC converter (right hand side of Fig. 9) is connected to the laboratory power grid which is a 3 phase $400V_{LL}$ 50Hz grid. Through that converter the DC Bus is charged up to a desired level, and then this energy is immediately available for the AC to DC (left hand side of Fig. 9) which is driven by the v_{ABC} reference signals.

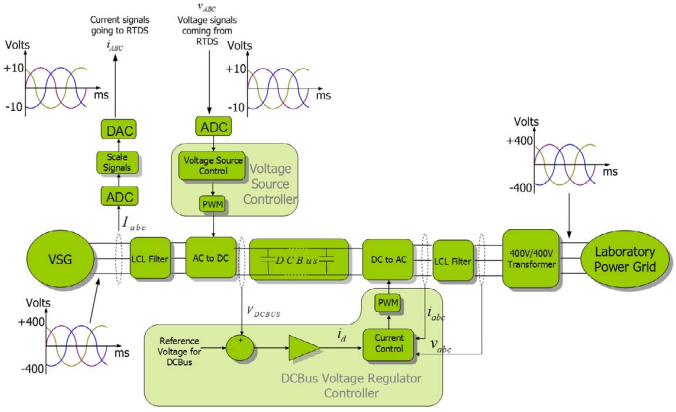

Fig. 9. Components layout and controls of Power Interface.

D. Closed Loop Operation

Fig. 10 illustrates in blocks of operation the test setup as it is in a closed loop and it is a developed version of Fig 2. The 'simulated power system' in the RTDS block is the simulated network used for this experiment and will be explained in the next section.

Starting from the top of Fig. 10, the power system is at a steady state and the frequency is at 50Hz. The v_{ABC} reference signals, that are scaled versions of the voltages at the point of measurement, define the dynamic shape of the voltages at the grid creating side of the power interface but not the behavior. The VSG, in simple terms, will either inject power or absorb power and that action should not be influenced in any way by the power interface. For that reason the AC to DC converter (left hand side of the power interface Fig. 10 and 9) is set to operate as a voltage source meaning that its behavior towards power exchange is passive allowing exclusively the VSG to dictate how much power is injected or absorbed, according to the frequency disturbance.

As soon as the 'varying load R' value is changed in steps, the frequency of the simulated power system deviates from the steady state. This is picked up by the PLL of the VSG initiating the power injecting/absorbing action. When this VSG action occurs, power can be extracted from the laboratory power grid i.e. over-frequency disturbance, or can be pushed into the laboratory power grid i.e. under-frequency disturbance.

This is achieved by setting the DC to AC converter (left hand side of the power interface in Fig. 10 and 9) to act as a voltage regulator for the DCBus. The DC to AC converter monitors the DC bus voltage level and always tries to keep it stable at the predefined voltage reference, which is usually chosen to be around 640-660V, to also satisfy the stable operation requirements of AC to DC converter (right hand side of the power interface Fig. 10 and 9).
In the case where the VSG pushes power, the DC Bus voltage of the power interface will start to rise forcing the DC to AC converter (right hand side of the power interface Fig. 10 and 9) to extract energy from the DC bus keeping the voltage level to the predefined reference. In the case where the VSG absorbs power, the DC bus voltage level will start to fall

causing the DC to AC converter (right hand side of the power interface Fig. 10 and 9) to add energy in to the DC bus again in an attempt to keep the voltage level of the DC bus to the predefined level.

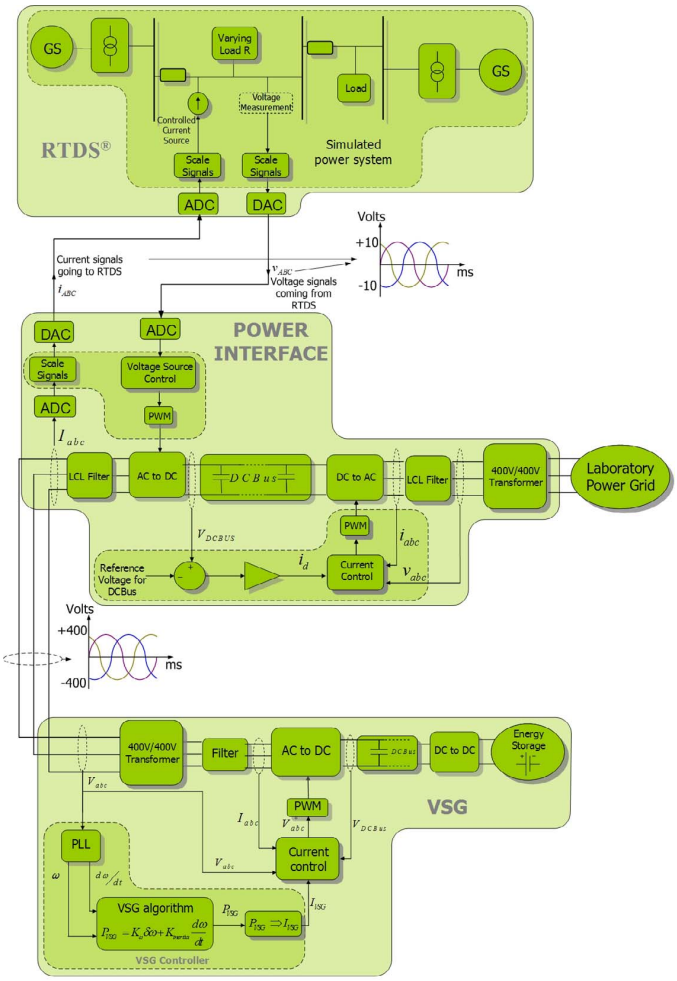

Fig. 10. Expanded version of RTDS, Power Interface and VSG in a closed loop shown in Fig. 2.

During the power exchange, the current that flows between the VSG and the power interface is constantly measured by the latter. Scaled versions of these measurements are sent back to the RTDS that, after another scaling process to match the rating of the simulated power system, control the current source and the simulation is informed of the VSG action.

IV. Simulation and Lab Results

A. Matlab/Simulink Results

Before testing the real hardware VSG with the RTDS, (3) is tested in a Matlab/Simulink environment since it is the origin of the power system which is shown in Fig 11. The test network comprises two generating stations (Fig. 3) feeding power to a simple three bus system. A pure resistive load R changes its value every 60 seconds causing the frequency of the power system to deviate from the 50 Hz.

The loads power absorbing capabilities are between 0% and 7% of the total power of the two SGs. The VSG is rated at 2% of the total power of both the SGs.

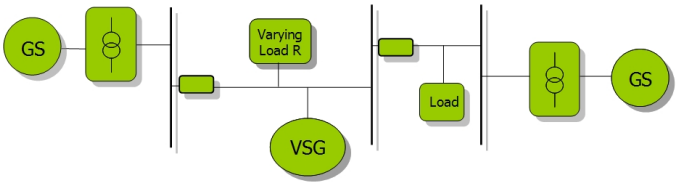

Fig. 11. Power_System in Matlab/Simulink

As mentioned before the constants K_ω and K_i are defined as:

- $K_\omega = P_{VSG\_nom} / 2.5$ Hz
- $K_i = P_{VSG\_nom} / 1$ Hz/s

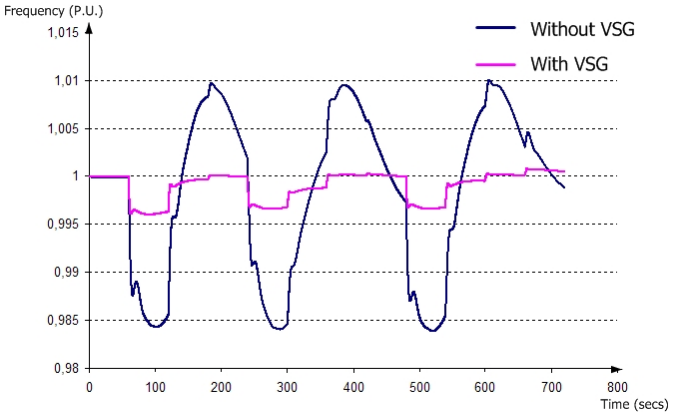

Fig. 12. Matlab/Simulink results: the frequency deviations decrease substantially with employment of the VSG

Fig. 12 illustrates the results of the simulations where the effect of the VSG is clearly apparent as the frequency deviations reduce in size. A similar result is pursued with the laboratory test setup.

B. Laboratory Results

The results from the test setup shown in Fig. 10 are presented in Fig. 13. The specifications of the network, the load and the VSG are identical to what was used in the previous section.

Three separate runs of the experiment were made, one without VSG, a second with a VSG and a third with a VSG but with constants K_ω and K_i doubled. The x-axis of the graphs is in data points which are obtained every 1,25ms.

In Fig. 13, the graph a shows the value of the resistive load as it changes and graphs b, c and d show the frequency response of the power system to these changes. It can be observed that there is a misalignment between the graphs. That is because each graph is from a separate run and there is no mechanism at the moment to completely synchronize the data-logging between each run. In order for the reader to be able to trace the frequency deviations to the respective load changes, numbers have been added.

Graph b in Fig 13 shows how the frequency of the power system deviates, due to the load step changes, when there is no VSG present. By comparing these results with those obtained

from Matlab/Simulink (Fig. 12), a different frequency response is observed. This is due to the fact that the SG controls in RSCAD have a faster reaction time than those in Matlab/Simulink. Although the response could probably be matched, by tuning the parameters of the turbine-governor, either in RSCAD or in Matlab/Simulink, it is not crucial at this stage of the research. The performance of the VSG is proven on the fact that it can decrease the size of the frequency deviations caused by load variations

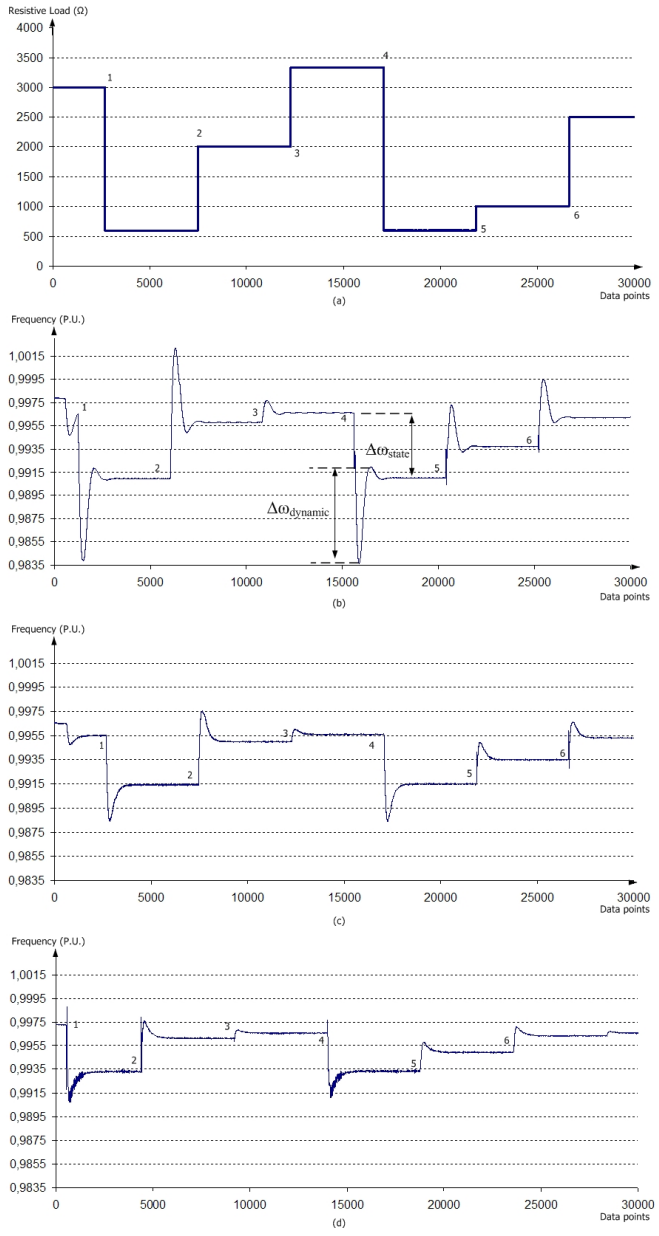

Fig. 13. Laboratory results: a) Load, Frequency response b) Without VSG, c) With VSG, d) With VSG and constants K_ω and K_i doubled.

Looking at graphs c, d and comparing them with graph b of Fig. 13, the utilization of the VSG indeed decreases the size of the frequency deviations. As a measure of performance we can distinguish two indicators. One is the $\Delta\omega_{state}$ which is the distance between two successive steady states and a second one is the $\Delta\omega_{dynamic}$ which is the size of the first frequency oscillation before it settles to steady state. Comparing now graphs c and d, it is seen that by increasing the constants K_ω and K_i, the $\Delta\omega_{state}$ and $\Delta\omega_{dynamic}$ decrease further and the following graphs in Fig. 14 can be produced.

Increasing K_ω and K_i means that more power will be either injected or absorbed for the same amount of frequency deviation and ROCOF respectively.

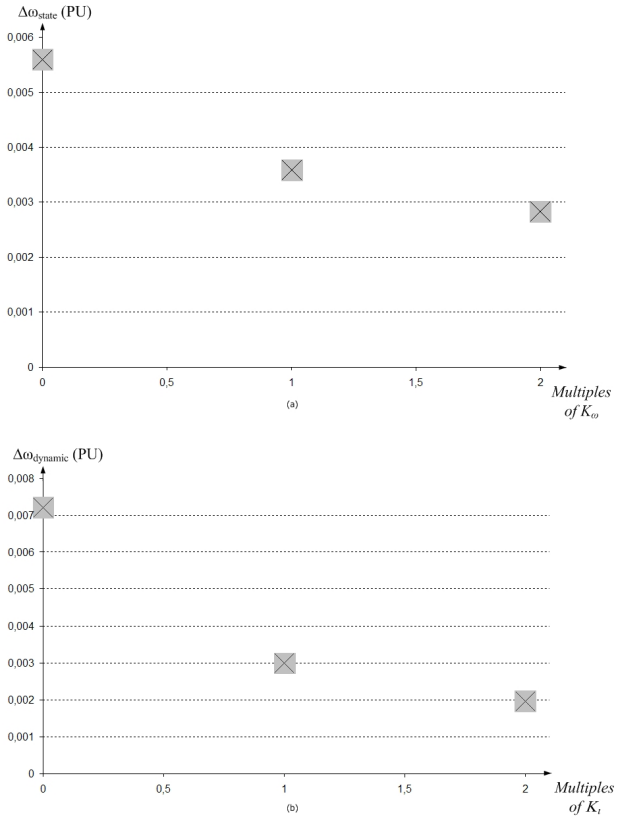

Fig. 14. a) $\Delta\omega_{state}$ decreases as K_ω increases and b) $\Delta\omega_{dynamic}$ decreases as K_i increases.

V. Conclusions

This paper describes the approach taken to test and verify the operation of a real hardware VSG. The laboratory test setup involves a power system that is simulated in real-time and interacts with the VSG through a power interface. The VSG successfully decreased the amplitude of the frequency deviations within the simulated power system induced by load variations. Furthermore, we can differentiate between the reduction of the distance of consecutive steady states due to the frequency droop part of (4) by 35% and damping of oscillations prior to settling to a steady state due to the inertia emulation part of (4) by 58%. By doubling the constants K_ω and K_i of (4) results in an enhanced VSG effect by an additional reduction of 13% and 14% respectively.

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