Loss Estimation of Modular Multi-Level Converters using Electro-Magnetic Transients Simulation

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Abstract—The power losses of the Modular Multi-level Converter (MMC), recently introduced for HVDC transmission are evaluated in this paper. The paper discusses the two capacitor voltage balancing algorithms that have been proposed for the MMC operation based on; (a) ranking of capacitor voltage values and (b) pulse-width modulation (PWM) and the impact of control methods for the MMC on the power losses is also studied. The paper also compares the operating losses of MMC converter with the two-level conventional voltage sourced converters (VSC). In this paper, all type of converters power losses are estimated using a recently developed electro-magnetic transients simulation (EMT) model for accurate representation of switching losses and thermal performance in power electronic systems.

Keywords: **Converter Power Losses, Modular Multi-level Converter (MMC), Voltage Sourced Converters (VSC), Electromagnetic Transients (EMT) Simulations.**

I. INTRODUCTION

THE newer voltage-sourced converter based HVDC (VSC-HVDC) technology is becoming more competitive for intermediate power levels up to a few hundred MW [1]. In comparison with conventional line commutated thyristor based converters (LCC), VSC-HVDC transmission systems exhibit enhanced technical features that can cope with the requirements of modern power transmission systems. The VSC converter can operate in weak or even passive ac systems and does not require reactive power support from the ac grid. And also, VSC-HVDC system can independently control active and reactive power exchange with the ac system [2].

Till recently, VSC-HVDC systems have been based on two- or three-level technology which enables two or three different voltage levels to the ac terminal of the converter. As a result, high and steep level changes are applied at the converter ac terminal hence extensive filtering measures are required [3]. In order to lower harmonic distortion, pulse-width modulation (PWM) techniques are used in voltage synthesis whereas, most of these methods require a very high switching frequency to obtain the very advantage of improved harmonic performance. This causes considerable power losses and eventually, reduces the total efficiency and substantially increases the total cost of the VSC-HVDC project [4].

Instead of two- or three-level technique, the use of multi-level converters can significantly reduce the switching losses [3]. These converters synthesize a stepped ac waveform resembling a sine wave, by stacking fixed magnitude voltage steps on top of each other. A newly introduced multi-level converter for high voltage application is the modular multi-level converter (MMC). The VSC based MMC was initially developed using H-bridge modules for STATCOM

applications [5].

The MMC topology has been recently emerged as a promising technique for VSC based high voltage, high power transmission systems after the introduction of AC/DC conversion with half IGBT/diode bridges [6]. This topology is designed to avoid connecting the devices in series that has been a problem of most of other multi-level topologies. The MMC consists of a stack of identical sub-modules, each with two IGBT switches and a dc capacitor as shown in Fig. 1(a). By suitably controlling the two switches in the sub-modules, a multi-level ac voltage waveform can be synthesized as shown Fig. 1(b). As the multi-level converter output voltage can assume several discrete levels, the harmonic content is low hence, the filters are not required. An inclusion of more sub-modules increases the voltage and power ratings of the converter. The topology is designed to make low voltage stresses on each switching devices. Therefore, MMC can conceptually exploit the potential of conventional (two- or three-level) VSC-HVDC schemes to the best.

Each sub-module capacitor voltage provides one step in the resulting multi-level ac waveform. Therefore, it is required to maintain the capacitor voltages at a constant value using an internal control unit. The function of this capacitor voltage balancing controller is to generate firing pulses for each sub-module to maintain the sub-module's capacitor voltage at a constant value. Therefore, the number of IGBT switching operations required in a power cycle is mainly determined by the capacitor voltage balancing algorithm. Hence, the IGBT switching loss, which is a major contributor to the converter power loss, depends heavily on the voltage balancing algorithm.

An accurate estimation of converter losses is an important step in the thermal management system design [7]. One of the
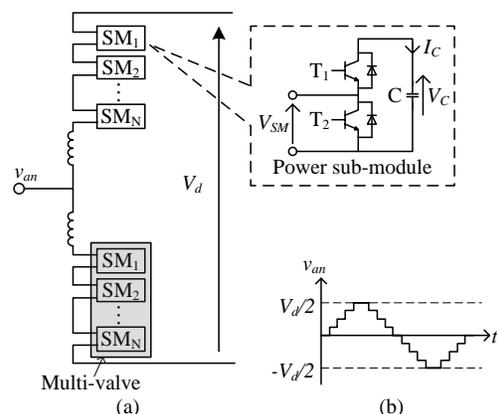
Fig. 1. (a) Schematic diagram of an MMC phase unit and (b) MMC output waveform for 10 sub-modules per multi-valve (*N*=10).

methods used for estimating MMC switching losses is the post-processing the results of time domain simulations [8]. If the VSC's ac output waveforms are assumed to be ideal, analytical estimation has also been used [9]. These methods are well suited to estimate the overall converter efficiency. However, they do not typically assess the converter losses during the startup and other transients. This paper investigates the operating losses of the MMC converter using a recently developed approach [7] that considers only the pre- and post-switching voltage and current values, and estimates the wave-shape between these instants using interpolation. Information required to conduct the interpolation can be obtained from datasheet values. The switching power loss is then readily calculated by multiplying these estimated waveforms.

Using this approach, the MMCs losses can be estimated for steady-state as well as transient and abnormal operating conditions. The impact of control methods on the losses is also investigated. The paper also compares the operating losses of the MMC based systems with the more common two-level VSC-based HVDC system.

II. Modular Multi-level Converter Topology

A. Output Voltage Synthesis

A phase unit of MMC consists of two; upper and lower multi-valves, each with a number (N) of half bridges known as sub–modules (SM$_j$). The sub-module terminal voltage, V_{SM} can have either the capacitor voltage, V_C or 0 depending on the switching states of T_1 and T_2 (1):

$$V_{SM}(t) = \begin{cases} V_C & \text{............... if } T_1 = ON \text{ and } T_2 = OFF \\ 0 & \text{.................. if } T_1 = OFF \text{ and } T_2 = ON \end{cases} \qquad (1)$$

Therefore, the sub-module can make a step change to the converter output voltage waveform when the sub-module's terminal voltage is switched between V_C and zero. Since there are a number of sub-modules (typically more than a hundred) in a phase unit, the firing of all switches should be properly controlled to generate a multi-level ac voltage waveform as shown Fig. 1(b) and this voltage synthesis mechanism is described below.

When the sub-module voltage is V_C, it is said to be in the 'ON' state, and when it is zero, it is considered to be 'OFF'. If the multi-valve has 'N' number of sub-modules, then converter can generate a phase voltage with ($N+1$) levels. Considering the instantaneous level number of the converter phase voltage is '$n(t)$' (where, $0 \leq n(t) \leq N$) and the number of sub-modules; N_U and N_L where, $0 \leq N_U, N_L \leq N$ required to be 'ON' in the upper and lower multi-valves respectively;

$$v_{an}(t) = \left[n(t) - 1 \right] * V_C$$
$$= \frac{V_d}{2} - N_U * V_C \qquad \text{(from the upper multi-valve)} \qquad (2)$$
$$= -\frac{V_d}{2} + N_L * V_C \qquad \text{(from the lower multi-valve)}$$
$$\text{where } N_U = N - N_L$$

With this method, the full dc bus voltage can be seen across the total number $\left(N = N_U + N_L \right)$ of 'ON' sub-modules. Thus, since all capacitor voltages are required to be the same, each must be equal to:

$$V_C = \frac{V_d}{N} \qquad (3)$$

B. Capacitor Voltage Balancing

The objective of this capacitor voltage balancing controller is to generate firing pulses for each sub-module to maintain the sub-module's capacitor voltage at a constant value as given in (3). Two capacitor voltage balancing algorithms proposed for the MMC operation based on; (a) ranking of capacitor voltage values [11] and (b) pulse-width modulation (PWM) [12] are discussed below.

(i) Capacitor Voltages Ranking Based Approach

The block diagram of this capacitor voltage balancing control algorithm is shown in Fig. 2.

As discussed in section II-B, the total number of 'ON' state sub-modules is being varied from 0 to N during the generation of one cycle of the converter output voltage waveform. Therefore for a specified number of 'ON' state sub-modules in a multi-valve, there are different switching combinations which are referred to as 'redundant switch states'. In a modular multi-level inverter, the redundant switch states are groups of switch states that produce the same phase voltage, providing all the capacitor voltages are equal in magnitude. As shown in Fig. (2), when the 'quantizer' demands the required number of 'ON' state sub-modules to the 'sub-module selector', the duty of this unit is to select the most suitable candidate sub-modules from the multi-valve. This property being used by the 'sub-module selector' for capacitor voltage balancing approach is discussed in below.
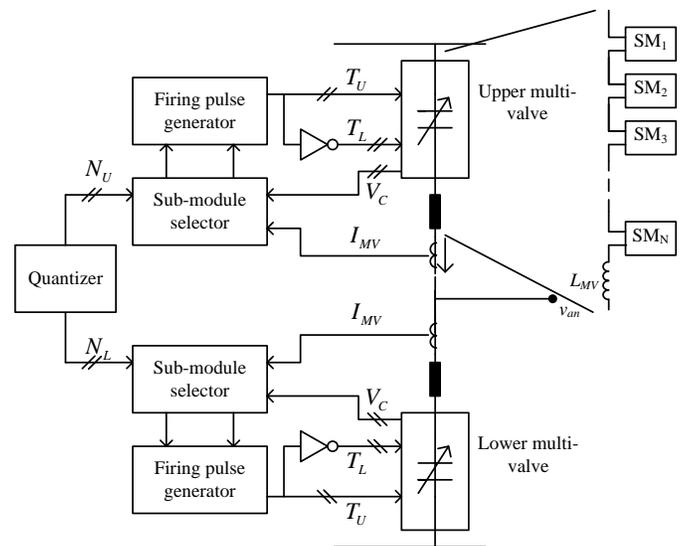
Fig. 2. Block diagram of a MMC capacitor voltage balancing and firing generation units.

The 'Sub-module selector' creates a table in which the capacitors are ranked in order of increasing dc voltages. The table is consulted when the quantization algorithm demands a step change (i.e. change in N_U and N_L). As in Fig. 1(a), when T1 is 'ON' and T2 is 'OFF', the capacitor voltage (V_C) is increasing or decreasing depending on the direction of current across the capacitor (I_C). If I_C is positive, then the capacitor voltage, V_C is increasing and V_C is decreasing when I_C is negative. However, instead of measuring the direction of individual capacitor currents, the multi-valve current can be used.

Consider the upper multi-valve which requires N_U sub-modules to be 'ON'. If the current I_{MV} is positive (Fig. 2), then turning on a sub-module will result in capacitor voltage increase. In that case, the N_U sub-modules ranked lowest in voltage are turned ON, so that they can be re-charged. If I_{MV} is negative, then the highest-voltage sub-modules are turned ON, so that their voltages may discharge. The same is done for the lower multi-valve.

The capacitor voltages of sub-modules can be controlled in a narrow band by applying this methodology for all three phases [6], [13].

(ii) Multi-level Carrier-Based PWM

Multi-level carrier-based PWM uses 'N' number of triangular carrier signals, which can be modified in phase in order to reduce the output voltage harmonic content. The lth carrier is phase shifted by an angle equal to $2(l-1)\pi / N$ in this modulation. By comparing a sinusoidal reference waveform with the 'N' carrier waveforms, the firing signals are generated for the 'N' sub-modules in the multi valve. Each transition in the multi-level output from one level to next level can be determined corresponding to the respective phase shift in modulating signal and carrier.

Fig. 3(a) shows the modulation signal and two phase shifted carrier signals for a 12 sub-modules per multi-valve case. The modulation frequency index is equal to 2 in this example. For the carrier waveforms in Fig. 3(a), the resultant sub-module output voltage waveforms of an upper multi-valve are shown in Fig. 3(b and c). This modulation technique
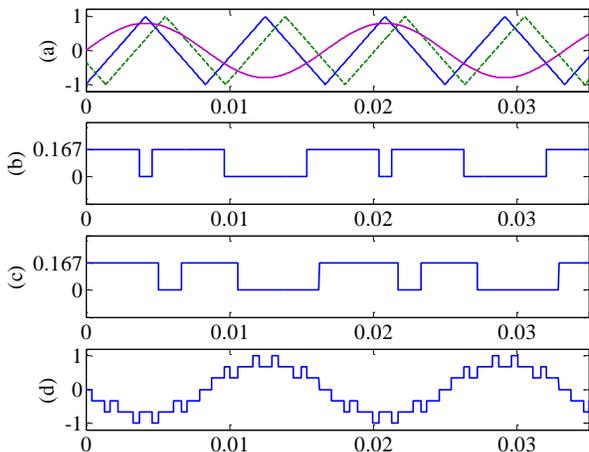
Fig. 3. Phase shifted carrier based PWM waveforms (a) Sinusoidal reference and carrier, (b and c) Resultant sub-module output voltages, and (d) MMC output voltage.

produces an even distribution of power among sub-modules, and this property can be used to equalize the sub-module capacitor voltages. In Fig. 3(d), the converter output waveform generated by phase shifted modulation is presented.

As discussed above, the number of IGBT switching operations required in a power cycle is mainly determined by the 'capacitor voltage balancing algorithm as it demands the required number of 'ON' and 'OFF' state sub-modules at a given moment. Hence, the switching loss, which is a major contributor to the converter power loss, heavily depends on the capacitor voltage balancing algorithm and the effect of voltage balancing algorithm on the converter losses will be discussed in a following chapter.

III. CONVERTER LOSS EVALUATION

The converter loss is contributed by the losses of switching devices in three forms:
  (i) Conduction
  (ii) Off-state
  (iii) Switching losses.

The conduction losses are computed in a straightforward manner by multiplying the on-state voltage by the on-state current. Similarly, off state losses are calculated using the leakage current and device blocking voltage during the off-state. However, the calculation of switching losses is a challenge, as the switching event occurs over a very short time period (about 100-200 ns). Therefore, it is difficult to accurately capture switching transients; particularly with the several micro-second time-step used in typical electro-magnetic transients (EMT) simulations of power electronic systems. A recently introduced approach estimates the switching period waveforms from the pre- and post- switching voltages and currents and semiconductor datasheet information without explicit simulation. The losses can then be calculated by analytical integration of the estimated waveforms, and have been shown to be relatively accurate [7].

A. Loss Evaluation Model

The loss evaluation approach used in this paper is schematically presented in Fig. 4 [7]. The model has been implemented in PSCAD/EMTDC simulations program. The switch model available in the host program has been modified to capture more parametric data which are input to the device loss estimation model. The losses in the device are estimated by observation of the pre- and post-switching currents and voltages using the algorithm described in [10]. The equations
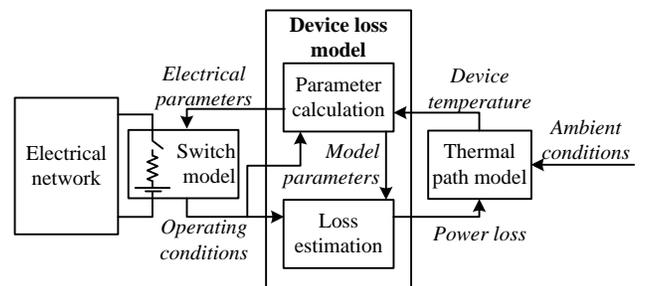
Fig. 4. Block diagram of the device loss estimation model.

used in [10] "fill-in" the intermediate sub-microsecond values of voltage and current during the larger simulation time-step of several microseconds. The parameters of these equations are derivable from the pre- and post–switching voltages, currents, and other physical data. Thus, the EMT type simulation can be conducted with a larger time-step, with the developed formula providing an estimate of the loss at each switching.

These losses, estimated by 'Device loss model' are the inputs to a dynamic model of the heat-management system (thermal path) which computes the temperature changes in various parts of the system. From a thermal point of view, the IGBT can be represented by a lumped parameter equivalent circuit as in Fig. 5 [7]. While the power loss of the device is P_{Lj}, the junction and case temperatures are T_j and T_c respectively. R_{thi} and C_{thi} represent the thermal resistance and capacitance of various layers of the semiconductor device. The number of stages usually depends on the number of materially different layers in the thermal path. The approach to extract of these thermal parameters is discussed in [7] in details. In this study, the heat sink model is not considered however, a constant (ambient) temperature is input as the case temperature assuming the heat sink maintains that constant temperature value. Because the device losses are functions of temperature, the computed device temperature is then used to change the parameters of the switch loss model for the next time-step.
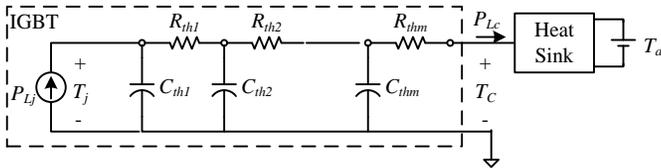
Fig. 5. Equivalent thermal network of a semiconductor device.

B. MMC Loss Evaluation

The switching loss model developed in [7], [10] is applicable to IGBT devices subject to "hard switching" which are widely used in today's HVDC and FACTS (Flexible AC Transmission Systems) devices. Therefore, this model can be directly applied to estimate the power losses of MMC converters. As the turn-on of the IGBTs (and hence, the turn-on switching loss) is significantly affected by the reverse recovery behavior of the freewheeling diode and the parasitic inductances [7], the parasitic inductance values have a significant influence on the switching losses. In this paper, the same stray inductance for all switches has been used as this value depends on the physical layout of the device/buses which are symmetric in general.
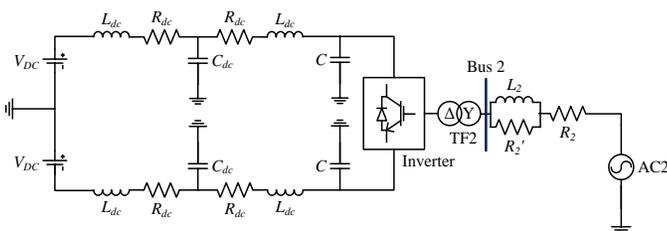
Fig. 6. Inverter model of a HVDC system.

IV. SIMULATION RESULTS

To evaluate the converter losses using the above approach, the inverter operation of a point to point HVDC system was simulated using the PSCAD/EMTDC program. The rectifier operation was modeled as a constant dc source and a detailed model for the inverter was used as shown in Fig. 6. The dc system's ratings were 25MW and ±14kV. The inverter controller is responsible for regulating the power (25MW) and ac voltage (15kV) at Bus 2. Two separate simulation cases were developed for the MMC and conventional two-level VSC converters for the comparison of resulting converter losses.

A. MMC – HVDC System

In this study, 24 sub-modules were used in each phase of the converter, thus it gives a total of 144 IGBT/diode semiconductor switches. Each phase of the converter was modeled as shown in Fig. 1(a). As given in (3) the rated sub-module voltage is equal to 2.33kV and hence, ST1500GXH24 from Toshiba, rated at 4.5kV, 1.5kA was chosen as the IGBT/Diode switch [14]. The overvoltage limit for this switching device is more than 93%.

The internal controls of the converters were used for capacitor voltage balancing and generation of firing signals as discussed in section II-B. Two separate simulations were carried out for each capacitor voltage balancing algorithms.

(i) Capacitor Voltages Ranking based Approach

Fig. 7 shows the resulting power loss and voltage waveforms when the capacitor voltage ranking based method described in dub-section II-B(i) is used as the voltage balancing technique. As shown in Fig. 7(a), the converter power loss estimated using the method discussed in section III is equal to 0.23MWper converter or 0.46 MW considering both the rectifier and inverter. This is 1.84% of the total transmitted power. Fig. 7(b) shows the measured power and rms voltage at bus 2 which are equal to the reference values. The converter output voltage and top most sub-module capacitance voltage (phase A) are shown in Fig. 7(c) and (d)
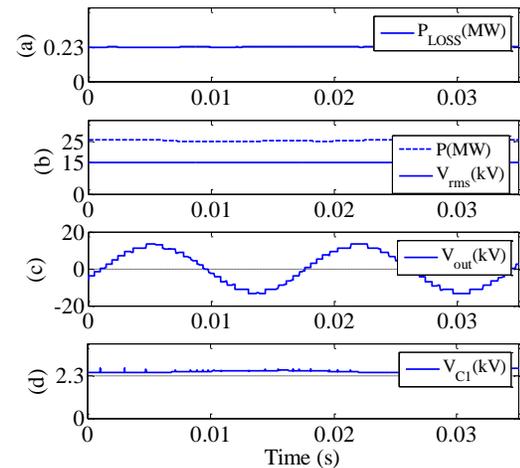
Fig. 7. MMC waveforms using capacitor voltages ranking based approach: (a) Inverter side power loss, (b) Power and rms voltage at inverter side Bus 2, (c) Inverter output voltage, and (d) top-most sub-module capacitor voltage of phase 'A'.

respectively. Calculation also shows the total harmonic distortion (THD) of the ac voltage waveform to be 6.06%.

(ii) Multi-level Carrier-Based PWM

The MMC's power loss was also estimated the multi-level carrier based PWM technique as discussed in sub-section II-B(*ii*). The resulting power loss and voltage waveforms are shown in Fig. 8. As shown in Fig. 8(a) and (b), when the converter transmits 25MW, the resulting power loss for a single converter is 0.22MW per converter, giving a total MMC system loss of 1.76% of the rated power. The converter output voltage and top most sub-module capacitance voltage (phase A) are also shown in Fig. 8(c) and (d) respectively. Analyzing the ac voltage waveform yields a THD figure of 5.42%. In this test carrier frequency was chosen as 360Hz to assure the fluctuation of sub-module capacitor voltages is well within the range of $\pm 7.5\%$.
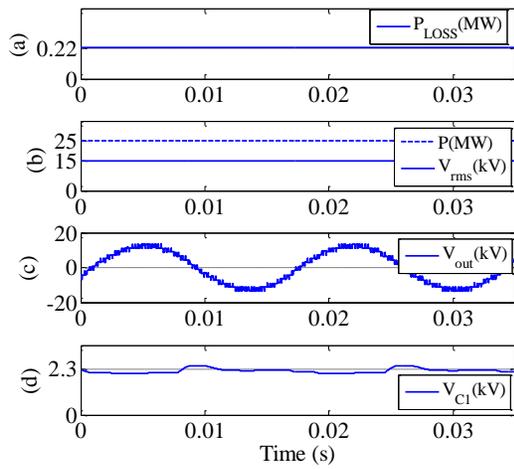
Fig. 8. MMC waveforms using multi-level carrier based approach: (a) Inverter side power loss (b) Power and rms voltage at inverter side Bus 2, (c) Inverter output voltage and (d) top-most sub-module capacitor voltage of phase 'A'.

B. Two-level VSC – HVDC System

In this section, a similar loss estimation was carried out for a 2-level VSC based HVDC converter, shown in Fig. 9. T_i's represented a group of series connected IGBT/diode switches. To be comparable with the MMC based inverters, eight ST1500GXH24 switches (S_i) made the valve group (T_i) as shown in Fig. 9. Thus dc voltage blocking capability for each
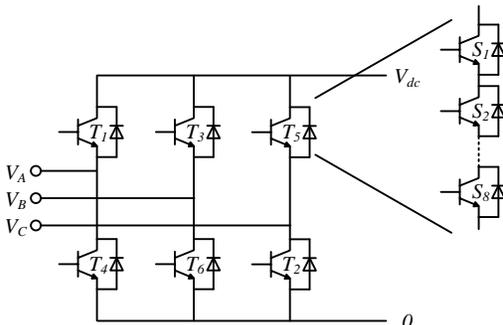
Fig. 9. Two-level voltage sourced converter and valve group.
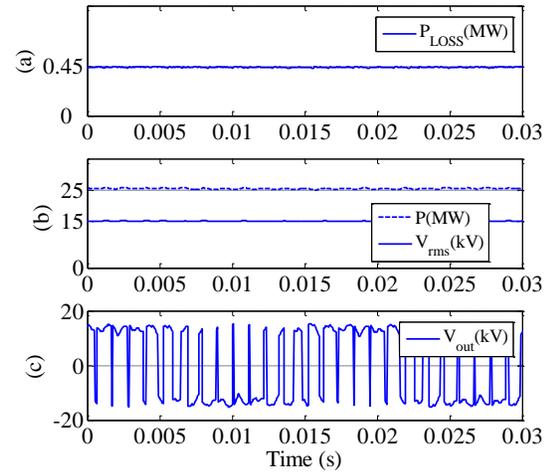
Fig. 10. Two-level VSC waveforms (a) Inverter side power loss, (b) Power and rms voltage at inverter side Bus 2, and (c) Inverter output voltage.

valve group is 36kV which is well above the margin of 28kV, giving 28% of overvoltage margin.

The output voltage waveforms were synthesized using the sinusoidal pulse width modulation (SPWM) with the carrier frequency of 900 Hz. The converter losses were estimated using the same approach discussed above and the resulting waveforms are shown in Fig. 10. As seen in Fig. 10(a), the converter loss is equal to 0.45MW per converter when 25MW (Fig. 10(b)) is transmitted giving 3.60% total power loss for the 2-level VSC HVDC scheme. Fig. 10(c) shows the unfiltered converter output voltage (phase), which has a THD value of 111%.

C. Results Summary

Table 1 summarizes the converter power losses and total harmonic distortion for different approaches discussed above. Two different MMC cases, one with 24 sub-modules, the other with 48 sub-modules are considered. The losses of the MMC for the two control methods (capacitor voltage ranking and phase shifted PWM are essentially the same, and decrease when a larger number of sub-modules is used. The loss for the

Table 1. Converter power losses comparison.

Converter Type	No. of Sub-modules /phase	Power Loss/ Converter (MW)	Total Power (MW)	HVDC system power loss (%)	THD (%)
MMC (Capacitor ranking)	24	0.23	25	1.84	6.06
	48	0.20	25	1.60	5.00
MMC (PWM)	24	0.22	25	1.76	5.42
	48	0.20	25	1.60	3.84
2-VSC (SPWM)	N/A	0.45	25	3.60	111

2-level VSC is significantly higher- over twice that of the MMC. The THD figures for the MMC are also significantly lower than that for the 2-level VSC, and decrease even more when the number of sub-modules is increased. For the MMC, the phase shifted PWM method appears to have slightly less THD than the capacitor voltage ranking method.

V. CONCLUSIONS

The converter power losses for MMC based HVDC systems were evaluated using an approach that 'fills-in' the waveform shape in between simulation time-steps. The simulation results show that when MMC converters are used, the operating loss of the rectifier and inverter combined is less than 2% of the rated HVDC power. The impact of control methods for the MMC on the losses was also investigated by considering two capacitor voltage balancing algorithms that have been proposed for the MMC converters based on; (a) ranking of capacitor voltage values and (b) pulse-width modulation (PWM). The converter efficiency is in the same range for both the algorithms but the PWM based method has the advantage of a slightly lower harmonic distortion.

In comparison, the two-level VSC based HVDC system losses are almost double that of a MMC based system, indicating that the MMC based dc systems are significantly more efficient.

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