An FPGA-Based Hardware-in-the-Loop Simulator for Multilevel Converter Systems

Mahmoud Matar, Maryam Saeedifard, Amir Etemadi, and Reza Iravani

***Abstract*—This paper presents an FPGA-based real-time simulator, for multilevel converter systems, that is primarily intended for hardware-in-the-loop (HIL) testing applications. The proposed simulator utilizes a customized hardware architecture, as the computational engine, that maps the solution algorithm of the power electronic system under consideration. The designed computational engine enables the use of a simulation time-step in the range of tens to few hundred nanoseconds. Thus eliminating the need for corrective algorithms, to account for the errors arising from the inter-simulation time-step switching phenomenon associated with HIL testing, without compromising the accuracy or the numerical stability.**

The simulator is tested and its HIL capability verified based on the closed-loop testing of the controller platform for a three-level neutral-point clamped (NPC) converter.

***Index Terms*—Real-time Simulation, Electromagnetic Transients, Multilevel Converters, Power Electronics Interface, Modeling, FPGA.**

I. Introduction

MULTILEVEL converters have attracted significant interest for medium- and high- power applications. As compared with the conventional two-level converters, they (i) provide higher power quality at the AC-side, (ii) can operate at higher AC voltage levels and minimize or even eliminate the interface transformer, and (iii) reduce switching losses [1]. Among the multilevel converter configurations, the three-level neutral-point clamped (NPC) converter has been widely accepted for applications in medium/high power drives and the utility systems [1]. In spite of its merits, an NPC converter is prone to voltage drifts of its DC-side capacitors. The voltage-drift phenomenon deteriorates the AC-side voltage waveforms and, consequently, results in unsatisfactory operation and even failure of the NPC converter. The converter controller bears the burden of ensuring the balance of the DC-side capacitors voltages and the satisfactory operation of the converter. As such, the converter controller has to be thoroughly tested and its functionalities verified prior to installation and commissioning.

To thoroughly test the converter control platform in realistic conditions, a hardware-in-the-loop (HIL) arrangement of the physical controller platform in association with a real-time simulator has to be used [2]–[5]. In the HIL arrangement, the real-time simulator is interfaced to the control/protection platform to be tested and both are operated simultaneously in a closed-loop manner, Figure 1. The real-time simulator solves the mathematical model of the system under consideration to reproduce the actual time-domain voltage and current waveforms and sends them to the control/protection Platform. On the other hand, the control/protection platform sends the associated signals, e.g., gating signals, to the simulator. For proper closed-loop operation, the simulator must be able to accept inputs from the control/protection platform under test, incorporate these inputs into the ongoing simulation, and solve the system model fast enough such that the outputs are available before the next simulation step commences.

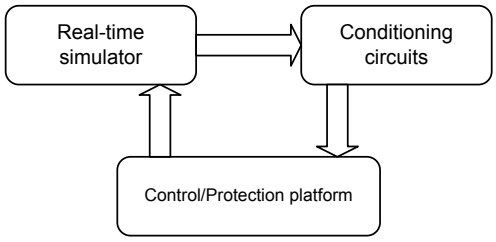

Fig. 1. HIL arrangement for closed-loop testing of controller platforms

Real-time simulation of power electronic converter systems, in the context of HIL testing, is a challenging task. This is due to:

1) the computational burden imposed on the simulator hardware due to the inherent switching nature of power electronic converters, and
2) the asynchronous digital interface between the controller PWM outputs and the simulator inputs. PWM gating signals generated by the controller rarely coincides with the real-time simulation time-grid. Switching events are usually imposed by the controller in-between two simulation instances. The simulator, unlike an actual system, cannot instantaneously respond to the PWM outputs of the controller and only accounts for it at the end of the simulation time-step, thus, errors are introduced to the simulation results. The percentage error due to ITS is a function of the simulation time-step of the simulator and the switching frequency of the controller. This problem is more pronounced in multilevel converter systems, particularly when the voltage balancing task of the converter is carried out through the modification of the switching functions, with no requirement to additional

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power circuitry. With the increase in the switching events per simulation time-step, it will be very likely to have multiple switching events imposed by the controller in-between two simulation instances. This phenomenon is called multiple inter-simulation time-step switching (MITS).

This paper presents an FPGA-based real-time simulator for multilevel converter systems that is primarily intended for HIL testing applications. The developed simulator addresses the aforementioned challenges based on implementing a customized hardware architecture, on the FPGA, that maps the solution algorithm of the power electronic system under consideration. The designed customized hardware architecture enables the use of a simulation time-step in the range of tens to few hundred nanoseconds. Thus eliminating the need for corrective algorithms, to account for the errors arising from MITS events, without compromising the accuracy or the numerical stability [6]–[8].

The developed FPGA-based simulator enables not only accurate real-time simulation of high power converters but also real-time simulation of high-frequency power electronic converters for aerospace and automotive applications. Moreover, the cost of the developed FPGA-based real-time simulator is a fraction of the cost of existing multiprocessor based simulator while delivering at least one fold performance improvement.

The rest of this paper is organized as follows. Section II presents the architecture of the FPGA-based real-time simulator. Section III introduces the proposed techniques to interface the external control/protection platform with the simulator and the different options for monitoring of the waveforms generated inside the simulator. Section IV and V, through a case study, provide validation and evaluation of the performance of the developed simulator. Conclusions are stated in section VI.

II. FPGA-based Real-Time Simulator Architecture

Figure 2 shows a schematic diagram of the FPGA-based real-time simulator. The core of the simulator is the computational engine. The design philosophy of the computational engine, to enable the use of nanosecond range simulation time-step, is to:

- exploit all possible levels of parallelism inherent to the solution algorithm of the system model, and
- design a customized hardware architecture that closely maps both the solution algorithm and dataflow.

The solution algorithm adopted in this work is based on representing each circuit component by its companion circuit model in the form of a current source, that represents the history of the circuit as it depends on the currets and/or voltages from the previous time-steps, in parallel with a conductance G. As such, the original system is transformed into a system of resistive elements and current sources [9], [10].

To alleviate the computational burden imposed by the need to invert/refactorize the admittance matrix due to switchings, this work adopts the associated discrete circuit (ADC) approach for modeling of the multilevel converter systems. The

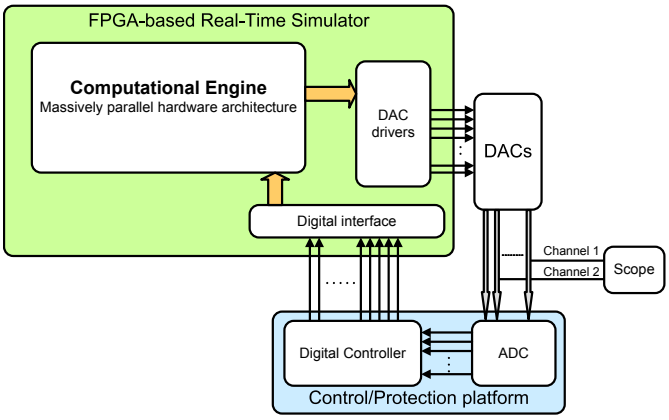

Fig. 2. Schematic of the FPGA-based real-time simulator in HIL testing arrangement

ADC modeling approach offers the advantage of maintaining the entries of admittance matrix fixed irrespective of the switching states. The ADC approach represents a power electronic switch with a current source in parallel with a conductance G_S [11]–[15]. In this approach, the conductance G_S is fixed irrespective of the switch ON/OFF state. The switch ON/OFF state is only accounted for by the value of the shunt current source. Thus, the ADC approach maintains the admittance matrix constant irrespective of the ON/OFF state of each switch [11], [12].

Another salient advantage of the ADC model is that it allows the inclusion of snubber circuits with little additional computational cost [12], i.e., it is more accurate and at the same time computationally efficient model. Figure 3a shows an ideal switch with a parallel RC snubber, Figure 3b shows the equivalent ADC model of all components, and Figure 3c shows the reduced-order model of the combined switch and snubber circuit model.

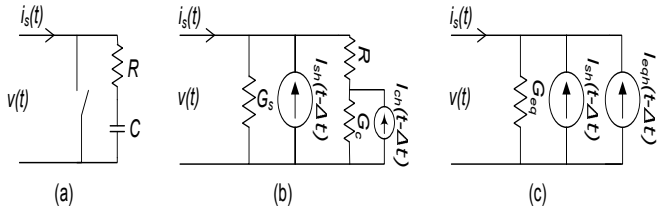

Fig. 3. (a) Switch with a snubber circuit (b) equivalent ADC model (c) Combined switch model

The flowchart of Figure 4 demonstrates the main solution steps. Figure 4 indicates that two sets of equations have to be solved consecutively. First, nodal analysis is used to solve for the node voltages at each time-step based on the values of the history current sources from the previous time-step. Second, the values of the history current sources are updated based on the calculated node voltages. The time is then advanced and the process is repeated. Thus, parallel execution of the two sets is not feasible. However, parallelism among each set of equations is possible.

The computational engine is designed to map the solution algorithm illustrated in Figure 4. The computational engine

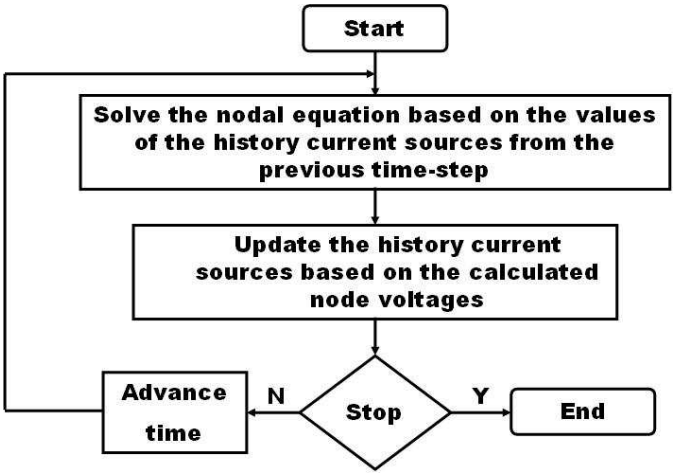

Fig. 4. Flowchart of the simulation process based on the adopted solution algorithm)

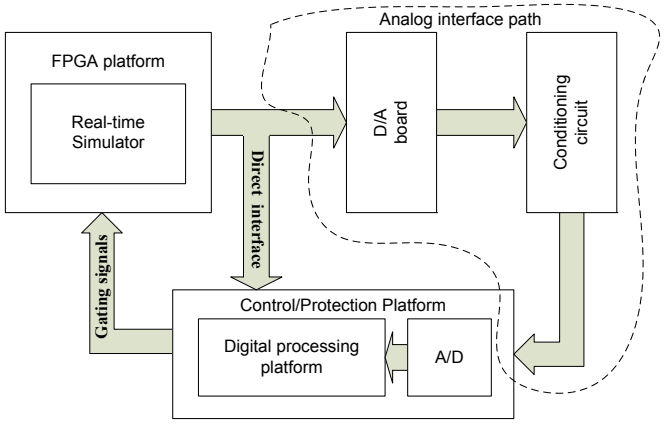

Fig. 5. Simulator/controller interface options

has two main units that are operated sequentially:

- the first unit is responsible for calculating the node voltages, and
- the second unit is responsible for updating the history current sources associated with switching and non-switching elements.

The first computational unit has a massively parallel hardware architecture, with n^2 parallel multipliers and n parallel adder trees, for the simultaneous solution of the node voltages, where n is the dimension of the admittance matrix. The second computational unit has a massively parallel hardware architecture, with 2m parallel multipliers and m parallel adders, to update the history current sources in parallel, where m is the number of history current sources. Details of the computational engine are available in [6], [16], [17].

III. Interfacing with External Control Platforms

HIL testing involves data exchange between the real-time simulator and the controller platform. The inputs to the controller platform are usually analog in nature since in real-life operation these inputs are voltage and current measurements from the actual power system. On the other hand the outputs from the controller platform - the PWM gating signals - are inherently digital in nature. Thus, the gating signals are transferred directly from the Controller platform to the simulator in digital format. The number of digital inputs to the simulator is equal to the number of control signals which is dictated by the number of switching devices present in the power system being simulated.

The FPGA-based real-time simulator provides two options for transferring the real-time simulator outputs to the external Controller Platform; either via (i) an analog interface, which utilizes digital-to-analog converters (DAC) to generate analog signals corresponding to the simulated voltages and currents, or (ii) a direct digital interface, Figure 5.

In this work, DAC boards based on the Linear Technologies 16-bits parallel input LTC1668 DAC are developed to be used with the FPGA-based real-time simulator. The main advantage of this DAC unit is its very small settling time of approximately 20 ns, i.e., the overhead time due to the digital to analog conversion process is limited.

The direct digital interface enable the direct transmission of the digital signals, corresponding to the simulated voltages and currents, to the Control/Protection Platform. This scheme is useful in verifying the implementation of the control/protection algorithm on the Control/Protection digital signal processing platform during the development stage.

Regardless of the output format from the simulator, i.e., digital or analog, the outputs have to be synchronized with the simulator time grid. In this work, the simulator outputs are updated based on the rising edge of the simulator clock.

IV. Case Study

The main objective of this case study is to demonstrate the capability of the FPGA-based real-time simulator to operate in hardware-in-the-loop configuration. The real-time simulator is interfaced with an external controller and the complete setup, i.e., the simulator and the controller, is operated in closed loop. The simulator represents the power electronic system and sends the voltage and current signals to the controller, and the controller sends the appropriate gating pulses to the simulator.

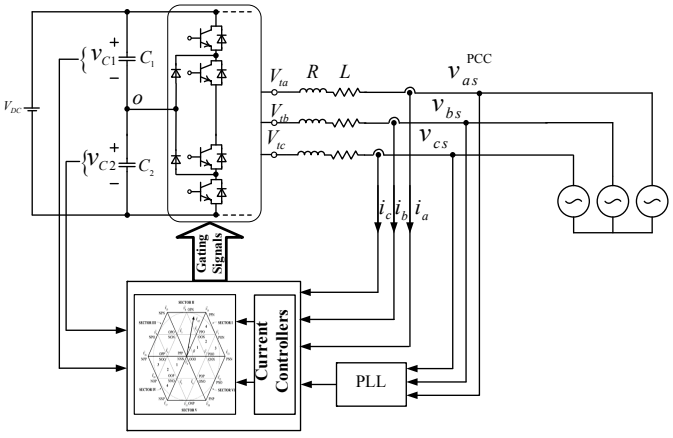

Fig. 6. Schematic diagram of the NPC converter system and its controller

The NPC converter of Figure 6 controls the real and reactive power exchange with the grid at the Point of Common Coupling (PCC). The system parameters are given in Table I. The NPC converter also maintains the DC-capacitor voltages at their desired reference values, i.e., VDC/2. To control real and reactive power components of the NPC converter, angle and magnitude of voltage at the AC-side terminals should be controlled. A Space Vector Modulation (SVM) strategy is utilized to (i) control the AC-side terminal voltages of the NPC converter and (ii) balance the DC-side capacitor voltages at their reference values [18].

TABLE I
CASE I: SYSTEM PARAMETERS

AC system line voltage	580 V
Frequency	50 Hz
Resistance R	0.035 Ω
Inductance L	3 mH
Net DC voltage	1500 V
Resistance r	0.0156 Ω
Capacitors C1 and C2	10000 μF

A. System Model for Controller Design

The mathematical equation that describes the system of Figure 6 is

$$V_{tabc} = V_{sabc} + Ri_{abc} + L\frac{di_{abc}}{dt} \tag{1}$$

The dq mathematical equations, i.e., (2) and (3), are obtain by transforming (1) from the abc frame to a synchronously rotating dq frame [19].

$$L\frac{di_d}{dt} = -Ri_d + L\omega i_q + v_{td} - v_{sd} \tag{2}$$

$$L\frac{di_q}{dt} = -Ri_q - L\omega i_d + v_{tq} - v_{sq} \tag{3}$$

Inspection of (2) and (3) reveals that i_d and i_q cross-couples the two equations. To simplify the process of controller design, this coupling has to be removed. Decoupling can be achieved by a change of variables such that

$$u_d = \omega L i_q + v_{td} - v_{sd}, \tag{4}$$

$$u_q = -\omega L i_d + v_{tq} - v_{sq}. \tag{5}$$

By introducing new variables u_d and u_q, (2) and (3) are decoupled and the two independent first order equations (6) and (7), with inputs u_d and u_q, are obtained [18], [20].

$$L\frac{di_d}{dt} = -Ri_d + u_d, \tag{6}$$

$$L\frac{di_q}{dt} = -Ri_q + u_q, \tag{7}$$

B. AC-side Current Controllers

Based on the decoupled equations, i.e., (6) and (7), an identical pair of PI controllers are designed. One controller is responsible for controlling i_d and the other one is responsible for controlling i_q. The currents control block diagram is shown in Figure 7.

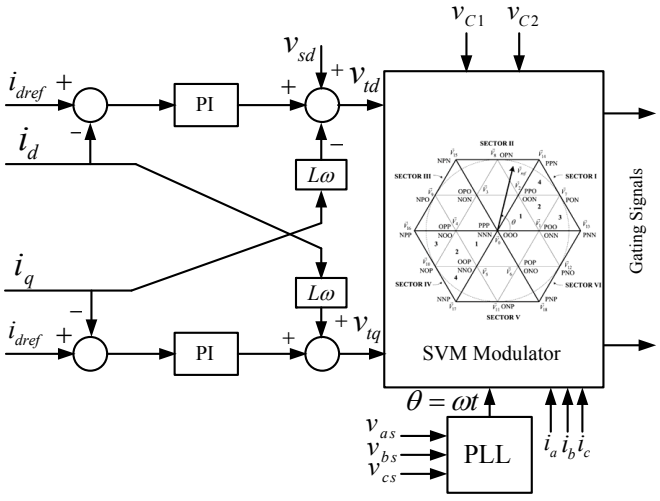

Fig. 7. Currents control block diagram

C. PWM and Capacitors Voltages Balancing

The NPC converter is prone to voltage drifts of the DC-side capacitors, resulting in distorted AC-side voltages or even converter failure [18]. One efficient way to mitigate the voltage drift is to modify the switching pattern such that the capacitor voltages are maintained balanced. This is possible if the PWM strategy adopted is based on space-vector modulation (SVM) where the redundancy in switching states associated with the SVM is exploited to enforce the average current values in the intermediate branches to zero. Thus, the capacitors voltages are maintained balanced [18]. The SVM with the built-in capacitors voltages balancing scheme is adopted in this work [18].

D. Hardware-in-the-Loop Setup

Figure 8 shows a photo of the FPGA-based real-time simulator in the HIL configuration. The real-time simulator is realized based on Altera's DE3-150 Development and Education board [21], where the mathematical model of the converter system of Figure 6 is implemented inside the simulator Stratix III FPGA. The simulator operates in real-time with a fixed simulation time-step of 500 ns and the inputs to the simulator are 2.5 kHz PWM signals, i.e., the simulation time-step is approximately 800 times less than the switching period. Thus, there is no need for any corrective measures to account for the ITS or MITS.

The controller and the SVM strategy are implemented on the National Instrument CRIO platform comprised of an 800 MHz real-time PowerPC processor and a Virtex-5 LX110 FPGA [22]. The sampling frequency of the controller is 2.5 kHz.

For the HIL operation, the FPGA-based real-time simulator sends to the controller, through the D/A interface, (i) four voltage signals, i.e., the total DC-side voltage, the lower capacitor voltage, the ac system phase a and phase b voltages, and (ii) two current signals, i.e., the AC-side phase a and phase b currents. Based on the required operating conditions and the measured voltages and currents, obtained from the simulator, the control subroutine calculates v_{td} and v_{tq} and send them

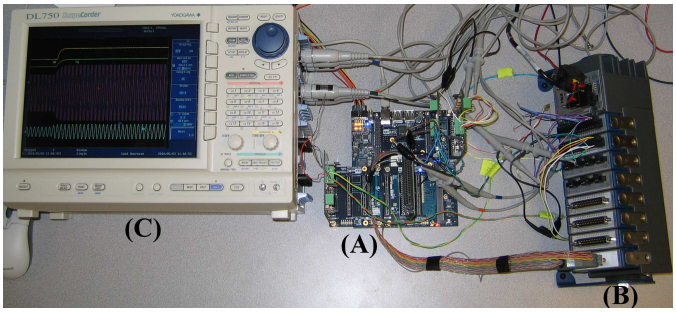

Fig. 8. Photo of the experimental setup: (A) the FPGA-based real-time simulator, (B) the CRIO controller platform, and (C) the oscilloscope

to the SVM subroutine. In turns, the SVM determines the switching pattern and the ON duration time of the switches [18], and accordingly generates and sends the gating signals to the real-time simulator.

V. Results and Discussions

This section presents the closed loop simulation results obtained from the FPGA-based real-time simulator as well as those obtained from the PSCAD/EMTDC.

Scenario I: Response to Step Change in i_d Reference Current: Initially the system of Figure 6 is operating in a steady state condition with zero AC-side currents, i.e., i_{dref} and i_{qref} both are zero, and then a step change of 300 A is imposed on i_{dref}. Figure 9 shows an oscilloscope screen capture of the FPGA-based simulation results corresponding to the d and q components of the AC-side currents, and the phase "a" and "b" currents. Figure 10 shows the d and q components of the AC-side currents, and the phase "a" and "b" currents obtained from the PSCAD/EMTDC.

Scenario II:Response to Step Change in i_q Reference Current: Initially the system of Figure 6 is operating in a steady state condition with i_{dref} set to 300 A and i_{qref} set to 200, and then a step change of -400 A is imposed on i_{qref}. Figure 11 shows an oscilloscope screen capture of the FPGA-based simulation results corresponding to the d and q components of the AC-side currents, and the phase "a" and "b" currents. Figure 12 shows the d and q components of the AC-side currents, and the phase "a" and "b" currents obtained from the PSCAD/EMTDC.

A. Discussions

The close agreement between the corresponding results of Figures 9 to 12 verifies the validity of the FPGA-based real-time simulator to operate in the HIL configuration for testing external controllers. The stability and the accuracy of the simulations for long running durations are also verified as the FPGA-based simulator along with the controller are left continuously running in HIL configuration for hours.

The slight discrepancies between the simulation results obtained from the FPGA-based real-time simulator and those from the PSCAD/EMTDC are due to:

- the delays in the controller outputs imposed by the computation time required by the controller platform to perform the arithmetic calculation of the control algorithm and of the PWM scheme. This delay time is not account for in the PSCAD/EMTDC simulation,
- the discretization errors since the PSCAD/EMTDC adopts floating point representation whereas the FPGA-based real-time simulator is based on the fixed point number representation, and
- the errors introduced due to the D/A and A/D converters.

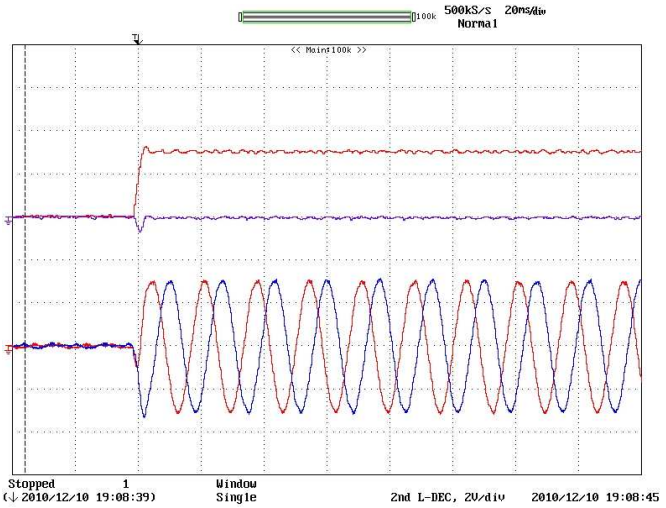

Fig. 9. Oscilloscope screen capture of the FPGA-based simulation results for Scenario I

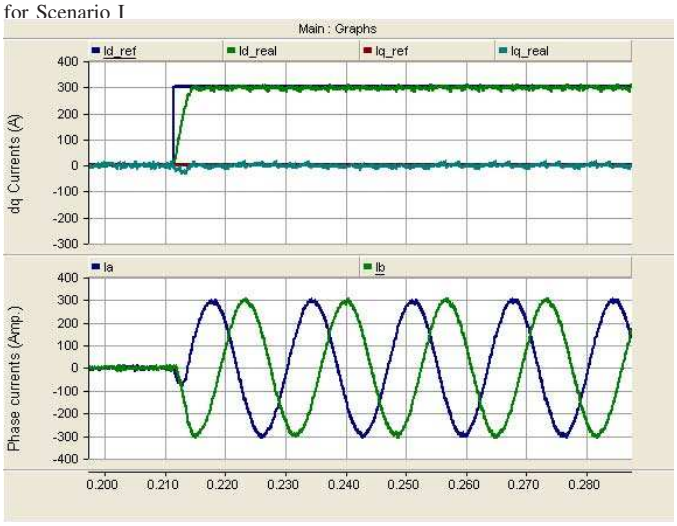

Fig. 10. The simulation results generated by the PSCAD/EMTDC for Scenario I

VI. Conclusions

This paper presents an FPGA-based real-time simulator for hardware-in-the-loop HIL testing of control/protection platforms. The core of the simulator is the massively parallel computational engine. The hardware architecture of the computational engine exploits all possible levels of parallelism inherent to the solution algorithm of the system model. The developed simulator enables the real-time simulation of multilevel converter systems with a nanosecond range simulation time-step. Thus, eliminating the need to incorporate corrective

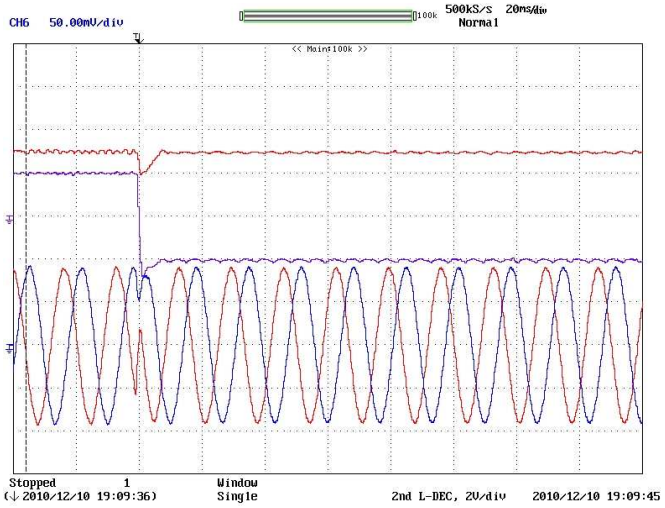

Fig. 11. Oscilloscope screen capture of the FPGA-based simulation results for Scenario II

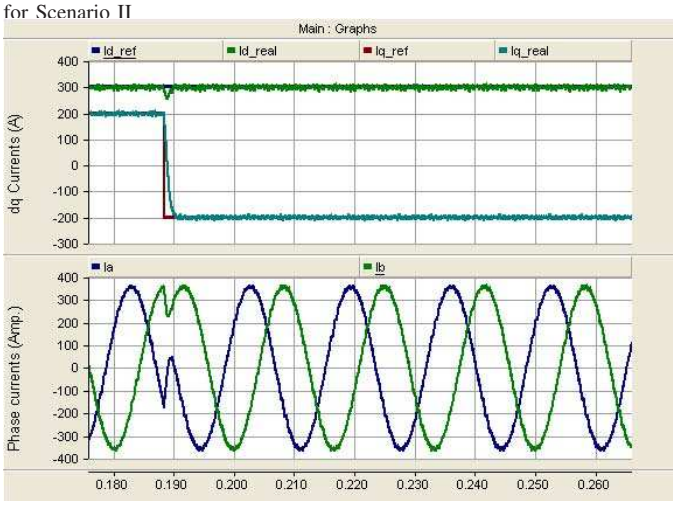

Fig. 12. The simulation results generated by the PSCAD/EMTDC for Scenario II

measures to account for the error arising from the inter-simulation time-step switching phenomenon associated with HIL.

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