Time-Domain Model of a Bidirectional Distribution Electronic Power Transformer

S. Alepuz, F. González-Molina, J. Martin-Arnedo, J. A. Martinez-Velasco

***Abstract*--Transformer size can be significantly reduced by increasing the operating frequency, which may be achieved by means of power electronics converters installed as interfaces to the power frequency systems at both transformer sides. In this work, a model for a bidirectional high-frequency solid-state transformer is presented. Several case studies have been carried out to evaluate the behavior of the transformer under different operating conditions and test its impact on power quality. The results show that the new transformer matches most functions of a conventional power transformer, and provides additional capabilities for mitigating dynamic power quality problems.**

***Keywords*: Bidirectional converter, distribution system, electronic power transformer, modeling, power electronics, power quality, pulse width modulated (PWM) power converters.**

I. Introduction

TRANSFORMERS are widely used in electric power systems to perform primary functions, such as voltage transformation and isolation. Since the size of a conventional copper-and-iron based transformer is inversely proportional to the operating frequency, an increase of this frequency would provide a higher utilization of the magnetic core and a reduction in transformer size [1].

The connection of distributed energy resources (i.e., distributed generation, energy storage devices) is raising new challenges. For instance, a high penetration of distributed generation at a low voltage (LV) distribution grid might force a power flow reversion across distribution transformers, so the LV distribution system can become a distributed generation source for the higher-level medium voltage (MV) grid [2].

Although the conventional transformer has been, and still is, the traditional link between end-users and the distribution network, a high-frequency solid-state transformer is foreseen as a fundamental component that might cope with many of the challenges of the future smart grid [3].

The list of capabilities available to this new type of transformer includes voltage sag compensation, instantaneous voltage regulation, harmonic compensation, power factor correction, auto-balancing and variable-frequency output [4] – [9]. In addition, its control must allow the possibility of having bidirectional power flow and achieve the mitigation of faults and disturbances coming from both sides.

A model for a bidirectional distribution electronic power transformer (DEPT), implemented in Matlab/Simulink, is presented in this paper. The focus is to study its behavior under variable operating conditions and disturbances, located at both sides of the solid state transformer.

II. Description of the Electronic Power Transformer

A. Description

The DEPT configuration selected for this study includes three parts: a high-voltage stage, an isolation stage, and a low-voltage stage [10]. Fig. 1 shows a detailed and feasible topology for each part of the DEPT. Although the new DEPT can manage bidirectional power flow, as a matter of explanation, the power is considered flowing from the HV to the LV power network. In such case, the input power-frequency voltage is first converted into dc voltage by the HV-side three-phase pulse width modulated (PWM) ac/dc converter, shown in Fig. 1a, working as rectifier in this case. The isolation stage includes the high-frequency transformer, and two H-bridge voltage source converters (VSC). The HV-side converter, shown in Fig. 1b, converts the HV dc voltage into a high-frequency square-wave voltage applied to the primary of the high-frequency transformer. In the secondary side, the transformed high-frequency square-wave signal is converted into a LV dc voltage by the LV-side converter. Finally, the LV-side three-phase PWM dc/ac converter works as inverter and provides the output power-frequency ac waveform from the low dc voltage, see Fig. 1c.

B. DEPT Model

- *Input Stage - High-voltage Side Front-end Converter*: The input stage is implemented by means of a three-phase PWM converter [11] - [13], without a path for the common mode or zero-sequence current.
- *Isolation Stage*: The dc voltage coming from the input stage is modulated to a high-frequency square wave, coupled to the secondary and finally converted back into a low dc voltage. A widely accepted dc/dc converter topology is the full-bridge circuit operated at constant frequency under a pulse width control strategy. This topology features minimal voltage and current stresses in

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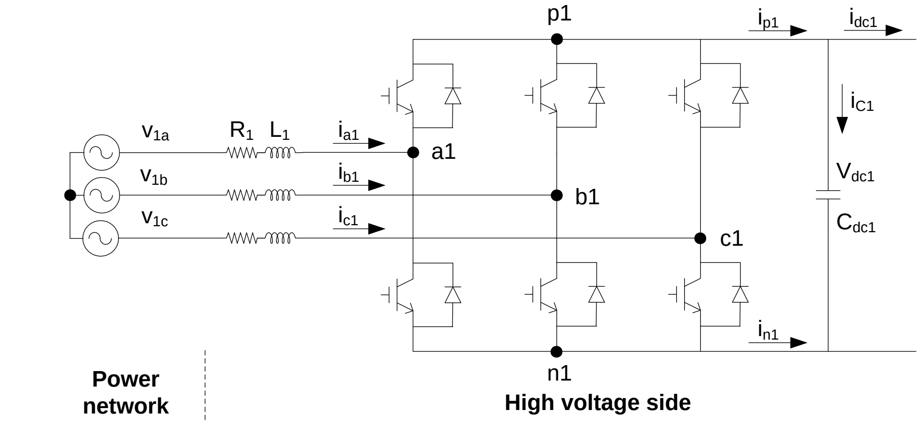
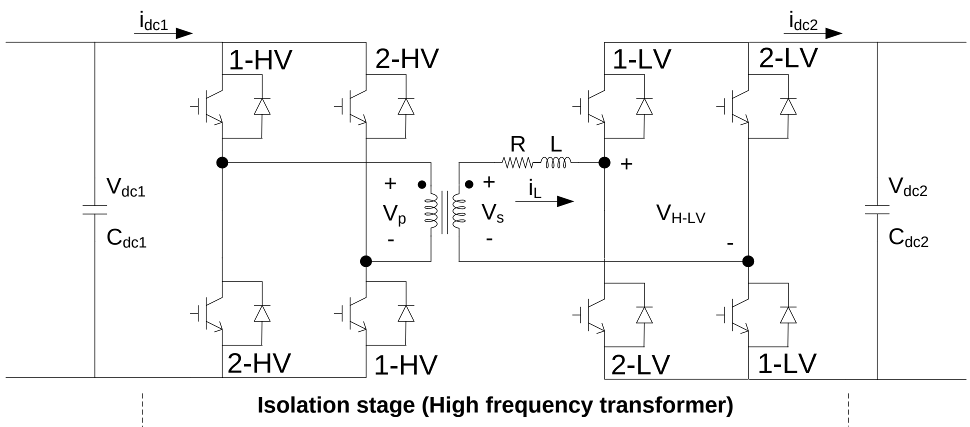
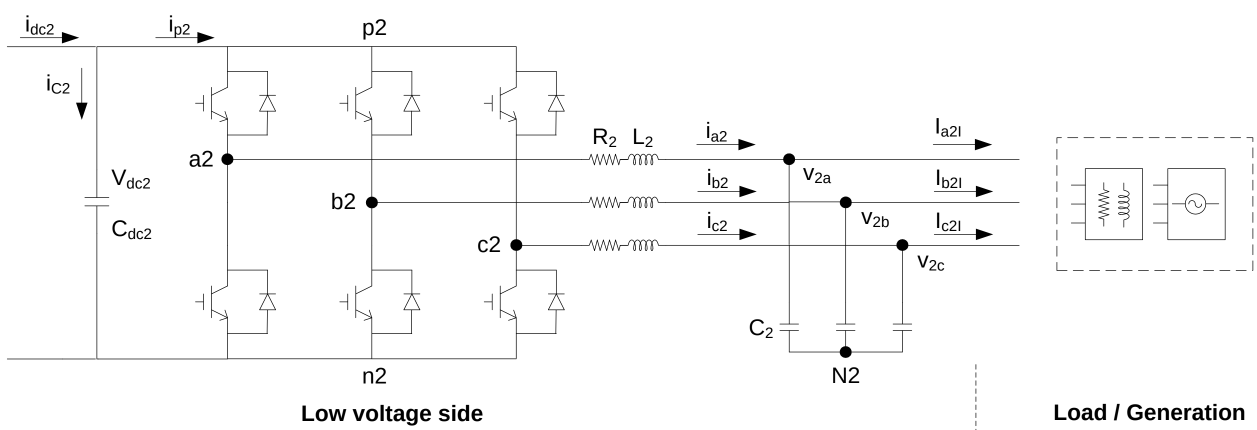


a) High-voltage side three-phase converter configuration



b) Isolation stage configuration



c) Low-voltage side three-phase converter configuration

Fig. 1. DEPT implementation.

the devices, minimum VA rating of the high frequency transformer, as well as low ripple current levels in the output filter capacitor. Soft-switching variations of the full-bridge converter make possible a reduction in device switching losses and an increase in switching frequency [14]. Primary and secondary H-bridges work with a high-frequency square-wave switching strategy. AC square-wave signals for high- and low-voltage side H-bridges are shifted with an angle φ to regulate the amount and direction of the active power flow, which is limited mainly by the transformer inductance.

- *Output Stage - Low-voltage Side Front-end Converter*: The configuration of the LV-side three-phase PWM converter is similar to that of the HV side converter. The LV side converter is connected to load and/or generation through an *LC* filter, and is responsible for controlling the voltage in the capacitor filter terminals; i.e., it controls the voltage (waveform and value) seen by the load/generation.

III. CONTROL STRATEGIES

Each DEPT stage has its respective independent controller, but given that a bidirectional power flow is assumed, there is a need to implement an overall control strategy to coordinate the three independent controllers.

A. *Input Stage - High-voltage Side Front-end Converter*

A simple but very effective strategy for PWM rectifiers under unbalanced input voltage conditions, the voltage oriented control (VOC), has been used here [15] – [17].

The control block diagram for the input stage is shown in Fig. 2. The selection of parameters is detailed in [16]. This scheme ensures constant dc bus voltage, unity power factor condition at the input terminal in an average sense, and no ripple in the input active power. Voltages and currents are expressed in the synchronous rotating *dq* reference frame.

A phase-locked loop (PLL) is employed to obtain a noise-free synchronous grid angle, needed for the *dq* transformations [18], [19]. For conventional control of this rectifier circuit, there are an outer dc-link voltage control loop and an inner grid current control loop to achieve high dynamic response and stability.

The inner grid current control loop provides fast compensation for input supply disturbances. The reference for the grid current loop is given by the output of the outer dc-link voltage control loop. All controllers have been implemented by using conventional PI regulators. Because of the coupling between the d- and q- components of the grid currents, a conventional solution of adding two decoupling feed-forward inputs to each current control loop has been considered.

A sequence separation method is applied to grid voltages. The negative sequence grid voltages are fed-forwarded and generated at the converter terminals. Therefore, no negative sequence voltage is seen by the inductive filter and only positive sequence currents flow between the grid and the converter, even in presence of asymmetrical grid disturbances.

B. *Isolation Stage*

The control block diagram for the isolation stage is shown in Fig. 3. The amount and direction of the active power flow is controlled by the phase-shift angle φ between the two ac square-wave signals [14]:

$$P_0 = \frac{V_{dc1} \cdot V_{dc2}}{m(\omega L)} \cdot \varphi \cdot \left(1 - \frac{|\varphi|}{\pi}\right) \tag{1}$$

where P_0 is the average power through the transformer, V_{dc1}, V_{dc2} are the capacitor dc voltages, m is the high-frequency transformer ratio, L is the transformer leakage inductance referred to primary side, φ is the phase-shift between central bridges, and $\omega = 2\pi f$, being f the switching frequency.

The dc–dc converter allows power flow to go towards the end-user side when voltage V_{dc1} leads voltage V_{dc2}, being φ denoted as positive. When power flows towards the MV distribution network, voltage V_{dc2} leads voltage V_{dc1}, and hence φ is denoted as negative. The absolute value of this reference phase-shift angle φ is limited to $\pi/2$ regardless of the power flow direction.

In order to control the phase-shift φ, it is necessary to obtain the output capacitor voltage V_{dc2} as a function of the power flow through the transformer. The control of this stage is divided in an outer loop used to regulate the capacitor voltage V_{dc2}, and an inner loop used to regulate the transformer inductance current I_{dc2}. The combination of these two loops avoids oscillations and speeds up control response.

C. *Output Stage - Low-voltage Side Front-end Converter*

This stage consists in a converter whose main task is to adapt the output voltage to the needs of end-user applications. Three-phase PWM control strategy has been implemented to keep the harmonic content above twice the switching frequency. A simple passive *LC* filter is used at the output of this stage to smoothen out the high frequency contents of the output voltage.

Fig. 4 shows the complete control scheme for this stage. The capacitor voltage has to be controlled by the regulator, and it is likely to have unbalanced load/generation currents, which causes negative sequence currents and voltages. Therefore, dual controllers have been considered for the positive and negative sequences. The negative sequence capacitor voltage reference is set to zero to cancel any negative sequence voltage at the filter capacitor terminals at all time, in presence of unbalanced load/generation currents. The positive sequence voltage controller regulates the filter capacitor voltages.

IV. MODEL BENCHMARKING

A. *Test System*

The test system selected for this work is that obtained when joining the three sections depicted in Fig. 1. This simple configuration will be used to evaluate the behavior of the DEPT under dynamic unbalanced conditions and any operation that could cause power flow reversion.

Table I presents the main parameters for the transformer. The rated primary and secondary voltages of the DEPT are respectively 25 kV and 400 V.

Table I - DEPT main parameters.

Parameter	**Value**
Input resistance (R_1)	0.5 Ω
Input inductance (L_1)	560.2 mH
DC link capacitance (C_{dc1})	5000 μF
DC link capacitance (C_{dc2})	2200 μF
Output filter resistance (R_2)	0.2 Ω
Output filter inductance (L_2)	1 mH
Output filter capacitance (C_2)	470 μF
Rectifier/Inverter switching frequency	10 kHz
Transformer operating frequency	1 kHz
Transformer short-circuit resistance	0.1 Ω
Transformer leakage inductance	1 mH

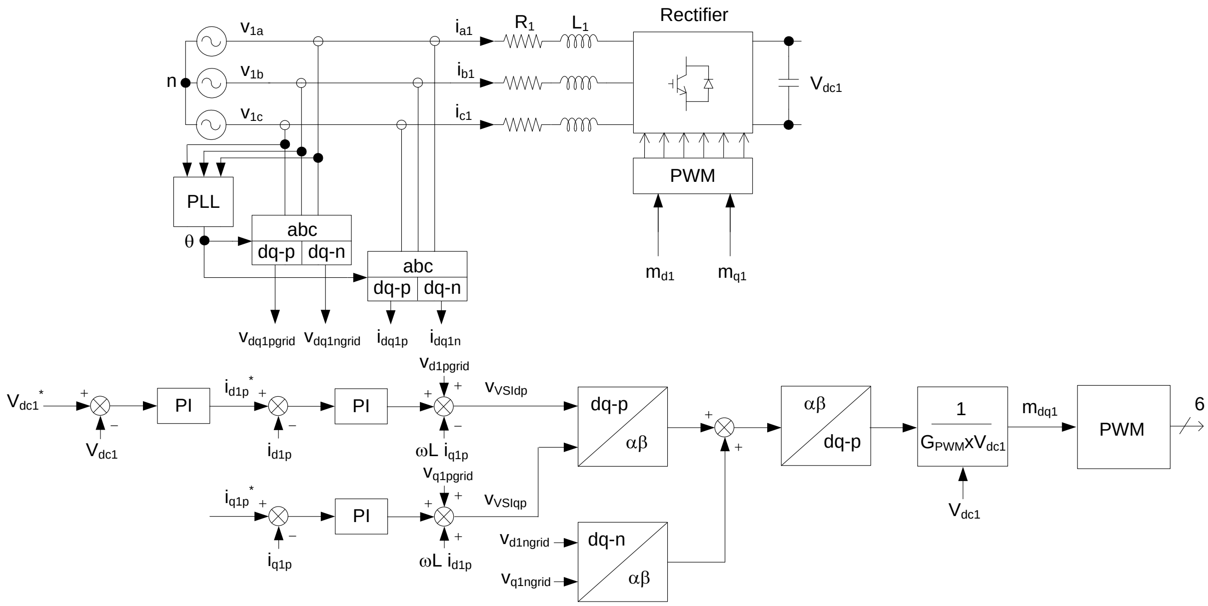


Fig. 2. DEPT control. Input stage.

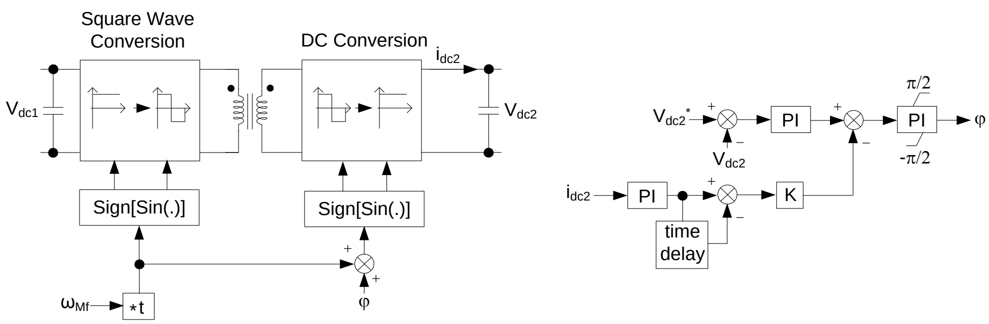


Fig. 3. DEPT control. Isolation stage.

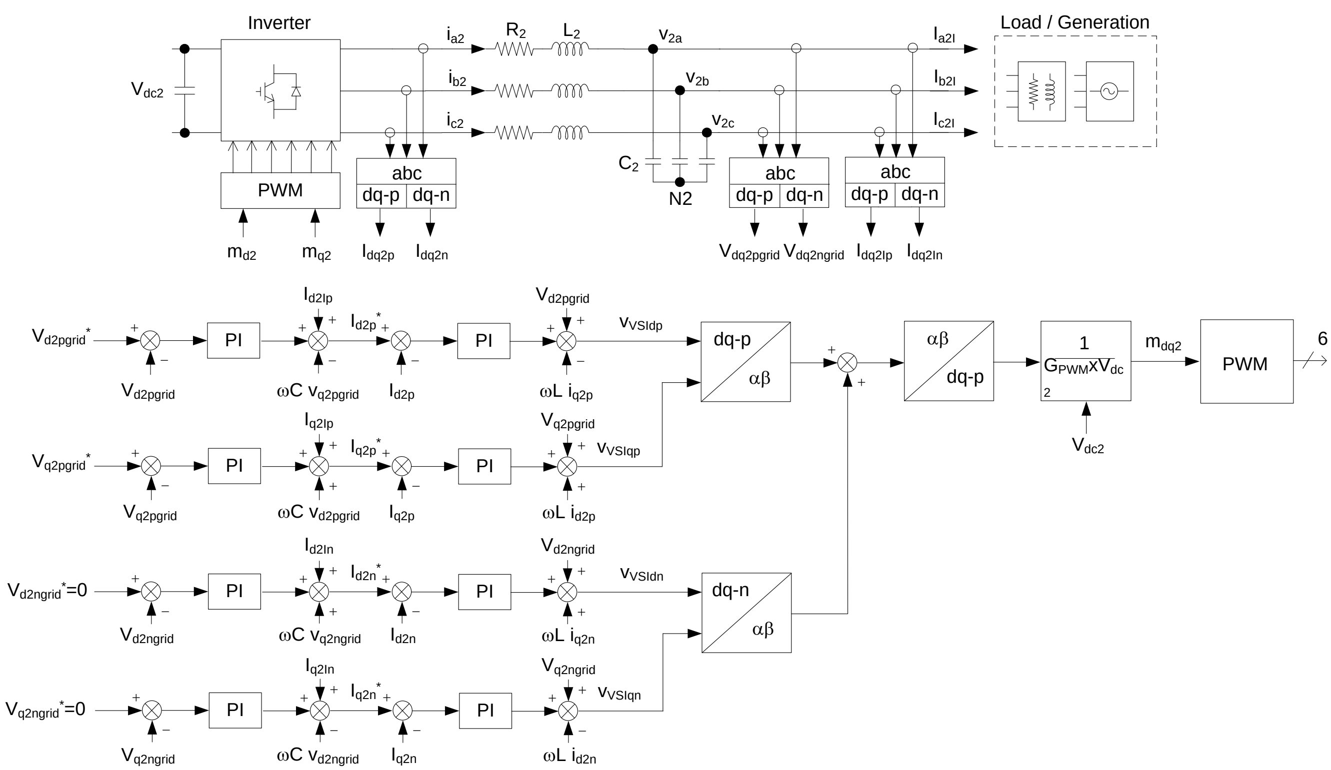


Fig. 4. DEPT control. Output stage.

B. Case Studies

Simulation results obtained from three case studies are presented below to illustrate the DEPT performance.

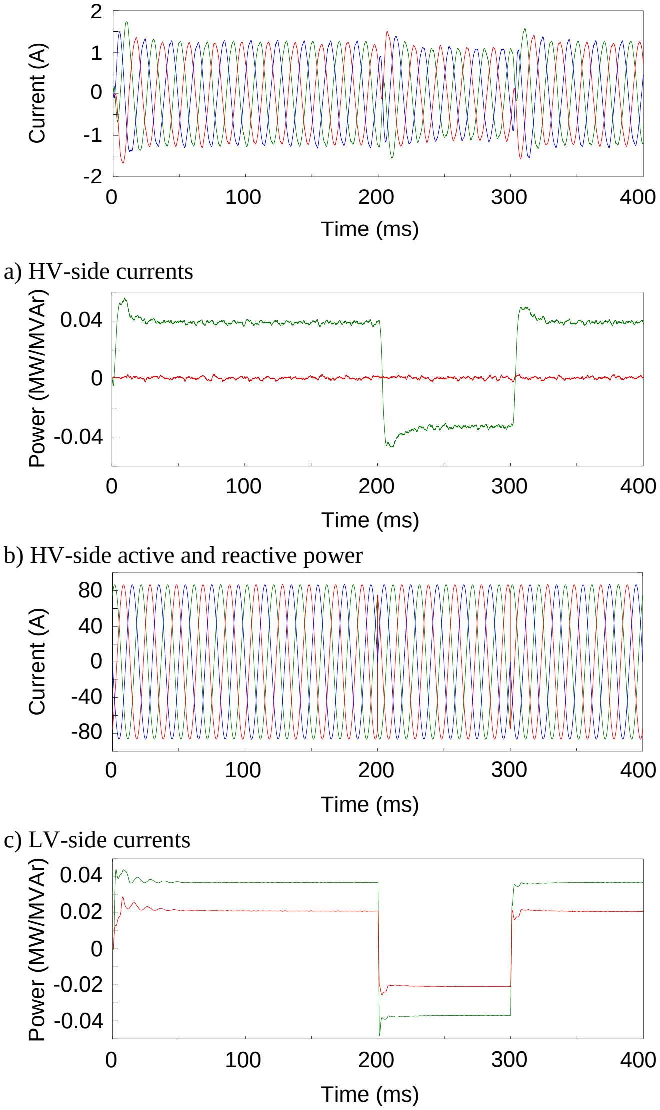
(i) Power flux reversion. A delta-connected current source acting as load is fed from the secondary side of the DEPT. Between 200 and 300 ms the current source phase shift is changed to 180º, the source acts as generator and the power flow is reversed.

(ii) Unbalanced voltage sag at the primary side. Between 200 and 300 ms the HV-side phase A voltage value experiments a reduction of 60%.

(iii) Overcurrent condition at the secondary side. The value of the load impedance falls between 200 and 300 ms.

The plots presented in Figures 5 through 7 illustrate some DEPT capabilities. Fig. 5 shows a fast response when active power flow is suddenly reversed, passing from a load characteristic to a generation characteristic. Fig. 6 shows how voltage unbalances in the primary side do not affect to the secondary voltages, just providing the required isolation level. To avoid damages in the converter, secondary side peak current was limited to 200 A by the controller. Fig. 7 shows a case in which the overcurrent originated at the secondary side causes a secondary voltage drop and consequently a decrease of the secondary active power; under these conditions, the primary current exhibits an opposite behavior and decreases.

The global DEPT behavior can be seen from the presented plots: it allows bidirectional power flow maintaining voltages in each side to their respective stable peak values, and do not propagate unbalanced situations appeared in one side to the other side (voltages are maintained constant on the other side; in addition, unity power factor is maintained at the input, while the output has both active and reactive power depending totally of the load connected at the secondary side).



a) HV-side currents

b) HV-side active and reactive power

c) LV-side currents

d) LV-side active and reactive power

Fig. 5. Simulation results: Power flow reversion.

V. Discussion

An important activity has been dedicated to date to the development of new topologies and control strategies for the solid-state transformer [4] - [9], [14]. This work has been aimed at studying the behavior of a bidirectional solid-state transformer under several dynamic and unbalanced situations.

Simulation results show that the disturbances affecting either the input or the output of the DEPT do not propagate to the other side. This uncoupling effect is achieved by the use of large capacitances as DC links (C_{dc1} and C_{dc2}). Fast voltage regulation, reactive power compensation, or waveform control are some of the advanced capabilities that are incorporated into the present version.

This work is part of a research aimed at building a DEPT prototype. Since it is currently based on a computer model, several refinements and improvements are to be introduced before building the prototype. For instance, (i) adding more detail on the transformer and converter models (e.g., add losses to semiconductor models); (ii) using multilevel converters; (iii) considering a four wire configuration (three phases plus neutral) at the LV secondary side.

VI. Acknowledgement

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VII. References

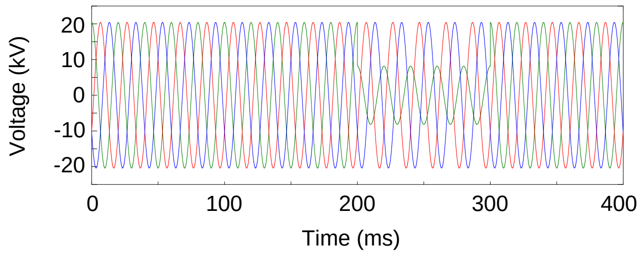
[1] EPRI Report, Development of a New Multilevel Converter-Based Intelligent Universal Transformer: Design Analysis, EPRI, Palo Alto, CA: 2004. 1002159.

[2] W. Kramer, S. Chakraborty, B. Kroposki, and H. Thomas, “Advanced Power Electronic Interfaces for Distributed Energy Systems. Part 1: Systems and Topologies,” NREL/TP-581-42672, March 2008.

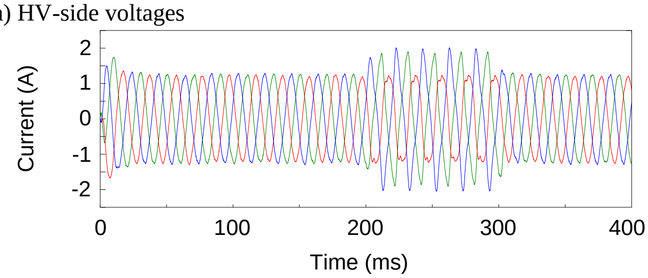
[3] J. Wang, A.Q. Huang, W. Sung, Y. Liu, and B. Jayant Baliga, “Smart grid technologies,” *IEEE Industrial Electronics Magazine*, vol. 3, no. 2, pp. 16-23, June 2009.

[4] M. Kang, P.N. Enjeti, and I.J. Pitel, “Analysis and design of electronic transformers for electric power distribution system,” *IEEE Trans. on Power Electronics*, vol. 14, no. 6, pp. 1133–1141, November 1999.

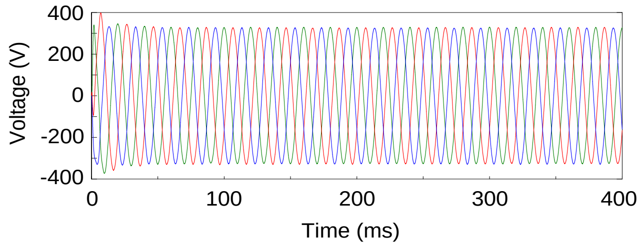
[5] E.R. Ronan, S.D. Sudhoff, S.F. Glover, and D.L. Galloway, “A power electronic-based distribution transformer,” *IEEE Trans. on Power Delivery*, vol. 17, no. 2, pp. 537–543, April 2002.



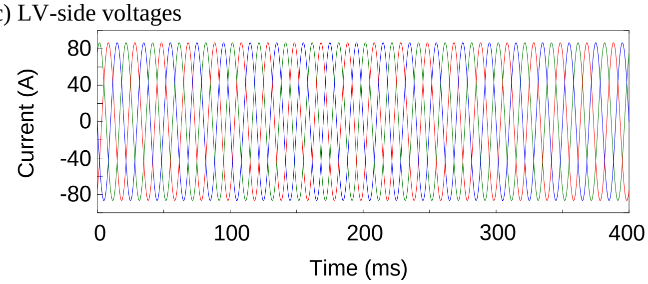
a) HV-side voltages



b) HV-side currents

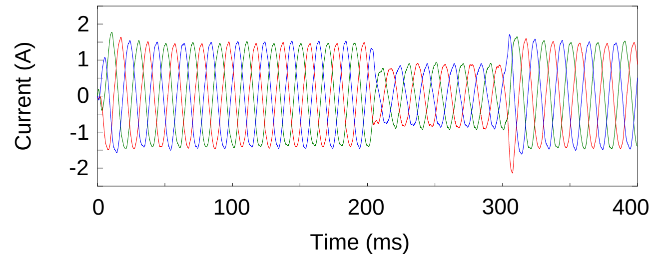


c) LV-side voltages

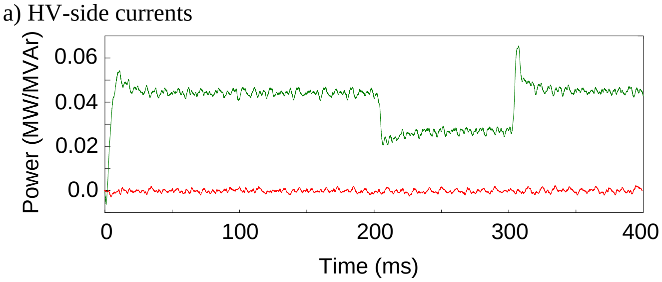


d) LV-side currents

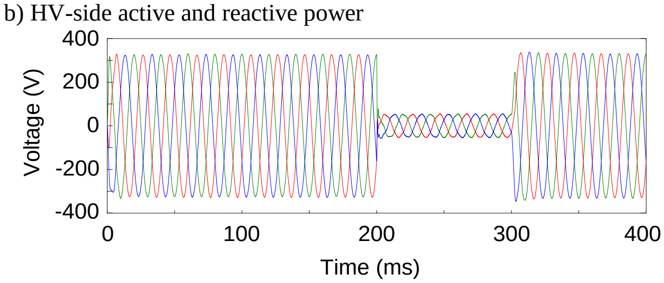
Fig. 6. Simulation results: Unbalanced voltages at the primary side.



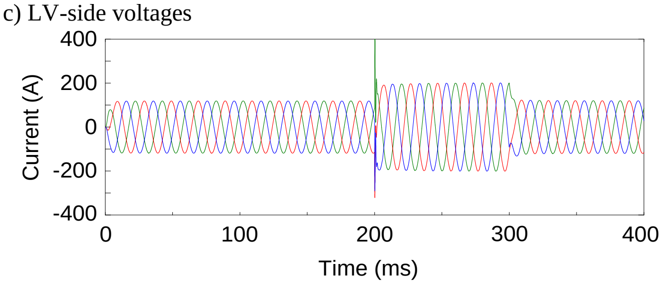
a) HV-side currents



b) HV-side active and reactive power



c) LV-side voltages



d) LV-side currents

Fig. 7. Simulation results: Overcurrents at the secondary side.

[6] D. Wang, C.X. Mao, J.M. Lu, S. Fan, and F. Peng, "Theory and application of distribution electronic power transformer," *Electric Power Systems Research*, vol. 77, no. 3, pp. 219-226, 2007.

[7] H. Liu, C. Mao, J. Lu, and D. Wang, "Optimal regulator-based control of electronic power transformer for distribution systems," *Electric Power Systems Research*, vol. 79, pp. 863–870, 2009.

[8] H. Iman-Eini, Sh. Farhangi, J.L. Schanen, and M. Khakbazan-Fard, "A modular power electronic transformer based on a cascaded H-bridge multilevel converter," *Electric Power Systems Research*, vol. 79, pp. 1625–1637, 2009.

[9] D. Wang, C. Mao, J. Lu, J. He, and H. Liu, "Auto-balancing transformer based on power electronics," *Electric Power Systems Research*, vol. 80, pp. 28–36, 2010.

[10] J. Martin-Arnedo, F. Gonzalez, J.A. Martinez, and S. Alepuz, "Development and testing of a distribution electronic power transformer model," *IEEE PES General Meeting*, San Diego, CA, USA, July 2012.

[11] B. Singh, B.N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D.P. Kothari, "A review of three-phase improved power quality ac–dc converters," *IEEE Trans. on Industrial Electronics*, vol. 51, no. 3, pp. 641–660, June 2004.

[12] J.R. Rodriguez, J.W. Dixon, J.R. Espinoza, J. Pontt, and P. Lezana, "PWM regenerative rectifiers: State of the art," *IEEE Trans. on Industrial Electronics*, vol. 52, no. 1, pp. 5–22, February 2005.

[13] H. Liu, C. Mao, J. Lu, and D. Wang, "Electronic power transformer with supercapacitor storage energy system," *Electric Power Systems Research*, vol. 79, pp. 1200–1208, 2009.

[14] N.M. Tan, T. Abe, and H. Akagi, "Design and performance of a bidirectional isolated DC–DC converter for a battery storage system," *IEEE Trans. on Power Electronics*, vol. 27, no. 3, pp. 1237–1248, March 2012.

[15] D. Kim and D. Lee, "Inverter output voltage control of three-phase UPS systems using feedback linearization," *33rd Annual Conf. IEEE Ind. Electronics Society* (*IECON*), Taipei, Taiwan, November 2007.

[16] D. Lee and J. Jang, "Output voltage control of PWM inverters for stand-alone wind power generation systems using feedback linearization," *Industry Applications Conf.14th IAS Annual Meeting*, vol. 3, pp. 1626-1631, October 2005.

[17] P.C. Loh, M.J. Newman, D.N. Zmood, and D.G. Holmes, "A comparative analysis of multiloop voltage regulation strategies for single and three-phase UPS systems," *IEEE Trans. on Power Electronics*, vol. 18, no. 5, pp. 1176–1185, September 2003.

[18] J. Dai, D. Xu, and B. Wu, "A novel control scheme for current-source-converter-based PMSG wind energy conversion systems," *IEEE Trans. on Power Electronics*, vol. 24, no. 4, pp. 963–972, April 2009.

[19] M. Fatu, C. Lascu, G. Andreescu, R. Teodorescu, F. Blaabjerg, and I. Boldea, "Voltage sags ride-through of motion sensorless controlled PMSG for wind turbines," *Industry Applications Conf. 42nd IAS Annual Meeting*, pp.171-178, September 2007.