Modeling of Modular Multilevel Converters for the France-Spain link

S. Dennetière, S. Nguefeu, H. Saad, J. Mahseredjian

***Abstract*-- The VSC based HVDC link between France and Spain (INELFE project: France-Spain ELectrical INterconnection) will be the most powerful VSC link by 2014. Commissioning of the link is planned in the late 2014. The French TSO RTE is currently conducting studies on this future installation.**

The large number of switching elements in Modular Multilevel Converters (MMC) introduces several complexities for modeling the converter in electromagnetic transient type (EMT-type) simulation programs. Depending on the type of phenomena being analyzed on the HVDC link, various types of EMT and phasor models are available. A brief description of the nature of these models is presented along with their application fields. The generic models developed and used in EMT tools by RTE are presented and discussed. Both offline and real-time implementations are addressed. Next, some electromagnetic transient studies based on the generic models are presented and analyzed: starting sequences, dynamic performances following AC and DC disturbances. The results of these studies are compared against the performances of actual equipment.

***Keywords*: HVDC VSC, Modular Multilevel Converters, Electromagnetic Transient simulation, EMTP, INELFE project.**

I. INTRODUCTION

Interconnections between national electrical grids have been historically developed along with each country's internal networks. Interconnections were initially used for external support in the event of failure affecting the security of the national electrical supply. However, it has been demonstrated that interconnections are not only useful for exceptional situations, but also offer outstanding advantages under normal operating conditions, such as optimizing the electrical power stations' daily production, increasing opportunities for operation with renewable energies, the creation of competition and improvement of supply conditions.

The importance of these interconnections explains why organizations managing European networks are currently working on about fifty projects to enhance existing interconnections in accordance with directives from the European Union. The Spain-France electrical interconnection between Spain and France currently consists of four AC lines (the last line was built in 1982): Arkale-Argia, Hernani-Argia, Biescas-Pragneres and Vic-Baixas. These lines have a total commercial exchange capacity of 1,400 MW, meaning that they represent only 3% of the current maximum demand in the peninsula.

The new HVDC line will allow doubling the current interconnection capacity, which will result in increased security of supply and, above all, greater stability of the grid by increasing its connection with the European system.

The new electrical interconnection line between Spain and France has a length of 64.5 km, 33.5 in France and 31 in Spain. It connects the towns of Baixàs, in the Roussillon region (France), and Santa Llogaia, in Alto Ampordá (Spain) as presented in Fig. 1.

Converter stations are designed and built by SIEMENS. Prysmian Cables & Systems has been awarded the contract for the installation of cables. More information on this project is available in [1].

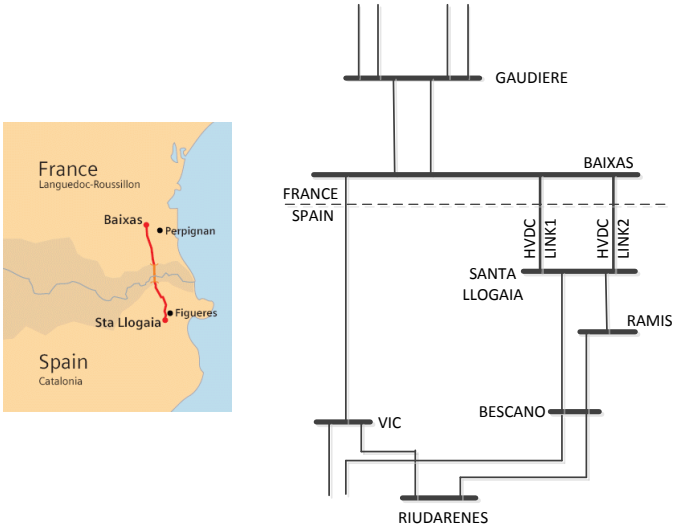

Fig. 1 VSC link location between France and Spain

This new HVDC interconnection will be the first VSC installation operated and maintained by the French (RTE) and the Spanish (REE) Transmission System Operators (TSO). RTE decided to acquire competences in modeling and simulation of VSC based equipment. Competences in this field were required for the INELFE project but, above all, were mandatory for the numerous HVDC and FACTS projects that are planned in a near future in the French grid.

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Collaborations with Ecole Polytechnique de Montréal in Canada and Ecole Centrale de Lille in France have been set up to develop models and tools suitable for electromagnetic transient (EMT) studies with VSC. The models and studies are presented in the following sections.

II. Characteristics of the Interconnection

The interconnection is composed of 2 HVDC links. Each link has two MMC terminals with a rated transmission capacity of 1,000 MW (+/-300Mvar) and a DC voltage of ±320 kV. A simplified single line diagram is presented in Fig.2. Each link is composed of 2 symmetrical monopole converters, 2 step down transformers and 2 underground cables.

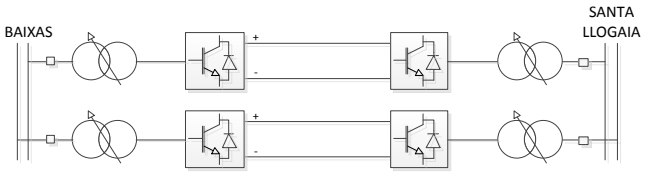


Fig.2 Single line diagram of the interconnection

VSC-HVDC technology, using the modular multilevel converter (MMC) topology, has been selected for this project due to the dynamic performance, power flow control requirements and the low AC short-circuit ratio of the France-Spain system.

Several hundreds of levels are commonly used in multilevel converters. Few years ago full detailed modeling representing the nonlinear characteristics of converter components was not feasible. EMT type simulations would have lasted several days to simulate an event of only a few seconds. Nevertheless due to the constant evolutions in computer processor speed and in the performance of numerical techniques, full detailed modeling of converters is now feasible, but still consumes significant time especially for repetitive studies and screening of operational scenarios. That is why simplified models are still required and remain very efficient and useful when the details of switching devices do not impact on the analyzed system behavior.

A. VSC MMC topology

The main concept of this topology is to generate a practically pure sinusoidal waveform from the DC voltage. Each arm behaves as a controllable voltage source with a high number of possible discrete voltage steps [2]. Fig. 3 shows the MMC topology. Each phase consists of one upper arm and one lower arm. For the INELFE project each arm is composed of more than 400 sub-modules. Each sub-module is a half bridge cell that contains a capacitor C and two IGBT/diode switches (S1 and S2). At any instant during normal operation, only one of the two switches (S1 or S2) is ON. As a result, when switch S1 is ON (S2 is OFF) the voltage at the sub-module terminal is the voltage at the capacitor terminals and when switch S2 is ON (S1 is OFF) the sub-module voltage is zero. The arm reactors help controlling and balancing circulating currents in the phase arms and also limiting fault currents [2]. A high speed bypass switch and a thyristor are integrated in each sub-module to protect the diodes against high currents values. DC fault currents will flow from the AC to the DC side of the MMC through the free-wheeling diodes which have low capacity to withstand high surge currents. That is why the thyristor is fired during the fault allowing most of the current to flow through the thyristor and not through the diodes.

The 1,050 MVA transformers are composed of 3 single phase units. The secondary winding is connected in delta to block the zero-sequence voltages generated by the MMC.

Due to the symmetrical monopole configuration no reference to ground is available in the delta side of the transformer. The star point reactor is used to give this reference. It is composed of high impedances connected to ground.

In order to limit the inrush currents during the starting sequence, the converter is energized through insertion resistors. These resistors are connected between the transformer and the converter and used to limit the inrush current due to capacitor charging.

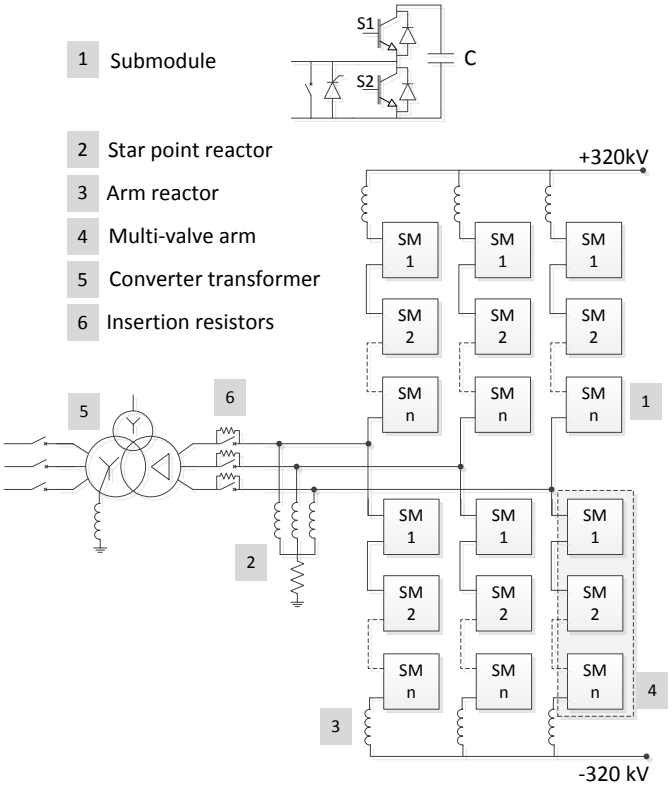


Fig. 3 Converter station – detailed view

B. Main data of the interconnection

The main parameters of the interconnection are given in TABLE I. Due to confidentiality issues, only generic data is provided in this section.

TABLE I
CONVERTER STATION - MAIN PARAMETERS

Converter transformer	Nominal voltage primary	400 kV
	Nominal voltage secondary	333 kV
	Rated power	1050 MVA
	Leakage impedance	18%
Converter reactor	Inductance	50 mH
Insertion resistor	Resistance	5 kΩ
Star point reactor	Inductance	5000 H
	Resistance	5 kΩ
Sub-module	Number of sub-module per valve arm	400
	Individual capacitance	10 mF

XLPE cables are used to transmit power between the 2 converter stations. The length of each cable is around 64.5 km (258 km in total). The cable cross section is 2,500 mm² with copper core, dry insulation and aluminum sheath. Detailed data for EMT studies is provided in Fig. 4 and TABLE II.

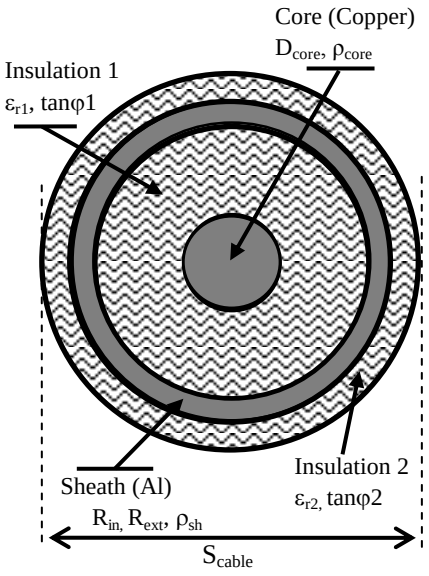


Fig. 4 Cable description

TABLE II
DC CABLE - MAIN PARAMETERS

D_{core} (mm)	64	R_{ext} (mm)	55.1
ρ_{core} (Ωm)	$1.84x10^{-8}$	ρ_{sh}(Ωm)	$2.8x10^{-8}$
ε_{r1}	2.3	ε_{r2}	2.3
tanφ1	0.0004	tanφ2	0.001
R_{in} (mm)	52	S_{cable} (mm)	139.2

III. MMC MODELING IN EMT TOOLS

The very large number of semi-conductors embedded in MMCs complicates the modeling of such converters in EMT-type simulation tools. Simplified models and efficient numerical techniques must be used to overcome computational speed issues while maintaining sufficient accuracy according to the analysis needs.

A. Main challenges

More than 10,000 semi-conductors (IGBT and diodes) are used in each INELFE converter. With detailed models based on this topology, the number of electrical nodes and control signals become extremely large. Two solutions are available for overcoming computational speed issues.

The first solution is to improve applied numerical techniques to solve very large system matrices much faster. This solution can be very complex because it requires modifications in the core of the computational engine and research in numerical techniques.

The second solution is to develop simplified models that contain less electrical nodes. In this case, results given by such models have to be carefully compared against results obtained with full detailed models in order to validate the simplifications and verify limitations.

B. Detailed models

Detailed MMC models have been proposed in [3]. The EMT model for half bridge cell sub-module (SM) is presented in Fig. 5a. The IGBT switches are modeled using an ideal controlled switch and two non-ideal (series and anti-parallel) diodes (Fig. 5b). The non-ideal diodes are modeled as nonlinear resistances using diode V-I characteristic functions.

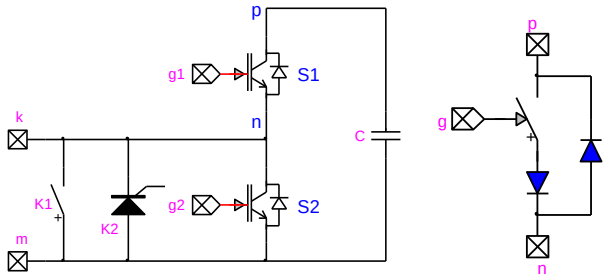


Fig. 5 a) MMC sub-module, b) IGBT valve model

The SMs are assembled in series to make up a multi valve arm. This type of model offers several advantages due to its accuracy in the modeling of IGBTs. It replicates the nonlinear characteristics of semi-conductors based on manufacturers' data sheet or measurements. It allows modeling all internal converter details and operational modes. The size of the electrical system based on this description can be extremely large. For a 401-level MMC converter the total number of electrical nodes is: 4 [Nodes/SM]*400[SM/valve arm]*6[arm/converter] = 9600 nodes. When such a model is implemented in the simulation tool EMTP-RV [4] , specific equations are required to describe ideal switches and diodes and the size of the final matrix to be solved at each time-step reaches around 20,000 x 20,000 for 1 converter. Such large systems require the usage of robust and fast sparse matrix solvers. In addition to the existing sparse matrix package in EMTP-RV, the KLU [5] method is tested in this paper for improving computational performance. This solver is known to be efficient when the system can be ordered into a block triangular form. But Block Triangular Factorization (BTF)

does not seem to be easily applicable in the present context because the system matrix is similar to a band matrix (a large number of devices are connected in series).

Another approach tested in this paper is the usage of ideal diode models instead of non-linear models and optimization of the sparse matrix solver proposed by default in EMTP-RV. The main idea was to force the solver to avoid reordering as much as possible during the simulation process. A simple solution is to add a resistor in parallel with the diodes D1 and D3 as presented in Fig. 6. The resistance is chosen to be sufficiently high thus avoiding any physical perturbation in the proposed model.

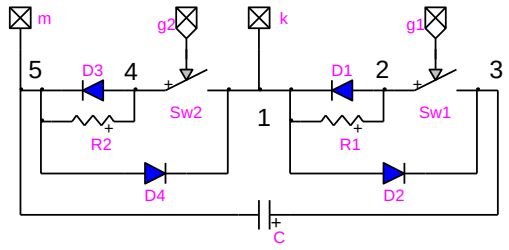
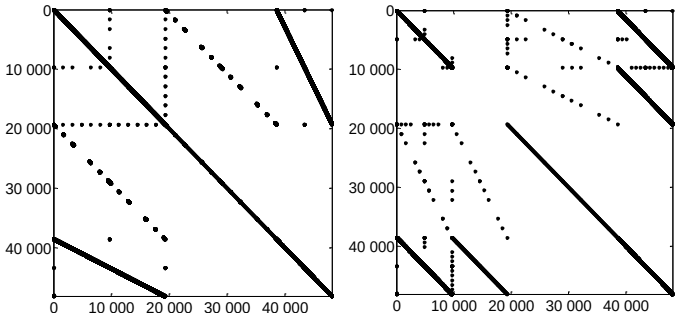


Fig. 6 Sub-module – modified model

By using modified-augmented-nodal analysis (MANA - [4]), the sub-module model presented in Fig. 6 is represented by equation (1) when Sw1, Sw2, D1, D3 and D4 are open and D2 is closed. This is one of the possible sub-module configurations during the start-up sequence. $1/R_C$ is the equivalent admittance of capacitor that depends on integration time-step and capacitance C.

$$\begin{bmatrix} \frac{1}{R_1} & -\frac{1}{R_1} & & & & & & & 1 & & 1 \\ -\frac{1}{R_1} & \frac{1}{R_1} & & & & & & & & -1 & \\ & & \frac{1}{R_C} & & -\frac{1}{R_C} & & & & -1 & & 1 \\ & & -\frac{1}{R_C} & & \frac{1}{R_C}+\frac{1}{R_2} & & -\frac{1}{R_2} & & & & \\ & & & & -\frac{1}{R_2} & & \frac{1}{R_2} & & & & -1 \\ & & & & & & & & 1 & & \\ 1 & & -1 & & & & & & & & \\ & & & & & & & 1 & & & \\ & & & & & & & & 1 & & \\ & & & & & & & & & 1 & \\ & & & & & & & & & & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ I_{D1} \\ I_{D2} \\ I_{D3} \\ I_{D4} \\ I_{SW1} \\ I_{SW2} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (1)$$

The above coefficient matrix is composed of 4 sub-matrices: admittance matrix **Yn** in the upper left part, ideal switch equations in the matrix **Sd** in the lower right part and connectivity matrices **Sc** (column) and **Sr** (row). The resistors R1 and R2 do not increase the system size and the corresponding admittances fill the **Yn** diagonal cells with non-zero values. Without R1 and R2, 3 zero elements are present in the **Yn** diagonal cells. This situation forces the solver to re-order the system every time a switch or a diode state changes with huge consequences on the simulation speed when the system is composed of thousands of sub-modules. The comparison of the solved time-domain sparse matrix for 1 HVDC link composed of 2 converters and 2 cables is presented in Fig. 7.



a) with R1&R2 resistors b) without any resistor

Fig. 7 Solved time domain sparse matrix for 1 HVDC link

When the non-linear diode models are used, a 1s time domain simulation of 1 HVDC link composed of 2 converter stations, 2 cables and a simple AC network requires 3400s on a standard laptop computer. The same simulation with ideal diode models and resistors requires 20% less time. When the ideal diodes are used without resistors, the simulation runs 100 times slower than the simulation with ideal diodes and resistors.

C. Detailed equivalent models

In order to decrease computational times, detailed equivalent models have been proposed in [6] and [7]. The main idea is to reduce the number of electrical nodes in the converter model. Detailed equivalent models presented in [6] and [7] also eliminate the possible conduction states. A more accurate detailed equivalent model has been proposed in [7]. In addition to gate signals and current direction, the model proposed in [7] takes into account the voltage across each diode in order to choose resistance values. The time-step used to run this model is between 5µs and 10µs due to the large number of switching devices.

Each valve arm is composed of a Norton equivalent circuit updated from gating signal and current direction. The number of electrical nodes in the main network matrix is reduced to 11 per converter. This number does not depend on the number of SMs in converter. For a MMC-401 levels, this type of model usually runs 30 to 50 times faster than full detailed models described in the previous section. It is suitable for many applications because of computational speed and the capability to model every SM status correctly. The limitations are in the capability to account for internal faults and converter losses.

D. Average value models

The computational burden introduced by detailed models highlights the need to develop more efficient models that provide similar dynamic response especially on the AC side. These simplified models, also known as average-value models (AVM), replicate the average response of switching devices, converters and controls by using controlled sources and switching or averaged functions. In AVMs, the IGBTs are not explicitly modeled and the MMC converter behavior is represented using controlled voltage and current sources. The controlled sources may also include the harmonic content from

the modulation control (or switching functions) on the AC voltage waveforms. Similar to the detailed MMC, the reference voltages are the output voltages obtained from the vector control where amplitude and phase are controlled independently. A detailed description of the AVM approach can be found in [3] and [10]. These models are useful to perform studies with small AC disturbances. They are not adapted for large AC under voltages and over voltages.

IV. Studies performed by RTE

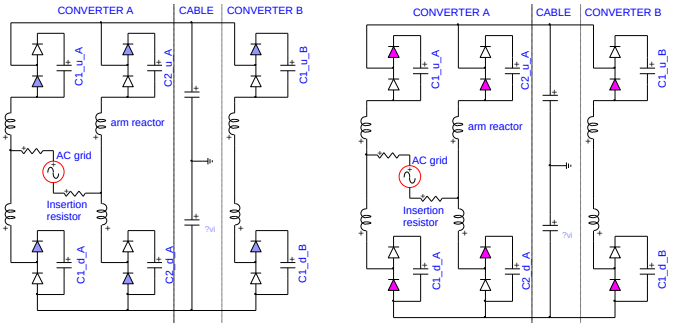
An overview of studies performed with the aforementioned models is presented in this section. For each study, the most suitable type of model is proposed.

A. Startup sequence analysis

The startup process of the MMC is complex since at the beginning of the process all capacitors are required to be equally charged to a certain level before being able to operate. Moreover, current and voltage stresses in the power switches and on the AC grid have to be limited during start-up. The starting sequence of INELFE converters is similar to the scheme presented in [9].

The system has to be driven from the STANDBY state with the AC breakers at both converter stations initially open as well as the breakers across the insertion resistors and no firing signals on the IGBT gates, to the COUPLED state where all capacitor modules and cables are charged, AC breakers are closed and power is transferred. The cables are considered always connected to the DC terminals on both sides.

Let A be the first station to be connected to the AC grid and B is the other station. The star point reactor is only grounded at terminal A to provide a reference for the voltages.



a) Charging state 1 b) Charging state 2

Fig. 8 Simplified charging diagram with side A energized

After closing the AC grid breaker on side A, inrush currents are observed due to the saturation of transformers and capacitor charging. All module capacitors and DC cable capacitors are charged through the insertion resistors of side A and the diodes of both sides. Fig. 8 presents a simplified circuit to help understanding the charging process. It can be basically divided into two states. State1 (Fig. 8a) corresponds to the positive cycle voltage from AC grid. State2 (Fig. 8b) corresponds to the negative cycle. Conducting diodes are represented by color-filled symbols. Upper and lower valve arms forming a phase arm on side A are charging alternatively in state1 and state2, whereas on side B, they are charging simultaneously with half DC voltage. Thus at the end of the passive charging process, side B capacitor voltages are half the side A capacitor voltages.

Upon stabilization of DC voltages, the insertion resistors are short-circuited thanks to the bypass breakers. Then the voltage rises across side A and side B module capacitors and cables.

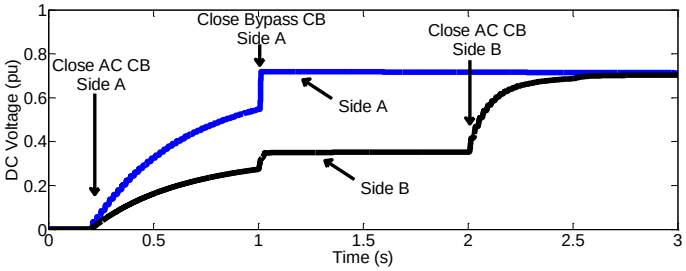


Fig. 9 SM capacitor voltages during start-up

When the DC voltage is stabilized, the module IGBTs at side A are activated to control the DC voltage, the reference being equal to the previously achieved pole-to-pole steady state voltage. When the oscillations due to the activation are damped, the voltage reference is ramped up to 1 pu. An intermediary IDLE mode may be necessary to balance the voltages across the modules without any impact at the AC side and at the DC side of the converter. Such a mode is described in [8]. This process is repeated for station B: AC breaker is closed leading to further charging of side B module capacitors from half their nominal voltage, via the diodes and the insertion resistor. Then side B resistors are short-circuited yielding a step in the module capacitor voltages. After stabilization, side B IGBTs are activated. DC voltage reference is ramped up from the actual stabilized value to 1 pu. At this stage two controllers are regulating DC voltage at the same set point at both ends of the cables. No active power is transferred between stations A and B. To initiate power transfer, the controller of the sending end is switched from the DC voltage regulation mode to the active power regulation mode. Real and reactive power references are ramped up from 0 pu to the desired final output. The detailed models presented in sections III. B. and III. C. are required to study startup sequence because semi-conductor states have to be modeled in details. When detailed equivalent models are used, an iterative process for diodes states will avoid numerical oscillations issues.

The interconnection is composed of 2 HVDC links. The impact of starting a second link when the first link already operates has been also studied. This study does not show any interaction problems.

B. AC faults

3-phase faults and unbalanced faults are studied in this section. Tuning AC protection systems in the vicinity of the HVDC substations is dependent on the fault current that may be injected by converters. For symmetrical faults average value models are used. The system has been specified to

reduce real power (P) reference and increase reactive power (Q) generation during faults i.e. when AC RMS phase to phase voltage is below 380 kV. For an HVDC VSC link, one side usually controls real/reactive power and the other side controls reactive power and DC voltage. These control strategies are assigned to each side independently of the power direction, but it can lead to differences in dynamic performances as explained below. In the following discussion a 3-phase metallic fault occurs at t=1.5s and is clear at t=1.7s.

First assumption: the sending end controls P while the receiving end controls the DC voltage (V_{dc}). This is the classical scheme for VSC high level controls.

- When a fault occurs in the rectifier's side AC grid, the AC voltage drop results in a P drop hence V_{dc} drops and hits its lower limit before the fault is cleared and power transmission resumed.
- When a fault occurs at the inverter's side AC grid, P injection from the rectifier continues thus V_{dc} rises and hits its upper limit.

Second assumption: the sending end controls V_{dc} while the receiving end controls P.

- When a fault occurs in the rectifier's side AC grid, there is a lack of power to maintain the V_{dc} level which drops and hits its lower limit.
- When a fault occurs at the inverter's side AC grid, P drops causing V_{dc} to slightly rise. But since it is still regulated by the safe side of the link, V_{dc} comes quickly back to its nominal value.

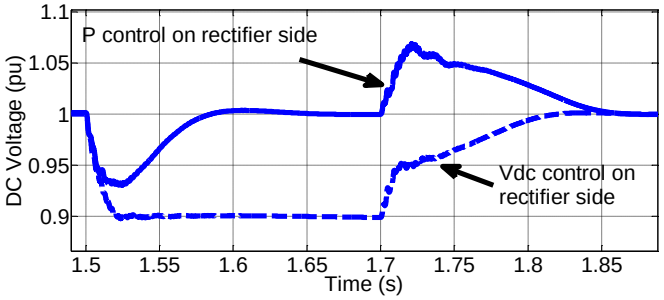


Fig. 10 DC voltage during 3-phase fault on sending end

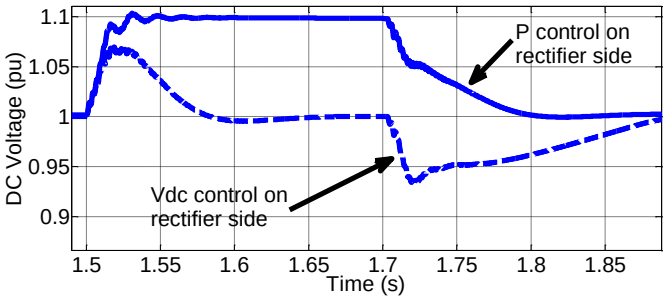


Fig. 11 DC voltage during 3-phase fault on receiving end

It is observed that the contribution of the converter station to the 3-phase fault is about 2200 A, i.e. high enough to be used for fault detection purposes. Regarding single phase to ground faults, the DC voltage is very similar to the 3-phase fault cases. When detailed models presented in [3] are used, the AC currents fed by converters are unbalanced. This is a limitation of the presently used control system models in RTE because, in reality, converters provide only positive sequence currents whatever the type of fault (balanced or unbalanced) [10]. Algorithms are implemented to balance energies among the 3 converter arms so that converters only provide positive sequence currents. Such a feature improve the ride-through capability of the link with respect to high impedance or remote single phase to ground faults, but simultaneously it is important not to jeopardize fault detection and clearing.

C. Temporary AC overvoltages

In this section, the behavior of the converter under AC voltage fluctuations is investigated. When AC peak voltages are very high with respect to DC pole voltages, the freewheeling diodes can conduct in such a way that AC phase to ground voltage is directly applied to the DC cable, rated at ±320 kV. Assuming at the secondary of the transformer a 333 kV nominal line-to-line voltage, the condition to have the AC overvoltage transferred to the DC side is:

$$U[pu] \geq \frac{320}{333}\sqrt{\frac{3}{2}} = 1.18\,pu \qquad (2)$$

Actually thanks to the third-harmonic component (roughly 15%) which is added to the sine wave in the controller to improve the modulation index of the converter, the system can cope with up to 1.35 pu AC overvoltage before any uncontrolled freewheeling diode conduction.

Exceptional AC overvoltages above 1.42 pu i.e. 5% more than 1.35 pu will result in a DC pole to ground voltage greater than 336 kV, which is the maximum tolerable continuous DC voltage. Hopefully AC voltages above 1.42 pu remain extraordinary, and there is no special action to be foreseen beyond the surge arresters which come into operation to maintain cable voltage below 1.8 pu in particular when a DC pole to ground fault occurs.

D. DC faults

Two types of DC faults can occur: pole-to-pole or pole-to-ground. Although a pole-to-pole fault is very unlikely in cables, the probability of occurrence still exists especially after the maintenance period of the converter hall. Faults on dc cables are considered permanent and protection scheme can just completely trip the dc link for fault clearance and repair. Generally, the pole-to-ground fault is more likely than the pole-to-pole fault. However, the pole-to-pole fault is more critical in the symmetrical monopole configuration due to high fault currents. On the contrary the pole-to-ground fault may merely result in the overvoltage of the healthy pole.

During the dc-link fault, the freewheeling diodes act as uncontrolled rectifier bridges and create a dc fault current through the short-circuit point on the dc link. The fault current cannot be cleared until the circuit breaker on the ac side is opened since the dc arc on the short-circuit point cannot be extinguished. Before fault clearance, the freewheeling diodes will experience high fault current. That is why, for the

INELFE project, the protection devices presented in Fig. 5a (thyristor and bypass switch) are embedded in every SM. More complex protection devices, as proposed in [9], are not required because non-permanent dc fault has not been considered for the design of the station.

DC faults should be studied with detailed models since conduction nonlinearity and commutation of diodes have to be taken into account. The detailed equivalent model could also give accurate results, however it must be always validated against the detailed model.

A zero-resistance pole-to-pole fault is simulated with detailed and detailed equivalent models. Results are presented in Fig. 12. Two current components can be identified in the pole-to-pole fault. The first current component comes from the energy stored in cables. The second current component comes from the AC grid. When such a fault is detected, the IGBTs of all converters are blocked and the thyristors K2 (see Fig. 5a) are fired. Thyristors fire to protect freewheeling diodes against overcurrents. The bypass switch K1 is closed in a second step. In this study K2 is closed when the current in arms exceeds 6pu, which occurs 350µs after fault ignition. The fault continues to be fed by the AC grid and the cable capacitance. The AC breaker then operates after 2 cycles. After the AC breaker is operated the fault current is only fed by the cable capacitance. During the DC fault the freewheeling diodes and switches K1 and K2 conduct and SM capacitors are floating. As a consequence converters are still charged after the fault clearing. Many minutes can be required to discharge the capacitors through small resistors embedded in SM electronic boards.

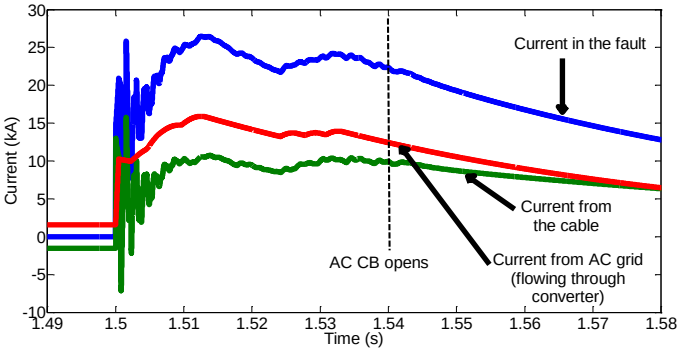


Fig. 12 Pole-to-pole fault – DC currents

V. Conclusions

The 2000 MW France-Spain link will be the first VSC link operated by RTE and REE by 2014. RTE decided to acquire competences in modeling and simulation of VSC based equipment. Competences in this field were required for the INLEFE project but, above all, were mandatory for the numerous HVDC and FACTS projects that are planned in a near future on the French grid. MMC introduces challenges for the modeling of such converters in EMT simulation tools. Due to the lack of generic models available in EMT tools a major commitment of RTE has been required to develop a large range of MMC models suitable for network studies. These models are now available to third party for testing and improvements. They are useful for preliminary studies performed by TSO when HVDC VSC installations are planned. These generic models and some typical network studies have been presented in this paper and in [3] (control system part). They have been compared and validated against results given by the manufacturer and typical results available in the literature. Next, specific models of the interconnection, based on these generic models, will be developed. In addition to modeling activities in the field of FACTS and HVDC, RTE decided to build a real-time laboratory that hosts a replica of the control system cubicles installed on site. Studies with the real controllers connected to the HYPERSIM real-time simulator will be performed before final commissioning of the France-Spain link. The dynamic performances of the link will be assessed and compared with tests done by the manufacturer with an RTDS real-time simulator. Moreover this simulation platform will give a tremendous opportunity to validate the specific EMT models of the link.

VI. References

[1] INELFE official web site : http://www.inelfe.eu

[2] B. Gemmell, J. Dorn, D. Retzmann, and D. Soerangr, “Prospects of Multilevel VSC Technologies for Power Transmission,” in Proc. IEEE Transmission and Distribution Conf. Exp., pp. 1-16, Milpitas, CA, Apr. 2008.

[3] J. Peralta, H. Saad, S. Dennetière, J. Mahseredjian, and S. Nguefeu, “Detailed and Averaged Models for a 401-level MMC-HVDC system,” IEEE Trans. on Power Delivery, vol. 27, no. 3, July 2012, pp. 1501-1508.

[4] J. Mahseredjian, S. Dennetière, L. Dubé, B. Khodabakhchian and L. Gérin-Lajoie: “On a new approach for the simulation of transients in power systems”. Electric Power Systems Research, Volume 77, Issue 11, September 2007, pp. 1514-1520

[5] Natarajan, “KLU A high performance sparse linear solver for circuit simulation problems,” Master’s Thesis, University of Florida, 2005

[6] Gnanarathna U., Gole A. & Jayasinghe R., "Efficient Modeling of Modular Multilevel HVDC Converters (MMC) on Electromagnetic Transient Simulation Programs", IEEE Transactions on Power Delivery, Vol 26, Pages 316 -324, January, 2011.

[7] P. Le-Huy, P. Giroux, J.-C. Soumagne, " Real-Time Simulation of Modular Multilevel Converters for Network Integration Studies", International Conference on Power Systems Transients, Delft, The Netherland, June 2011.

[8] Keyan Shi, Feifei Shen, Dong Lv, Ping Lin, Min Chen, Dehong Xu, "A novel start-up scheme for modular multilevel converter," Energy Conversion Congress and Exposition (ECCE), 2012 IEEE , pp.4180-4187, 15-20 Sept. 2012

[9] Xiaoqian Li, "Protection of Nonpermanent Faults on DC Overhead Lines in MMC-Based HVDC Systems," IEEE Transactions on Power Delivery, vol.28, no.1, pp.483-490, Jan. 2013

[10] J. Dorn, H. Gambach, J. Strauss, T. Westerweller, J. Alligan, "Trans Bay Cable - A Breakthrough of VSC Multilevel Converters in HVDC Transmission", Paper presented in the CIGRE symposium on HVDC and Power Electronic Systems for Overhead Line and Insulated Cable Applications – San Francisco 2-6 March 2012.