Real Time simulation of MMCs using the State-Space Nodal Approach

H. Saad, C. Dufour, J. Mahseredjian, S. Dennetière, S. Nguefeu

***Abstract*-- The Modular Multilevel Converter (MMC) topology is becoming an attractive solution for HVDC and FACTS systems. MMC structures are composed from several hundreds to thousands of half-bridge converters. Such large numbers of power switches and electrical nodes introduce important computational difficulties in electromagnetic transient (EMT) type programs. This becomes particularly more complex for performing real-time simulations. The combined state-space and nodal method (SSN) offers an efficient solution for clustering each MMC arm in order to reduce the number of nodes and decrease computation time. Moreover, the proposed approach permits simultaneous parallel computations and maintains accurate results. This paper presents the modeling of MMCs using the SSN method. A practical MMC-HVDC system case is used for testing the model under transient events and the results are validated by comparing with a detailed representation of all MMC components.**

***Keywords*: EMTP, HVDC transmission, Modular multilevel converter (MMC), Portability, Real-Time simulation, Voltage source converter (VSC).**

I. Introduction

THE inclusion of High Voltage Direct Current (HVDC) and Flexible AC transmission system (FACTS) devices in electric power grids is expanding rapidly [1]. The use of voltage source converters (VSCs) based on Insulated Gate Bipolar Transistors (IGBTs) is becoming more attractive mainly due to their higher performances and cost [2]. The recent Modular Multilevel Converter (MMC) topology based on half-bridge modules connected in series [3] offers significant benefits compared to previous VSC technologies, such as two-three level and neutral-point diode-clamped (NPC) topologies [4]. By using a significant number of levels per phase in the MMC, the filter requirements can be eliminated. Moreover switching frequency and transient peak voltages on IGBT devices are lower in the MMC, which reduces converter losses [5]. Scalability to higher voltages is easily achieved and reliability is improved by increasing the number of sub-modules (SMs) per phase [1].

The excessive numbers of power switches in the MMC, create significant computational difficulties in EMT-type simulation tools [6]. The numerous and nonlinear devices in the converter require an iterative process to solve the global matrix which significantly increases the computational burden. Thus, in real-time simulations, modeling a highly accurate switching device is out of reach with the current computational technology and some form of simplification is required to accomplish network integration and hardware-in-the-loop (HIL) studies.

In [7] it has been shown that by simplifying IGBTs/diode devices to the level of a switchable R_{ON}/R_{OFF} resistance, the Norton equivalent of each converter arm can be achieved, which decreases computational burden. In [8] and [9] the later approach has been tested in real-time. However, the algorithm implementation and the blocked state issues of sub-modules have not been investigated.

The inclusion of state-space equation into nodal equations has been applied in [10] (see also [11]) for the purpose of model circuit synthesis from fitted measurements. In [12] the general SSN methodology for the simultaneous interfacing of nodal equations with state-space equations for arbitrary network topologies is presented. It mainly shows that the SSN approach eliminates artificial delays and allows parallel execution of coupled sub-systems, which enhances computational speed.

In this article, the SSN method is applied to the MMC model type proposed in [7]. It will permit clustering and simultaneous parallel computation of each MMC arm. This will enhance accuracy and computational speed for real-time simulations.

A practical MMC based HVDC system is presented. The MMC-SSN model implemented in the SimPowerSystems (SPS) tool for Simulink is validated against a fully detailed MMC model implemented in EMTP-RV [13], which includes the representation of thousands of nonlinear IGBT devices [14]. Performances in real time simulations using the Opal-RT platform are also studied for different numbers of MMC levels.

II. MMC Topology

Fig. 1 shows the studied MMC topology. The MMC modeled in this paper has 100 sub-modules (SMs) per arm (200 SMs per phase). The inductor L_{arm} is added in each arm

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to limit arm-current harmonics and fault currents.

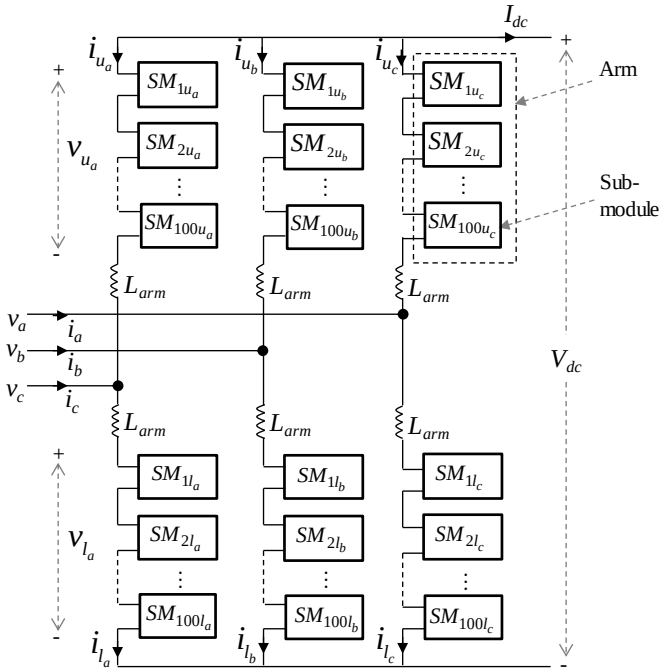


Fig. 1 Typical MMC topology for three-phase converter.

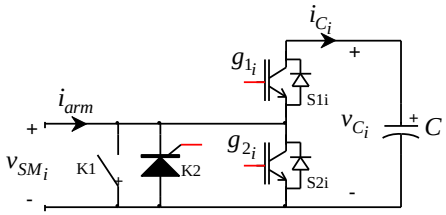


Fig. 2 Detailed diagram of a half-bridge sub-module.

III. Sub-module Operation

Each SM is a half-bridge converter as depicted in Fig. 2, it includes mainly a capacitor *C* and two IGBTs with antiparallel diodes (S1 and S2). Depending on the IGBT technology used in such a converter, the high-speed bypass switch K1 (Fig. 2) is required to increase safety and reliability in case of SM failure, and the thyristor K2 (Fig. 2) is fired to protect the IGBTs against high fault currents [1]. Each SM is controllable by means of two gate signals (g_{1_i} and g_{2_i}). Thus, each SM can have three different states:

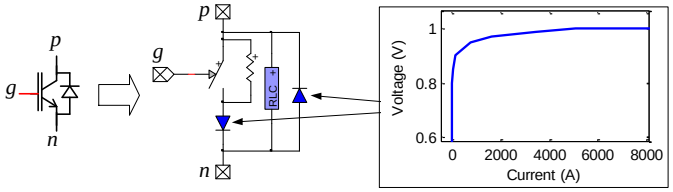
- ON state: g_{1_i} on and g_{2_i} off, SM voltage v_{SM_i} equals capacitor voltage v_{C_i} .
- OFF state: g_{1_i} off and g_{2_i} on, SM voltage equals zero.
- BLOCKED state: g_{1_i} off and g_{2_i} off, SM voltage depends on current arm direction i_{arm} . The capacitor may charge through S2 but it cannot discharge.

IV. MMC model

A. Detailed model

In this approach the IGBT valves are modeled using an ideal controlled switch, two non-ideal (series and anti-parallel) diodes and a snubber circuit, as shown in Fig. 3. The non-ideal diodes are modeled with nonlinear resistances using the classical V-I curve of a diode.

This model type offers several advantages due to its increased accuracy in the modeling of IGBTs. It replicates the nonlinear behavior of switching events (through diodes) allowing to account for conduction losses. The nonlinear characteristics are tuned based on manufacturer's data sheets or field measurements. The introduction of thousands of components (i.e. 1,200 ideal switches and 2,400 non-ideal diodes for a MMC-101 level) causes a high computational effort [14] and therefore, this modeling approach is out of reach for real-time simulation with the actual available processor technology. It should be mainly used as an accuracy reference for validating and tuning simplified MMC models.



a) b)

Fig. 3 a) Representation of a nonlinear IGBT valve, b) Diode V-I characteristic.

B. SSN-MMC model

By Simplifying power switches to become binary resistors (Ron/Roff), and discretizing the SM capacitor as an equivalent current history source $i_{C_i}^h$ in parallel with a resistance $R_C = \Delta t / (2C)$ (Fig. 4), the approach presented in [7] and [8] derives the Norton equivalent circuit of each MMC arm using nodal equations. In the Simulink/SimPowerSystems environment, based on state-space equations, the same discretized Norton equivalent circuit can be derived with the ARTEMiS State-Space Nodal (SSN) solver used in Opal-RT.

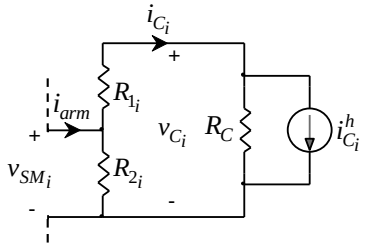


Fig. 4 Discretized Sub-module with simplified IGBT models

1) Brief presentation of the SSN approach

Considering the state-space equations of a generic circuit

$$\begin{cases} \dot{x} = A_K x + B_K u \\ y = C_K x + D_K u \end{cases} \quad (1)$$

where x and u are the state variable and input vectors respectively (they can be either current or voltage variables). The discretization of equation (1) can be derived [12]

$$\begin{cases} \mathrm{x}_{t+\Delta t} = \hat{\mathrm{A}}_K \mathrm{x}_t + \hat{\mathrm{B}}_K \mathrm{u}_t + \hat{\mathrm{B}}_K \mathrm{u}_{t+\Delta t} \\ \mathrm{y}_{t+\Delta t} = \mathrm{C}_K \mathrm{x}_{t+\Delta t} + \mathrm{D}_K \mathrm{u}_{t+\Delta t} \end{cases} \quad (2)$$

where Δt is the integration time-step and the hatted matrices result from the discretization process.

By combining and reorganizing equation (2)

$$y_{t+\Delta t} = C_K \left[\hat{A}_K x_t + \hat{B}_K u_t \right] + \left[C_K \hat{B}_K + D_K \right] u_{t+\Delta t} \quad (3)$$

It is apparent that the above equation has an historic term and can be rewritten as

$$y_{t+\Delta t} = y_{hist} + W_K u_{t+\Delta t} \quad (4)$$

If the input $u_{t+\Delta t}$ is a voltage variable, than W_K is an impedance, y_{hist} and $y_{t+\Delta t}$ are currents variables and equation (4) is therefore the Norton equivalent of the generic circuit.

The SSN solver automatically derives the Norton (or Thevenin) equivalents of SimPowerSystems models by dividing them into branches or groups having the form of equation (4) and solves them simultaneously using a classic nodal admittance method. The SSN solver can also interface 'manually-coded' branches or groups, like the MMC branches presented in this paper. Manually-coded groups enable in particular to optimize the coding with regards to some specific group properties like, for example, the highly repetitive topology of the MMC [18].

2) Norton equivalent model of MMC arm

The following steps (including also the BLOCKED state) and the main equations of the algorithm implemented in Matlab/Simulink are presented in Fig. 5.

The algorithm considers each SM separately and maintains a record of each capacitor voltage and current. It is applicable to any number of SMs per arm.

Real-time simulation requires fast computations. Pre-computation and optimization of the code is necessary to improve computational speed without effecting model accuracy. In the MMC code, as it was reported in section III, each SM can have three circuit configurations depending on the states: ON, OFF and BLOCKED. Thus, in point Fig. 5.d of, the equivalent Thevenin resistance of each SM (R_{SM_i}) and the resistive term that allows computing the Thevenin voltages ($v^h_{\mathrm{SM}_i}$), are pre-computed since they can only have three different values.

In point Fig. 5.b, the ON/OFF states can be computed directly according to gate signals. However, the BLOCKED state is defined depending on state and non-state variables. Thus, the zero-crossing of the arm current variable will cause numerical oscillations. To avoid this problem, the implementation of an iterative process could be a solution; however this approach will require more computing time which is problematic for real-time performance. In order to overcome this issue, a trigger is added to detect and maintain the "High impedance mode" (Fig. 5.b) for one more time-step. Moreover, the SPS/Artemis model uses a hybrid integration solver. Each SSN group (or decoupled circuit) uses a 5th order solver to compute its Norton equivalent circuit, for better precision and the Backward-Euler solver is used to solve the global network circuit to eliminate numerical oscillations when discontinuities occur [18].

a) Retrieve arm voltage from the network solution and compute arm current:

$$i_{arm}(t) = v_{arm}(t).Y_{arm}(t-\Delta t) + i^h_{arm}(t-\Delta t)$$

b) For each SM, set R_1 and R_2 values depending on gating signals, current arm direction, previous SM voltage and previous capacitor voltage:

if ($\mathrm{SM_i}$ ==ON_state)

$\left\{ R_{1_i} = R_{ON} ; R_{2_i} = R_{OFF} \right\}$

elseif ($\mathrm{SM_i}$ ==OFF_state)

$\left\{ R_{1_i} = R_{OFF} ; R_{2_i} = R_{ON} \right\}$

elseif ($\mathrm{SM_i}$ ==BLOCKED_state)$\{$

if $\left(\left(i_{arm}(t) > 0 \right) \&\& \left(v_{SM_i}(t-\Delta t) > v_{C_i}(t-\Delta t) \right) \right)$

$\left\{ R_{1_i} = R_{ON} ; R_{2_i} = R_{OFF} \right\}$

if $\left(\left(i_{arm}(t) < 0 \right) \&\& \left(v_{SM_i}(t-\Delta t) < 0 \right) \right)$

$\left\{ R_{1_i} = R_{OFF} ; R_{2_i} = R_{ON} \right\}$

else % High impedance mode

$\left\{ R_{1_i} = R_{OFF} ; R_{2_i} = R_{OFF} \right\}\}$

c) Compute capacitor voltages and currents for each SM:

$$i_{C_i}(t) = i_{arm}(t) - \frac{v_{R_{2_i}}}{R_{2_i}} \;\; ; \;\; v_{C_i}(t) = \left(i_{C_i}(t) - i^h_{C_i}(t) \right) R_C$$

d) Compute Thevenin equivalent for each SM:

$$R_{\mathrm{SM}_i}(t) = \frac{R_{2_i}\left(R_{1_i} + R_C \right)}{R_{2_i} + R_{1_i} + R_C}$$

$$v^h_{\mathrm{SM}_i}(t-\Delta t) = R_{\mathrm{SM}_i}(t) \left(\frac{R_C}{R_C + R_{2_i}} \right) i^h_{C_i}(t-\Delta t)$$

e) Compute voltages of each SM:

$$v_{SM_i}(t) = i_{arm}(t) R_{SM_i}(t) + v^h_{SM_i}(t-\Delta t)$$

f) Compute and send Norton equivalent (Fig. 6):

$$Y_{arm}(t) = 1 / \left(\sum_{i=1}^{N} R_{\mathrm{SM}_i}(t) \right)$$

$$v^h_{arm}(t-\Delta t) = \sum_{i=1}^{N} v^h_{\mathrm{SM}_i}(t-\Delta t)$$

$$i^h_{arm}(t-\Delta t) = -v^h_{arm}(t-\Delta t).Y_{arm}(t)$$

Fig. 5 SSN-MMC arm algorithm

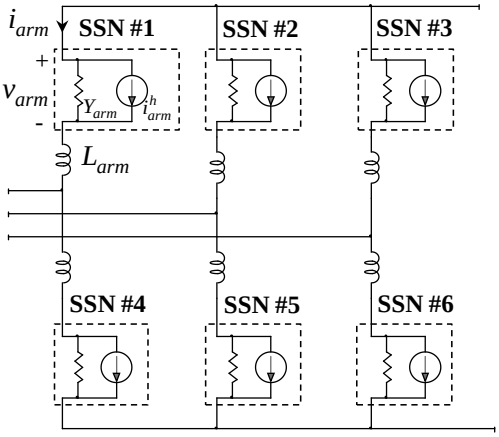


Fig. 6 SSN-MMC model

V. System set-up and Validation

The case study is a HVDC-VSC transmission system with a MMC-101 Level (Fig. 7). The control strategy considers an active/reactive power control on the sending end (VSC-MMC station #1 + Rectifier control) and a dc voltage/reactive power control on the receiving end (VSC-MMC station #2 + Inverter control). Further details on the control system used in this article are described in [14]. The ac grids are represented as equivalent sources with a short-circuit level of 10,000 MVA. The transmission capacity of the system is 1,000 MW. Rest of the details are shown on Fig. 7.

A. Coherency consideration between SPS/Artemis and EMTP-RV

In order to achieve real-time simulation, the first task is to transfer the original MMC based HVDC system model achieved in EMTP-RV to the Matlab/Simulink software using SPS and Artemis tools. By using Opal-RT eMEGAsim real-time simulator and the SSN solver, the transferred system can then be simulated in real-time [15]. However, each MMC-101 Level detailed model is composed from more than 6,000 electrical components including 2,400 nonlinear devices. It is practically unfeasible in SPS/Artemis tools since it would require a huge amount of computation time, thus the reference model is built and kept only in EMTP-RV. In order to validate the MMC model, it is essential that all other components of the system are identical or similar.

The control system of a HVDC can be translated block by block from one software to another. However, this task is time consuming and a significant effort is required to insure that the exact blocs are used and no mistakes are driven, especially for the complex control system. The Dynamic-Link Library (DLL) interface in EMTP-RV [16] allows combining different programming languages. By using this later, the generic control system developed in Simulink is directly interfaced with EMTP-RV [16]. This approach simplifies software interoperability and guaranties the concordance of control diagrams [17].

Regarding the power components, such as voltage sources, transformers, breakers and cables, the translation is performed manually using compatible devices.

Some differences are inherent to software packages:

- Integration method: EMTP-RV uses trapezoidal integration and Backward-Euler with half time-step to account for discontinuities. Also, an iteration process is used for non-linear devices. However, in Simulink a wide range of solvers exists. The Art5 with Backward Euler nodal interface is chosen for the reasons explained in the previous section.
- Equation type: EMTP-RV uses modified-augmented nodal equations, whereas SPS uses state-space equations.

B. From offline to real-time simulation

To simulate an electrical network in real-time, it is necessary to separate the network into sub-networks. Thus, each sub-network is simulated on one processor, which parallelizes the computation of the network and thus accelerates the simulation speed. Fig. 7 shows the separation of the HVDC-MMC system in 6 cores: CPU1 and CPU2 for each VSC-MMC station (each processor includes the SSN-MMC model), CPU3 and CPU4 for each equivalent network and CPU5 and CPU6 for each control system.

The distributed parameter models (DPL) for cables are used to decouple between both converter stations, and stubline blocks are used to decouple between stations (CPU1 and CPU2) and the equivalent networks (CPU 3 and CPU4). More details about these decoupling technics can be found in [15].

C. Real-time Model accuracy verification

This section compares the dynamic behavior of the SSN-MMC model against the reference model (section III). The modulation technique used in this article is the Nearest Level Control [19]. Based on [19], the sampling period for MMC-101 Level is (on average) $63.7\ \mu s$. The reference model simulated offline in EMTP-RV uses a time-step of $5\ \mu s$ for accuracy verification. Whereas, the SSN-MMC model simulated in real-time in the Opal-RT simulator (OP5600) uses a time-step of $30\ \mu s$. For all results, blue solid lines denote detailed model waveforms and the green dotted color is used for the SSN-MMC version.

Model validations are performed on realistic test cases: start-up sequence, circulating current variation, capacitor voltage variation, ac fault and dc fault.

1) Start-up sequence

This test studies the start-up sequence of the converter: all capacitor voltages are initially set to zero and all SMs are at BLOCKED state. The "main AC breaker" (Fig. 7) is closed and the "bypass breaker" is kept open for this test case. An insertion resistance of $1\ \mathrm{k}\Omega$ is connected between the converter and the secondary of the transformer in order to limit the inrush current during converter energization. Results are compared in Fig. 8.

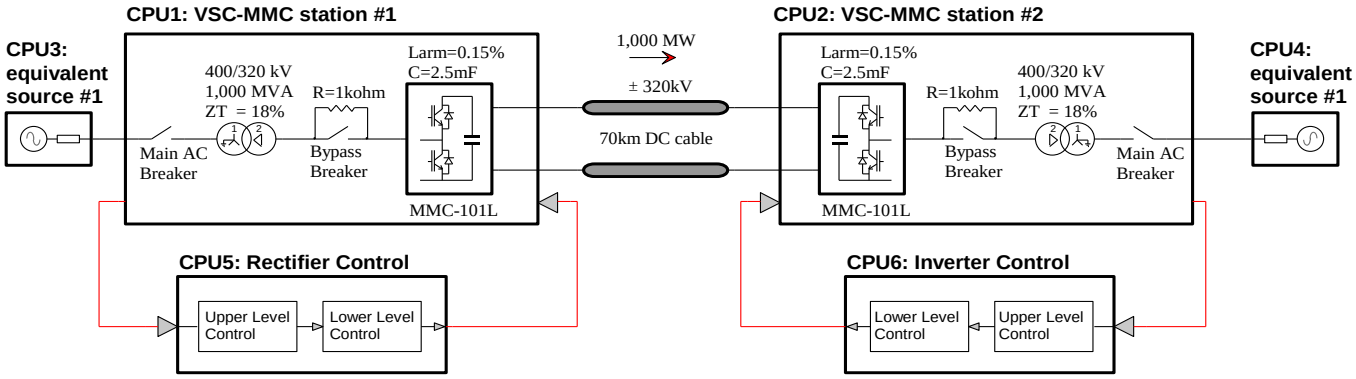
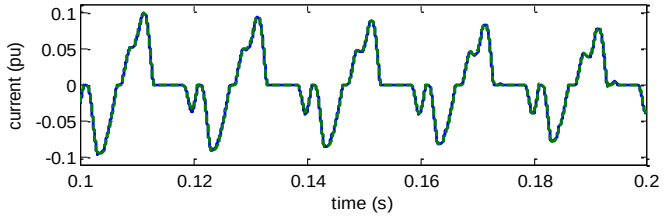
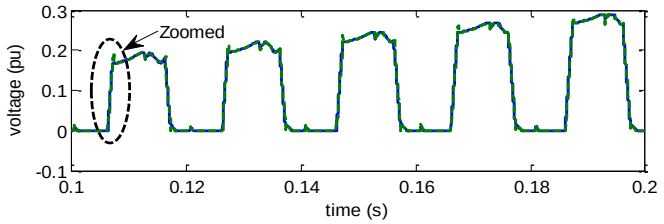


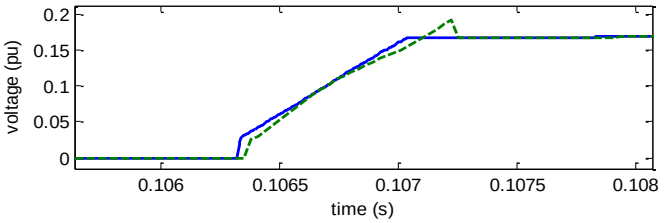
Fig. 7 MMC-HVDC transmission test system.



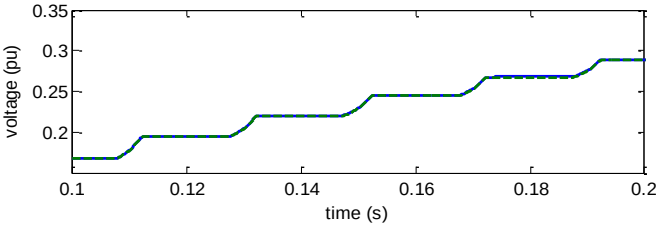
a) MMC current upper arm of phase A station #1



b) MMC voltage upper arm of phase A station #1



c) Zoomed waveforms, MMC voltage upper arm of phase A station #1



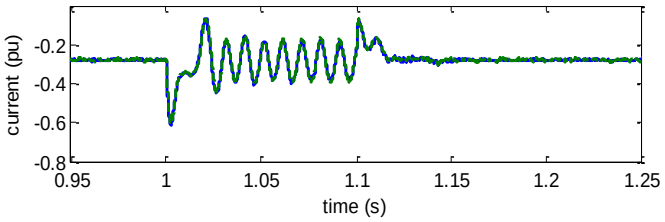
c) Sum of all capacitor voltages of MMC upper arm phase A station #1

Fig. 8: start-up sequence of Station#1 phase A upper arm

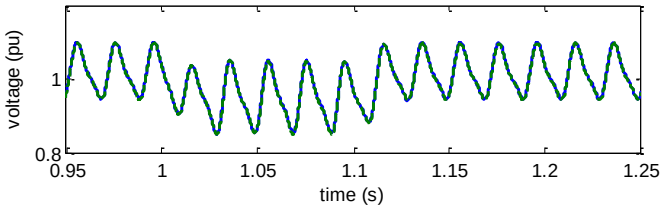
From the zoomed waveform of Fig. 8.c, a one time-step delay and a slight impulse are seen when conduction state changes occur. This is related with the blocked state implementation and cannot be avoided without an iterative process as stated in section IV. Nevertheless, the rest of the results in Fig. 8 show a good agreement between that SSN-MMC model and the detailed model for a start-up sequence. The agreements have been verified for all other ac and dc variables of the system.

2) Deactivation of circulating current controller

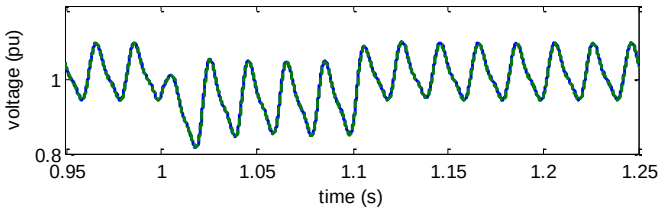
Internal MMC variables are evaluated in this section. The unbalances between arm phases introduce a circulating current which increases losses. The circulating current suppression control (CCSC) [20] is implemented in the control system to overcome this issue. In order to evaluate the circulating current variable when subjected to perturbations, the CCSC in the rectifier control (CPU5) is deactivated intentionally at $t = 1$ s for 100 ms. Internal variables are presented in Fig. 9.



a) Circulating current of phase A station #1



b) Sum of all capacitor voltages of the upper arm phase A station #1



c) Sum of all capacitor voltages of the lower arm phase A station #1

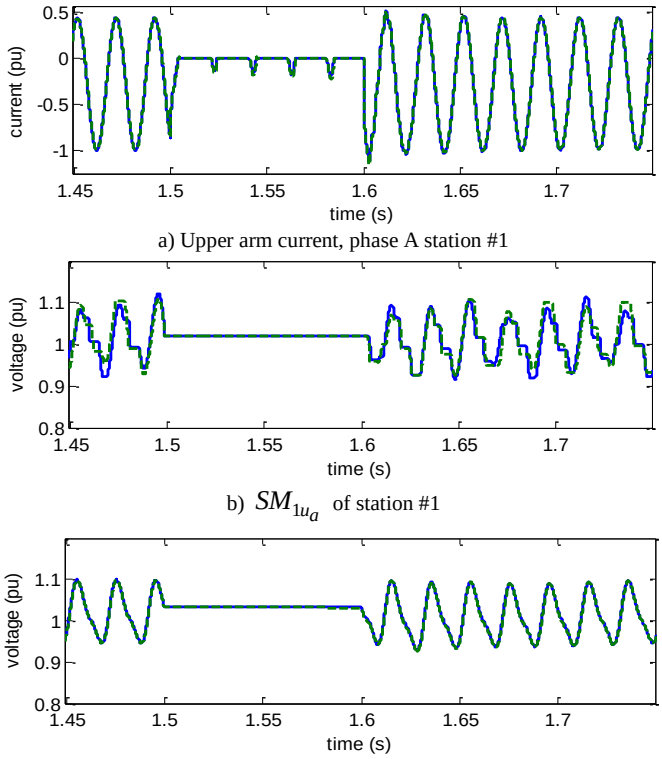
Fig. 9 CCSC deactivated in Station#1 phase A

It can be concluded that SSN-MMC models give also similar and accurate results for analyzing arm variables. Relative errors of these variables are in the range of 0.5 to 4 %.

3) Blocked state applied on one MMC arm

The capacitor voltage variables of SMs are studied in this section. All SMs of phase A upper arm of station #1 are set to BLOCKED state at t=1.5 s for 100 ms during normal operation. No special protection system has been added in

order to overcome this malfunction condition. Comparisons are presented in Fig. 10.



a) Upper arm current, phase A station #1

b) SM_{1u_a} of station #1

c) Sum of all capacitor voltages of the upper arm phase A station #1

Fig. 10 Blocked state applied in Station#1 phase A upper arm

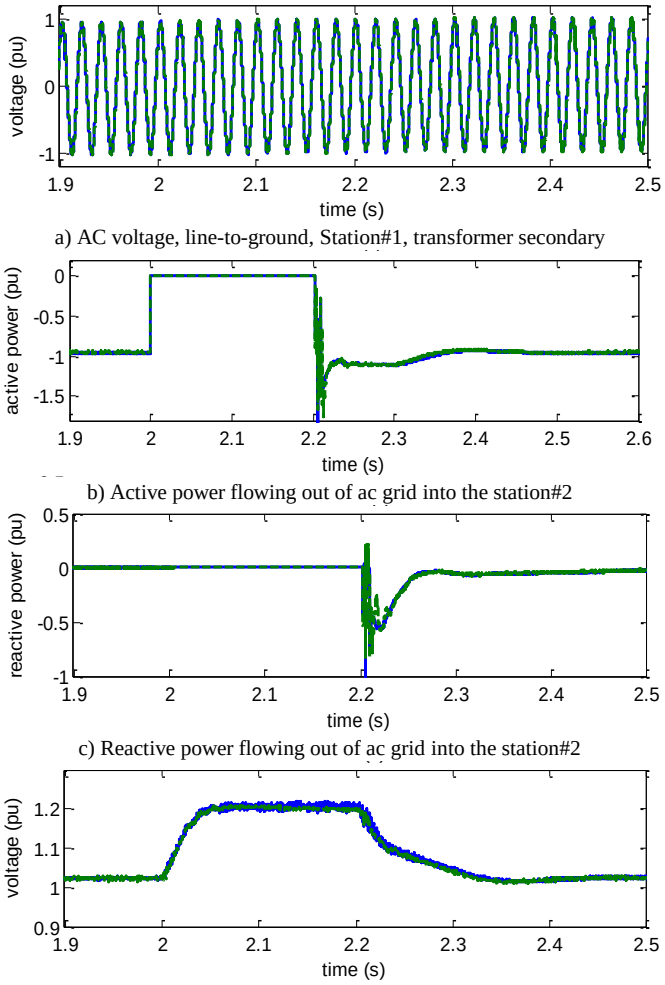
The differences depicted between SM_{1u_a} (Fig. 10.b.) are related to the capacitor balancing control strategy and not to the MMC model. This later control, selects the optimal SM that has to be switched ON/OFF. These selections are not necessary identical between two simulations, which make each SM choices different between simulations. However the sum of all capacitor voltages of each arm should be identical for both models, which is the case as shown in Fig. 10.c. The relative errors are on average of 0.5 %. To conclude, this test case shows also that the SSN-MMC model gives accurate results for internal variable perturbations.

4) Three-phase AC Fault

A 200 ms three-phase-to-ground fault is applied on the ac side (between CPU2: station#2 and CPU4: equivalent source#2) at 2 s of simulation time. Fig. 10 compares the dynamic responses. As it can be seen, a good agreement can be achieved for transient events on the ac side.

5) Pole-to-pole dc Fault

The models are tested for a permanent dc fault between the positive and negative poles in Station #2 applied at 3 s of simulation time. The following clearing fault method is used [21]: all thyristors (K2) are fired and all IGBTs are blocked 400 µs after the fault, and the "Main AC Breakers" (Fig. 7) of both VSC-MMC stations are opened after two cycles. The dc current flowing out from station #1is compared in Fig. 12.



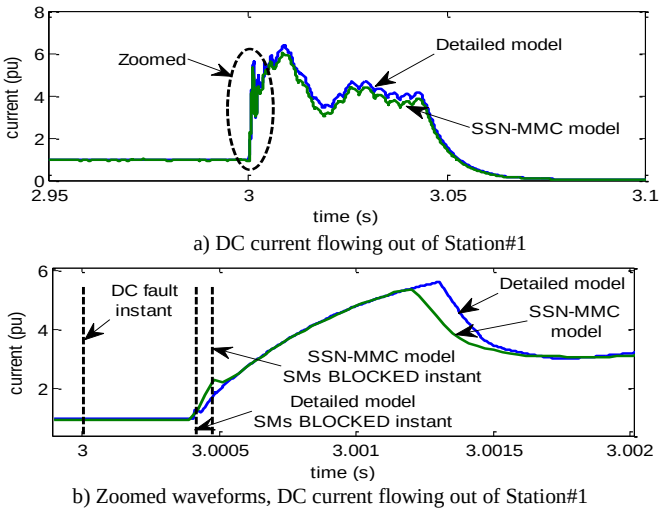
a) AC voltage, line-to-ground, Station#1, transformer secondary

b) Active power flowing out of ac grid into the station#2

c) Reactive power flowing out of ac grid into the station#2

d) DC voltage, Station#1

Fig. 11 AC three-phase-to-ground fault on station#2.



a) DC current flowing out of Station#1

b) Zoomed waveforms, DC current flowing out of Station#1

Fig. 12 DC current, pole-to-pole fault on Station#2 side.

Fig. 12 shows differences between the two models, the maximum amplitude reached from the reference model is 6.2 pu and instead the real-time simulation gives a peak current of 5.9 pu. Investigation shows that these differences are due to different cable models used in both software packages. Another cause of discordance is in the time-steps used for both

simulations. These time-step differences also impacted slightly on the Blocked state instant highlighted in Fig. 12.b. However, the global behavior of the SSN-MMC model follows clearly the reference model.

VI. Real-time simulation Performance

The real-time performance of the SSN-MMC model is studied in this section. The simulations were performed on the Opal-RT simulator (OP5600). In Table 1 the execution time of the processors dedicated to VSC-MMC stations (CPU1 - CPU2) are evaluated for several MMC levels.

TABLE 1
REAL-TIME PERFORMANCE OF SSN-MMC MODEL

Number of SM/arm	Execution time of VSC-MMC station (CPU1 or CPU2) in μs
40	13.5
60	17.4
80	20.6
100	24.1
120	28.3
140	32.0

Unlike the exponential evolution of the execution time as a function of the number of MMC levels presented in [7], Table 1 shows a linear relation between these two parameters. This demonstrates the efficiency of the SSN-MMC model presented in this paper. In Table 1, the execution times represent also the minimum step-time required for simulating the SSN-MMC model in real-time.

VII. Conclusions

This paper presented the implementation of MMC models for real-time simulation studies using the SSN method. A detailed reference model based on EMTP-RV has been used for validations. Several test cases, including perturbation of internal variables and blocked state events show the good accuracy of results from the SSN-MMC model. Real-time performance for different numbers of MMC levels demonstrates a linear proportional behavior between processor execution time and number of levels.

The SSN-MMC model presented in this article uses only one processor. For higher MMC levels, execution time becomes excessively high. Thus other solutions may be considered in order to decrease the computational burden as: parallelizing the MMC arms in a multiprocessor, or implementation of the SSN-MMC model on a field-programmable gate array (FPGA).

VIII. References

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